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Review of VLSI Architectures for FM0 Encoder and Manchester Encoder

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ABSTRACT: Communication process mainly depend upon the encoding and decoding techniques.The various architectures uses different forms of encoding techniques such as Miller, NRZ, FM0 and Manchester encoding. The finite state machine (FSM) can be used for all encodings, because at a time the input has given the corresponding output can be occurred due to this. Therefore results speed increased. This paper gives a review on different VLSI architectures of FM0 and Manchester code .The purpose of the FM0 and Manchester codes to reach dc-balance and enhancing the signal reliability etc.

KEYWORDS: Manchester encoder, FM0 encoder, FSM.

I. INTRODUCTION

Various Types of Encoding and decoding are used in data communications and networkingto convert information into a specialized format which can be suitable for efficient transmission and storage.Encoding techniques can also be used for security purposes. There are many ways to encode the data such as Miller encoding, Manchester encoding, FM0, NRZ, etc. In data communications, Manchester is a special form of encoding in which the binary digits (bits) represent the transitions between high and low logic states. This types of encoding is used on the transistor level for optical communication [1], minimizing the critical path, area, delay, and buffer size by adding a minimum number of buffers [2]. The terms encoding and decoding are often used in reference to the processes of analog-to-digital conversion and digital-to-analog conversion.A baseband processor such as a UHF RFID Reader, PIE encoder, FM0 decoder, or Miller decoder are used for encoding and decoding purposes, achieving higher efficiency and accuracy [3]. But in order to do this, it needs a high frequency clock [4].This paper is organized as follows: In section II, description of Manchester and FM0 encoding techniques is given. This section also exploit the FSM based architectures of Manchester and FM0 encoder. Next, section III gives the simulation results of both encoders. A brief application details of above architectures given in section IV. Finally in section V, we give conclusion and talk about future work of this paper.

II. ENCODING TECHNIQUES

A. FSM BASED MANCHESTER ENCODER :

The Manchester code is a very popular code as it is level insensitive, self-clocking, and it provides signal absence detection as the coded signal has always at least one transition per bit.Manchester code uses the negative falling edge of the high-to-low level transition torepresent logic 0 and the positive rising edge of the low-to high level transition to represent logic 1, therefore Manchester code is also called split phase coding or dual-phase coding. Figure 1, shows illustration of Manchester encoding example, where Clock signal and the input data are abbreviated as CLK and X respectively.Manchester encoding is Bi-phase encoding as there is simultaneous transition between the logic level 1 and logic level 0, thus long stream of logic 1 or logic 0 never occurs in Manchester encoded data. This give rise to zero DC power of the Manchester encoded data. These transitions contain sufficient information and are used to trace-out the clock from the Manchester encoded data, hence there is no need of clock at the receiver side for decoding the data. Therefore, while transmitting the data, the number of wires is minimized, which can be used to reduce the noise and transmission power.To obtain a high speed, provide a synchronized data source as the first clock pulse for input data.While transmitting the data, it is a digital encoding in which data transmission bits are represented bytransitions from

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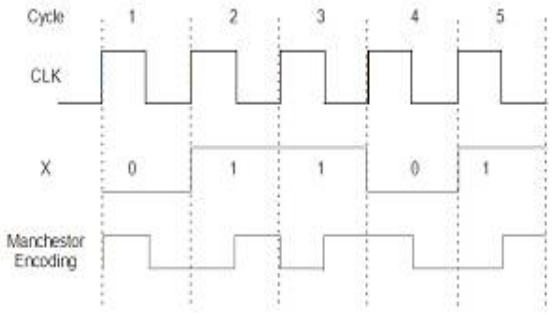

Figure 1. Illustration of Manchester Encoding.

one logic to another logic. The length of each bit is set as default this makes the signals as self-clocking. The state of a bit is determined according to the direction of the transition. The operation of the Manchester encoder is an exclusive

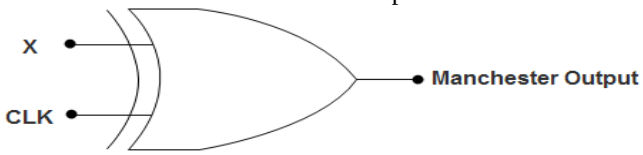

Figure 2. Manchester Encoding.

OR of the input signal with the clock signal as shown in figure 2.The operation of the Manchester encoding is given in table 1 below.The FSM of Manchester encoder can be design using four states as SO, S1, S2, and S3 shown in the following table 2.

Original Data	Clock	Manchester Value
0	0	0
0	1	1
1	0	1
1	1	0

State Names	Binary Encoding
S0	00
S1	01
S2	10
S3	11

Table 1: Operation of Manchester Encoding. Table2: Manchester State Encoding.

The corresponding finite state machine of the encoded signal is represented as in figure 3[5].

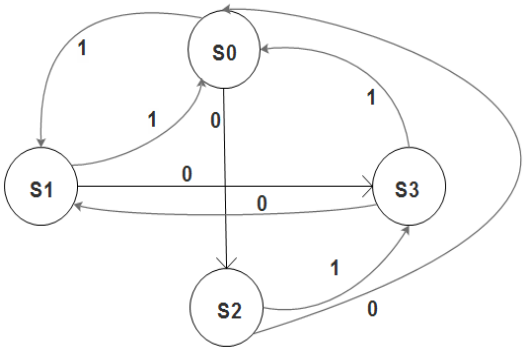

Figure 3: FSM of Manchester.

Based on the above FSM, the transition table of the above-mentioned state diagram is shown in table 3[5].

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Present State	Input		Next State	
	0	1	0	1
S0	0	1	S2	S1
S1	0	1	S3	S0
S2	0	1	S0	S3
S3	0	1	S1	S0

Table 3: Manchester Transition table

The main advantageof Manchester encoding is that the signal synchronizes itself, minimizes the error rate, and optimizes the reliability. There is no DC component and so a signal encoded in it can be AC coupled .The drawbacks to this encoding are that more bits are needed to transmit in the encoding signal than the original signal, thus it needs more bandwidth. Also the decoding circuitry is also complex.

B. FSM BASED FM0 ENCODER:

FM0 is also Bi-phase code. In FM0 encoding transition is present on every bit and an additional transition may occur in the middle of the bit. Also these transitions also contain sufficient clock information so that encoded data can be recovered from the FM0 data stream therefore no separate clock is needed for decoding at receiver side. Results in number of wires are minimized for transmission. It has also reach DC balance and thus enhance the signal reliability. It is used to reduce noise and transmission power. Rules for FM0 encoding are as follows:

1. When X is at logic 0,there is transition in the center of the bit.
2. When X is at logic 1 there is no transition from the center of bit.
3. The transition is allocated among each FM0 code no matter what the Xis.

Figure 4 below illustrate the FM0 encoding based on the above rules.

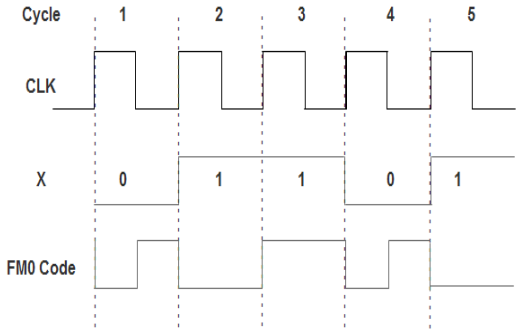

Figure 4: Illustration of FM0 Encoding

Based on above encoding principle of FMO, FSM of FM0 shown in figure 5[6]. The FSM of FM0 code is classified into four states namely S1, S2, S3, and S4. A state code is individually assigned to each state as shown in table 4 below. The state labels also represent the FMO waveform that is transmitted upon entering into the state. The label on the state transitions indicates the logical value of the data sequence to be encoded.

FSM of FM0 can be described as, when X is logic-0, the state-transitions of state S1 and S3 follows both rules 1 and 3. Also when the X is logic-1, the state-transitions of states S2 and S4 follows both rules 2 and 3. Thus, FSM of FM0 can be completely constructed form state-transition of each state. Based on above FSM state transition table of FM0 shown in table 5 below.A Block diagram for Hardware architecture of FM0 encoding constructed from FSM of FM0 shown in figure 6 below.The block diagram has an XOR gate, DFF1& DFF2, inverter, and MUX. FM0 encoding not only depends on X but also on the previous-state of the FM0 code.DFF1 and DFF2 store the state code of the FM0 code.Outputs of both FF's given to theMUX with the selection of CLK signal. For MUX if CLK signal is 0,it selects

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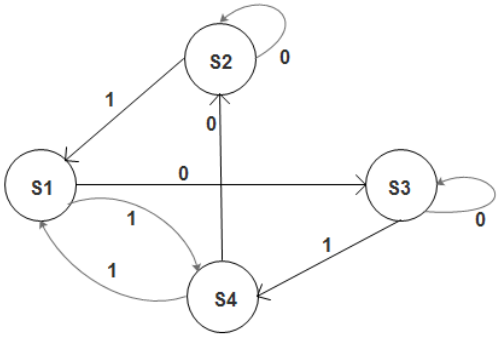

Figure 5: FSM of FM0 Encoding

State Names	Binary Encoding
S1	11
S2	10
S3	01
S4	00

Table 4:FM0 State encoding table

Present State	Input		Next State	
	0	1	0	1
S1	0	1	S3	S4
S2	0	1	S2	S1
S3	0	1	S3	S4
S4	0	1	S2	S1

Table 5: FM0 Transition Table

DFF1's output as FM0 code and if CLK of MUX is 1then it will select DFF2's output as FM0 code output.

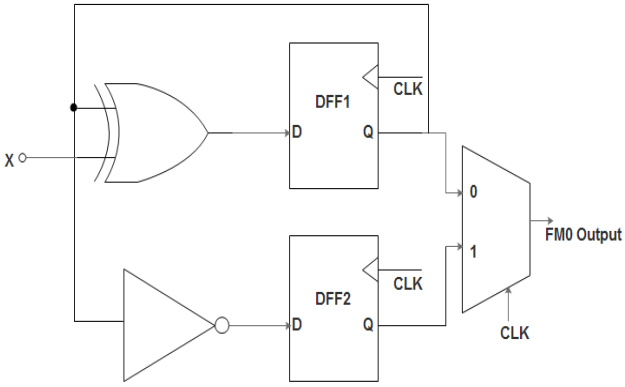

Figure 6: Block diagram for FM0 encoding

III. SIMULATION RESULTS

A. SIMULATION OF MANCHESTER ENCODER:

The state machine of Manchester encoder is written in Verilog HDL language and simulated on ModelSim 6.0. The simulation waveform of FSM based design for Manchester encoder is shown as follows in figure 7[5].Depend upon the input and clock, value of data output changes. Manchester encoder is XOR operation between original data and CLK signal. The input 'a' is 1 and the 'clk' is given as a rising edge which produces the output as 0. Depending up on the data value, output bit changes per clock cycle. Waveforms of figure 7[5] below verifies functionality of FSM based Manchester encoder.

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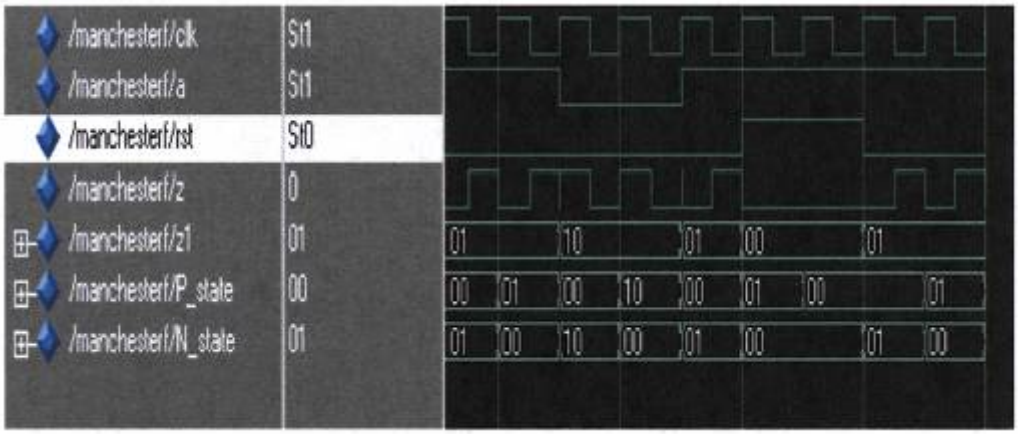

Figure 7: Waveform of FSMBased Manchester Encoder[5]

B. SIMULATION OF FM0 ENCODER:

The state machine of FM0 encoder is written in Verilog HDL language and simulated on ModelSim 6.0. The waveform of FSM based design for FM0 encoder is shown in figure 8[6] below. FM0 operation depends on values of 'clk', input 'a', and 'rst' as shown in figure 8[6] below. The input 'a' is 1 and the 'clk' is given as a rising edge which produces the output as 0. Also depend upon input data value output bit changes per clock cycle. Waveforms of figure 8[6] below verifies functionality of FSM based FM0 encoder.

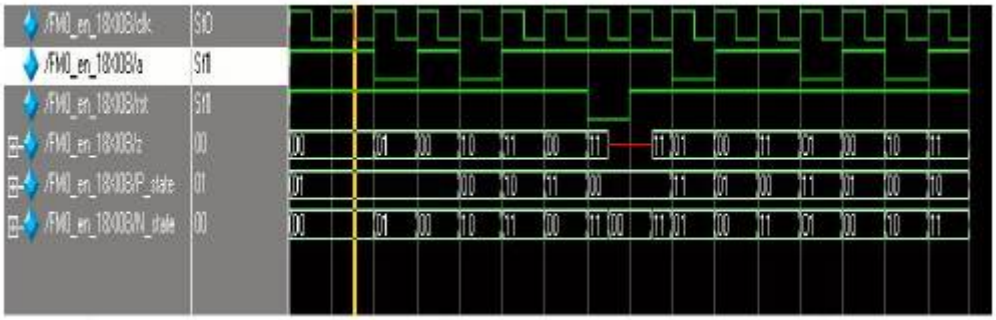

Figure 8: Waveform of FSM based FM0 Encoder[6]

IV. APPLICATIONS

It can be used in many applications like library RFID management systems having advantages like high reliability, automated materials handling, and long life. Likewise some other applications are E-passports, supermarkets, transportation, and tracking.

V. CONCLUSION AND FUTURE WORK

The presented work exploits the design strategies of the Manchester and FM0 encoders and finite state machines for both encoders has been designed using Verilog hardware description languages. The simulation waveforms confirms the functionality of the encoders. Since the coding diversity between FM0 and Manchester encoding limits the potential to design fully reused VLSI architecture thus hardware utilization rate of these architectures remains low. This encoding concept and with efforts to design a fully reused VLSI architecture for FM0 and Manchester encoding to use in variousapplications will be added as future work.

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