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Design Implementation and Functional Verification of AMBA Advanced Peripheral bus Protocol using UVM

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ABSTRACT: The on-chip bus in system-on-chip implements architecture called Advanced Microcontroller Bus Architecture (AMBA). AMBA is extensively implemented in the Application Specific Integrated circuit (ASIC) and SOC components. Advanced Peripheral Bus (APB) is a low-bandwidth and low-performance bus connected to low bandwidth peripherals like Keypad, UART, timer, etc... For interfacing purposes, low execution transport and fewer data move capacity in APB are used. The paper proposes the design and verification of the APB Protocol. The design is implemented using Verilog HDL and test cases are generated. The verification is carried out using Universal Verification Methodology (UVM). The software used here is Synopsys with technology. A standard methodology for the verification of an Integrated Circuit (IC) design is UVM.UVM Consists of a set of base classes with methods defined in it.

KEYWORDS: System-on-chip; Universal Verification Methodology; Bus Architecture; Advanced Peripheral Bus; Universal Verification Methodology; Verilog HDL.

I. INTRODUCTION

To overthrow the challenges so far for realizing the opportunities introduced by density and capability of semiconductors, electronic companies employ a SOC design methodology by including the proposed components called as SOC-Intellectual property. SOC is defined as a complex IC which integrates the utmost functional elements into the product forming a single chip. It contains analog, mixed, and digital signal and speed functions all located on a Single substrate [1]. These days in this era of modern technology, more devices are integrated with SOC form. In electronics industry SOC's are very commonly used due to its low power consumption and also embedded system makes great use of it. Some of the advantages of SOC's are low power, low cost, small size, fast operation, and disadvantages are increase in complexity, cost, and more complicated verification.

Reusable IPs fit for the improvisation of an ARM particularly focuses on the crucial of any Application Specific Integrated Circuit (ASIC) configuration. Rather than schematic graphs most of the Interconnections in checked IP squares and blocks depend upon the Hardware Description Language (HDL). They are Register transfer level (RTL) codes which are robust tried in the improvement of SOC.

A SOC principal feature is not only about the components and blocks it comprises but also about the interconnection between them. So, AMBA plays an important role in the interfacing of this block with each other. AMBA is a set of interconnecting specifications given by ARM which standardizes the on-chip communication between different blocks for the construction of High-Performance SOC Design. It is a freely available, platform-independent, open standard for interconnection among the blocks in SOC design and can be implemented with any processor architecture. AMBA usually consists of at least one or more microprocessors or microcontrollers along the internal or external memory bridge, Digital signal processing (DSP), Direct memory access (DMA), and other peripherals such as UART, Keypad, etc all are integrated on a single chip [2]. The primary motivation of AMBA is to have an efficient and standard way for the interconnection of blocks with reuse across multiple designs.

Figure 1 shows AMBA architecture mainly had 3 components, namely advanced system bus, advanced high bus (AHB), APB. The first two protocols are for high bandwidth interconnection and they are high-performance buses. So the higher bandwidth components such as on-chip RAM, DMA bus master, memory interface, and High-performance

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ARM processor. The AMBA 3 protocol family includes APB. It is an unpipelined protocol [3]. This paper presents the read and writes transfer without wait states of APB protocol.

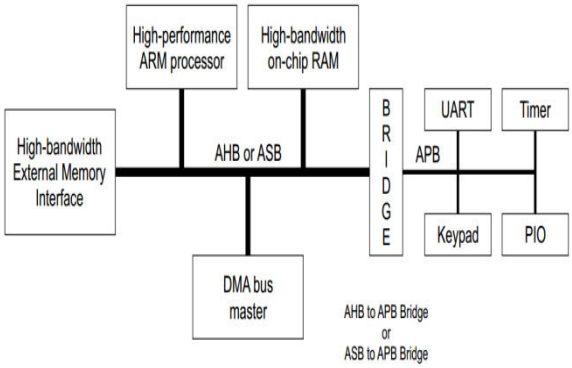

Figure 1: AMBA Architecture [4].

Open verification methodology (OVM) derives Universal verification methodology (UVM) which is given by an Accellera standard with EDA tool vendors. It is a standard verification methodology. With the help of UVM, more advanced methods are present in verification technology with the creation of reusable, robust, interoperable verification and test benches [5]. In this paper UVM is used for the verification Due to the For the newly joined and advanced teams in verification technology, UVM addresses the complexity in verification and interplay with companies and all over the electronic industry to provide consistency. Some of the common scripting languages are Python and Perl.

II. LITERATURE SURVEY

In an article [6], the APB bridge is implemented in an efficient arrangement of the system schemes are proposed. During the design of any sequential system, the clock becomes the major concern because when there is a generation of difference between the arrival times of clock signal then clock skews are introduced. The author proposes a ripple counter for the reduction of these clock skews.3-bit down ripple counter is implemented using Verilog HDL. An 8-bit APB bridge implementation is done on the Zync board. Vivado Design Suite ISim has been used for simulation and synthesis and design utilization summary Vivado Integrated Design Environment. (IDE) is used.

In the paper [7], APB Convention is implemented with the ASIC design flow has been proposed. The author presents the structure of APB. In APB, the peripherals are interfaced with the help of low data move capacity, low execution transport present. The ASIC execution of the present design is done in a synopsis toolchain with a 32nm library and verified utilizing UVM.

At the end of the paper, the author gives an ASIC design for APB by using Verilog HDL according to their constraints. Here design deals with maintaining the balancing between speed and region overhead. In the results and discussion, the APB simulation result is described. The read-write activity is carried with and without wait states.

In an article [8], the author proposes the IP core of the APB Bridge, which translates the capital AXI4.0-lite transfers into the APB4.0 specifications given by ARM in March 2010. Here the bridge provides the interfaces between the low-power APB domain and high-performance AXI bus. The author concludes that features of the implementation are proven as the PCLK clocked domain and the ALCK domain are completely independent and 32 bit APB master and AXI slave interface are achieved. It supports up to 16 APB peripherals.

In paper [9], the author describes the successful change in the widespread acquisition of system Verilog features for the verification in UVM. System Verilog verification is similar to the UVM verification for some users. This paper discusses the relations between UVM and System Verilog, by the addition of features in system Verilog which made the UVM smaller, easier to understand, and to use. At the end of the paper, It may look like the UVM fills all the drawbacks in the system Verilog but it is not the case with the author. So, according to the author System, Verilog and UVM have their advantages and disadvantages.

In paper [10], the authors present the rapid growth in SOC for the integration of many hardware accelerators into them. The challenges are performance goals, time to market, and functional verification. The author proposes a methodology on the vision-based hardware accelerators of SOC by tracing efficient and rapid ways for verifying their performance. The author concludes by proposing a methodology efficiently and rapidly for the verification of the accelerators. The effective method for the particular is by simulating at low resolution so that it reduces simulation time.

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III. APB DESIGN

The APB is represented by the AMBA protocol family. It is low bandwidth and a low-cost interface which reduces complexity during interfacing and reduces power consumption [11]. The APB can be interfaced to the peripherals which are low bandwidth such as UART, Keypad, etc. It has an unpipelined protocol thus a high-performance bus interface is not needed. The transition of signals is carried out during the rising edge of the clock for the integration of APB peripherals. From this APB can be implemented into any design flow.APB is a peripheral bus run at a speed of ~100MHZ. For every data transfer, it takes 2 cycles they are – setup cycle, Access cycle.

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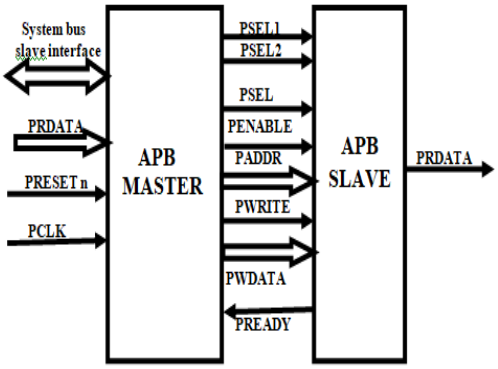

Figure 2: APB Block diagram.

Signal	Source	Description
PCLK	Clock source	The rising edge of PCLK times.
PRESET	System bus	The reset signal is active low.
PADDR	APB bridge	32-bit wide bus directed by the bridge unit.
PSELX	APB bridge	APB bridge generates this signal for each slave.
PENABLE	APB bridge	This signal represents the other two cycles after the default cycle.
PWRITE	APB bridge	When this signal is high it indicates APB write access and when low indicates the APB read access.
PWDATA	APB bridge	32-bit wide bus. Directed by bridge during write cycles.
PREADY	Slave interface	This signal extends APB transfer.
PRDATA	Slave interface	32-bit wide read data. Based on PSEL of slaves this bus is driven during read cycles.

Table 1: List of APB signals.

There are 2 independent data buses present in the APB protocol –Read data and write data are up to 32 bits wide. As there were no individual handshake signals for these buses the data transferring is not possible to occur on both the buses at a time [13].

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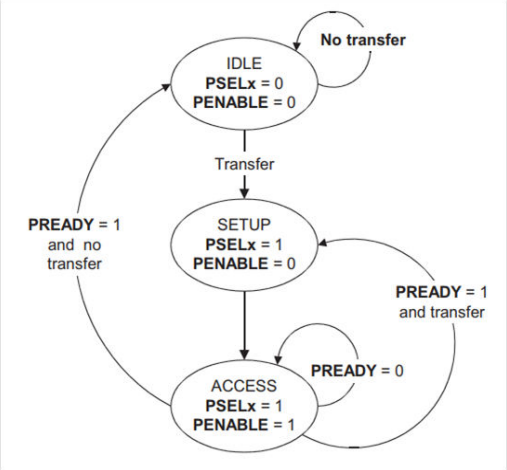

Figure 3: APB state diagram [14].

Figure 3 shows the state diagram of the APB protocol. There are three states, Idle, Setup, and Access states. In Idle state, at first clock cycle, the PSELx and PENABLE are low, there will be no data transfer. When PSELx has asserted the bus waits in the setup state for only one clock cycle. In the next rising edge the PENABLE gets high, the access state gets asserted. During the transition from setup state to access the PWRITE, PSELECT, and write data signals must be stable [15]. If PREADY becomes low then a bus will be in an access state and if it becomes high then it exits from the access state and returns to an idle state.

A. Write the transfer without wait states

At the first rising edge of the clock cycle, write transfer starts with composing activity with address location (PADDR), data (PWDATA), and signal (PWRITE). The first stage of the clock cycle is the Setup stage/Phase starts with data transfer. During the next edge of the clock cycle, the PENABLE gets asserted and the Access phase takes place [16].

During the access phase all the other control signals, information, locations are kept valid. The transfer ends with the completion of the clock edge during the Access cycle. The PENABLE is low after the completion. If there is no transfer followed by a previous transfer to the same peripheral, then the PSELx goes low.

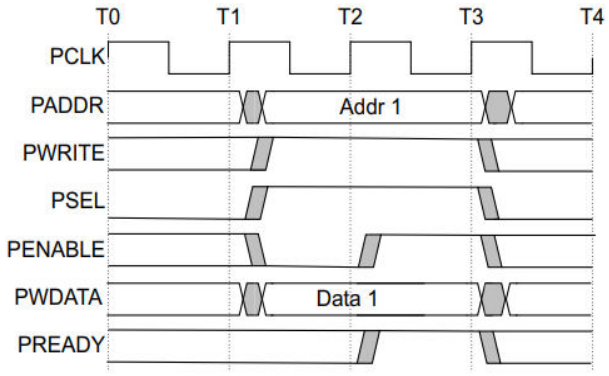

Figure 4: Without wait states for write transfer.

B. Read transfer without wait states

During the read transfer, the PSEL, PENABLE, PADDR, are kept the same as in the write transfer at the edge of T1 and PWRITE is kept low (setup phase). At T2, PENABLE and PREADY get asserted and read transfer is achieved. Here at the end of the transfer, the slave should provide data.

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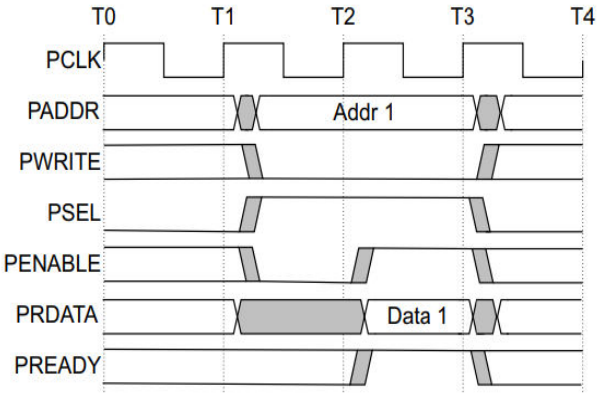

Figure 5: Without wait states for read transfer.

IV. VERIFICATION

During VLSI design flow, verification plays an important role. This verification helps to realize an error in the RTL design at a prompt stage. So that it won't affect the design process in the belated stage. Utmost 70% of the total time is kept for verification during the process and it is the most time-wasting process. With the rise of the transistors on IC's which causes a reduction in the feature size and use of design tools, the complexity in IC get increases. Hence, the need for the verification of IC is unavoidable.

UVM is a standard verification methodology for the verification of the register transfer level structure.UVM has a reusable verification environment i.e. verification components. Base classes of UVM are coded by the System Verilog. These components are encased, configurable, ready to use for protocol interfacing.

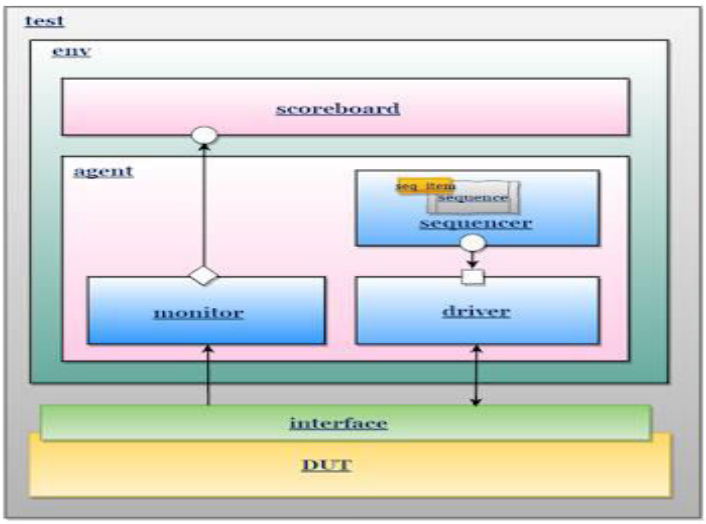

Figure 6: UVM Verification environment.

Figure 6 shows the UVM verification environment to verify the APB protocol.

A. UVM Testbench

In UVM the top entity is the UVM test. This test is instantiated on the test bench. This test bench instantiates the Design under test (DUT) and UVM test and forms a connection between them. It has Dynamic nature.

B. Test

The environment is instantiated in the test. A test can have multiple environments. The test is the top-level component in the UVM test bench.

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C. Environment

UVM environment is a hierarchical component that instantiates all the components they are agent, score board, or other environments are also instantiated in them.

D. Sequence Item

Each sequence consists of n number of sequence items. These are the extension from the uvm_sequence_item. This unit randomizes the data and address.

E. Driver

UVM_component extends the UVM_Driver. It communicates through TLM ports. It receives the sequence item transactions from UVM_sequencer and drives it on the DUT interface.

F. Monitor

It is analogous to the driver. It samples the DUT interface and sends it to test bench components. Analysis ports are used for communication.

G. Agent

UVM_Agent is extended from the UVM_ component. Agent comprises the driver, monitor, and sequencer.

H. Scoreboard

This checks the behavior of the DUT. The scoreboard receives the transaction which carries inputs and outputs of DUT through transistor level modeling (TLM).

V. RESULTS AND DISCUSSION

Figure 7 shows the read and write transfer of the data in hexadecimal format. From the simulation waveform, we can see that when the PWRITE is high the APB is writing the data and PWRITE is low APB reads the data

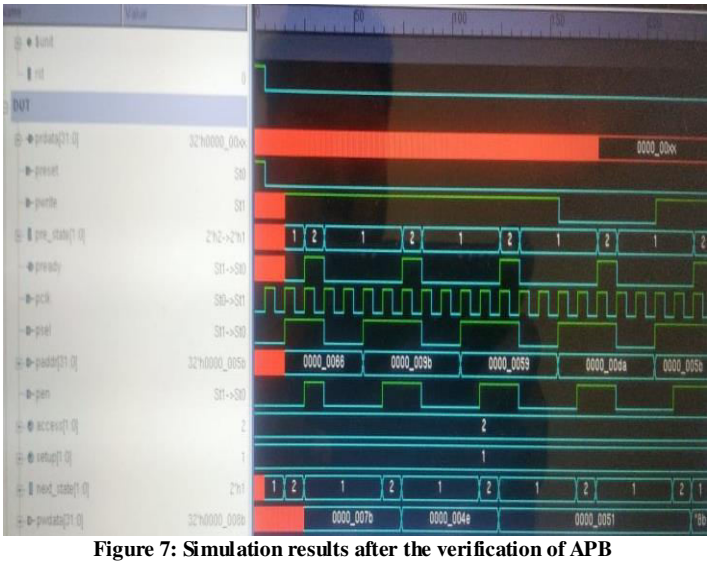

Figure 7: Simulation results after the verification of APB

Figure 8 shows the UVM report summary. The UVM_INFO shows thirty-five information messages. According to the UVM summary, the design is error-free and there is no more UVM_WARNING, UVM_ERROR and UVM_FATAL are zero.

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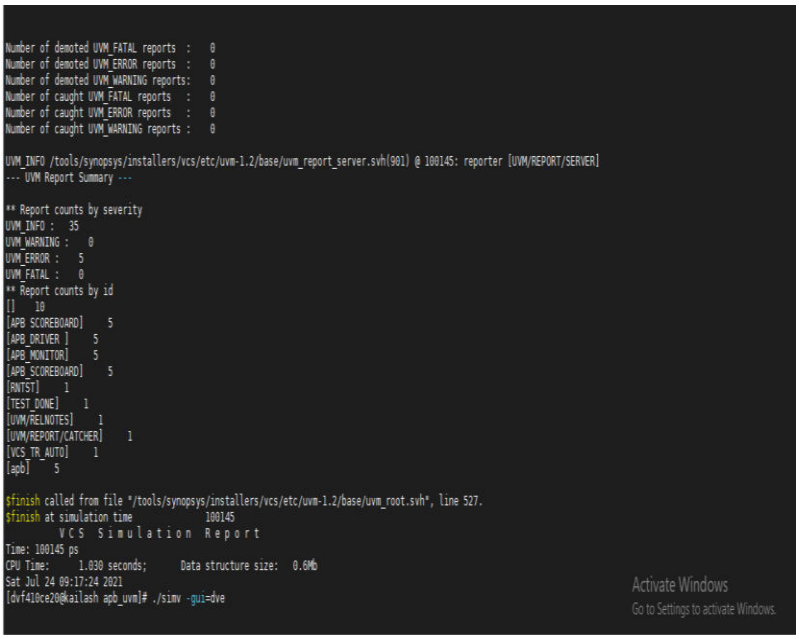

Figure 8: UVM Report summary.

VI. CONCLUSION

The main aim of the project is to design and verify an APB protocol using UVM. As a prior work to carry out this project, a literature survey has been done. APB protocol design is done for write and read operations without wait states and verification is carried out by using Universal Verification methodology using synopsis in 14nm technology. So, the simulation results show that the data read from the memory location is the same as the data written in that memory location. The UVM summary makes sure the accuracy of the design.

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