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5-Level Single Phase Multi-level Inverter: A Critical Review

Vivek Kumar[1], Prof. Amit Kumar Namdev[2]

M. Tech Scholar, Department of Electrical Engineering, Mittal Institute of Technology, Bhopal (M.P.), India[1]

Head of Dept., Department of Electrical Engineering, Mittal Institute of Technology, Bhopal (M.P.), India [2]

ABSTRACT: Energy is a critical component in the economic, social, and industrial growth processes. Because conventional energy sources are rapidly decreasing, the only answer is to use alternative energy sources. Apart from that, the transmission of power is also uneconomical in some situations, such as isolated areas and islands. As a result, it has become important to connect the main grid to a microgrid comprising renewable energy sources in order for the microgrid to ensure supply continuity in the case of main grid failure or a malfunction in the main grid. For grid connection, it is troublesome to connect power converters directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A MLI not only achieves high power ratings, but also enables the use of RE sources. RE sources such as PV, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. In this paper the study of multiplier level inverter and advantage and disadvantage are presented.

KEYWORDS: Multi-level Inverter, 5-level, Microgrid, Single Phase

I. INTRODUCTION

In modern technology, power electronics and processor plays a vital role in the field of motor control, light control, heat control, power supplies, vehicle system, HVDC, FACTS and renewable applications. The philosophy focuses on preserving the energy and meeting the power demand accurately and the power modulator pertaining to inverter / converter technology fulfills the requirements and this attracts the researchers to explore in the inverter field. The above-mentioned applications work in the range of medium power, high power at a higher voltage. With the help of semiconductor device technology, power converters are to be designed with higher operating voltage. As a single device fails to support such high voltages, a number of devices need to connect in series to meet the voltage rating. Another challenge in the industrial sector is the requirement and maintenance of the sinusoidal power supply with variable voltage and frequency. The above demerits are overcome by the introduction of Inverters. The series connected switches in the inverters and through control mechanism, the voltage stress with respect to high voltage rating is shared among the series switches and also the losses are minimized. Due to advantage of minimum losses, inverters is also used for medium voltage applications. The classical square wave inverter operating at higher voltage introduces the dominant harmonics, thereby the performance on the load side and on the front end of the inverter has a large impact and the performance is affected. Though the solution is sought through the passive filters, the loss are increased and occupies more space. The alternative path is provided by Multilevel Inverters (MLI) [1, 2]. MLI generates sinusoidal voltage waveform in the form voltage steps through switching sequence. The other advantages of MLI are reduced electromagnetic interference, reduced current distortion, good quality voltage waveform, good current waveform. The basic types of MLI are neutral point clamped MLI, flying capacitor MLI and cascaded H- bridge MLI. To synthesize nearly sinusoidal voltage, higher number of levels needs to be generated with the help of more number of switches, more number of sources and more number of gate drivers [3, 4]. Due to this, the efficiency decreases as more number of switches are utilized in the conduction path.

II. LIITERATURE REVIEW

Sen, P. et al. [1], multilevel inverters (MLIs) based on switched capacitors (SCs) are undergoing rapid development for a variety of dc-ac power conversion applications. This is because the voltage balancing and voltage boosting abilities do not require a complicated control circuit. Indeed, even with these significant benefits of SC geographies, a main point of contention in these circuits is the high inrush current while unexpected charging and releasing of capacitors. In this work, a new SCMLI circuit with fewer switches and a single source has been proposed to address this issue. The

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benefits of the proposed circuit, for example, voltage adjusting of capacitors without adding shut circle control, voltage supporting and single source necessities has roused the creators to utilize a similar circuit in photovoltaic (PV) application. The proposed SCMLI is connected with the PV frameworks through dc help converter. In addition to the SC network's ability to boost voltage, the dc-dc boost converter helps reduce inrush current caused by the presence of an inductor. A thorough comparison with existing configurations and an extensive simulation study of the proposed circuit's integration with the PV system confirm the advantages of the proposed structure.

Choi et al. [2], the decrease in the expense of photovoltaic (PV) energy is as yet expected to be serious as an elective energy source. The annual energy production as well as the reduction in the costs of operating and maintaining PV systems are both closely linked to the efficiency and dependability of PV inverters, making their improvement essential to lowering the price of PV energy. For efficiency and reliability enhancements, a single-phase IT-type NPC inverter with one-leg clamping pulse width modulation (OLC-PWM) is proposed in this article. Utilizing the advantages of I- and T-type NPC inverters in terms of power loss, the proposed IT-type NPC inverter with OLC-PWM can boost efficiency. Besides, its unwavering quality has been worked on contrasted and the customary I-type and T-type NPC inverters. The neutral-point voltage can also be balanced with the IT-type NPC inverter. Through simulations and experiments, the reliability and effectiveness of conventional I-type and T-type, asymmetric I-type and T-type, and IT-type NPC inverters are compared to demonstrate that the proposed IT-type NPC inverter is superior in these areas.

Choi et al. [3], although it has a limited voltage gain, the conventional active neutral-point-clamped (ANPC) inverter has excellent high-frequency common mode voltage (CMV) mitigation capabilities. A novel five-level ANPC inverter that can boost voltage in a single-stage dc-ac power conversion is proposed in this letter. The dc-link voltage utilization is increased and the high-frequency CMV is reduced by a common ground in the proposed topology. When compared to a standard two-stage, five-level ANPC inverter, the proposed topology is more compact and has lower voltage stresses. In addition to improving overall efficiency, the proposed inverter conserves one capacitor and three power switches. The proposed ANPC inverter's overall operation, efficacy, and practicality have all been confirmed through experiments and simulations.

Zhang et al. [4], the hybrid utilization of Si/SiC converters is a different strategy for balancing cost and performance than full-SiC mosfet converters. An efficient strategy is proposed to create 2-SiC and 4-SiC mixture three-level dynamic unbiased point-clasped (3L-ANPC) inverter geographies from two kinds of exchanging cells in light of the plan of freewheeling ways. Switching states and modulation strategies for both the 2-SiC hybrid 3L-APNC inverter and the 4-SiC hybrid 3L-ANPC inverter are discussed in depth. The 2-SiC hybrid 3L-ANPC inverter and the 4-SiC hybrid 3L-ANPC inverter's power losses are quantitatively compared. The intersection working temperatures of dynamic switches in various cross breed 3L-ANPC inverters are additionally assessed. With similar determinations and exchanging gadget boundaries, the most extreme result force of the 4-SiC mixture 3L-ANPC inverter with tweak procedure I is practically 1.47 times than that of the 2-SiC half and half 3L-ANPC inverter. A widespread model for the full-SiC plot, the full-IGBT conspire, and different Si/SiC mixture plans is worked to assess these geographies at transformation effectiveness and warm qualities. Exploratory outcomes and investigation show that the full-SiC 3L-ANPC inverter has the most noteworthy effectiveness, though the 2-SiC half and half 3L-ANPC inverter has the best expense execution. Additionally, in high-power density applications, the 4-SiC hybrid 3L-ANPC inverter with modulation strategy I outperforms the 2-SiC hybrid 3L-ANPC inverter in terms of thermal balance.

M. J. Sathik et al. [5], in this short, another cross-associated minimized exchanged capacitor (C 3 SC) cell is presented for staggered inverter applications. The proposed CCS cell involves four switches and two diodes for interconnecting the info dc source and drifting capacitors (FCs). The proposed C 2 SC cell is used to create a nine-level inverter that only requires two FCs and ten switches. A two-voltage gain makes the proposed C 3 SC cell-based MLI self-balancing. The input dc voltage (v in) value is the maximum blocking voltage for each switch in the proposed topology. The working guideline is nitty gritty, and a straightforward rationale door based entryway beat age conspire is introduced. To validate the operation of the proposed topology, in-depth simulations and experimental results from an 850 W prototype with numerous test cases are presented. At last, an itemized near evaluation is performed with other ongoing SCMLIs to exhibit the benefits and predominance of the proposed geography.

J. Zeng et al. [6], a single-source, multilevel inverter (MLI) based on the novel K-type unit (KTU) was proposed in this article. This article describes the 13-level topology's operation modes at various output levels, which include two KTUs and 1.5 voltage gain. Due to their symmetric operation during a cycle, the two capacitors connected in series with each KTU can achieve self-voltage balance, reducing control complexity in comparison to conventional MLIs. Both the calculation of capacitance and the analysis of self-balance are described in detail. A short time later, the

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single-source summed up structure outfitted with more KTUs is introduced for expanding yield levels. With more KTUs, the voltage gain rises as well as the output levels rise significantly. Also, through the relative review against other MLI geographies proposed lately, the upsides of the proposed KTU geography are shown in the viewpoints for diminished parts, self-balance, voltage stress, and by and large expense. Last but not least, fundamental frequency modulation (FFM) is used to implement a 13-level simulation and a 1-kVA experimental prototype to test the proposed topology's transient performance.

N. Sandeep et al. [7], in recent times, multilevel inverters have been one of the most popular choices for medium-voltage and high-power applications. In the class of five-level (5L) inverters, the most common topology is the active neutral-point-clamped (ANPC) one. Based on improving the 5L ANPC inverter with the fewest modifications, a nine-level topology with improved output waveform quality is proposed in this study. The proposed modification is to maintain the same precursor part count while adding only two switches to the conventional 5L ANPC inverter that operate at line frequency. To keep the flying capacitor voltage at the reference value, a logic form equation-based active voltage balancing scheme that is independent of load current and power factor is developed. The developed control scheme, the operating principle, and the most important features are all described in detail. Using MATLAB/Simulink, the proposed inverter's operation in a grid-integrated scenario is simulated and its steady-state and dynamic results are presented. The advantages of the proposed geography are explained by contrasting it and other exemplary geographies thinking about different noticeable perspectives. The significant advantages and distinctive features of the proposed topology have been demonstrated through this comparison. The presentation approval, practicality, and practicability of the proposed inverter are laid out through the exploratory outcomes got from a research facility scale model.

A. Taghvaie et al. [8], a DC to AC converter with the capability of increasing voltage is presented in this paper. The design of this inverter makes use of only one dc source. Also, output voltage levels can be raised by using a power storage technique and connecting charged capacitors and a dc source in series. This inverter can self-balance capacitor voltages thanks to its modular design. At the end of the proposed converter, no H-bridge inverter was used, and all parts can handle voltage stress equal to the amount of dc input. Both the total standing voltage and the peak inverse voltage fall dramatically as a result. The proposed inverter's potential for high-frequency performance is another advantage. The particular type of the proposed inverter gives the possibility of expansion to higher voltage levels and facilitates the support. In addition, the proposed inverter's performance at high voltage is added to its characteristics due to the fact that all components' stress is the same as the input source. The proposed inverter's nine-level structure is simulated, and its performance is tested in a laboratory setting.

III. MULTI LEVEL INVERTER

Figure 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an ‘n’ level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [5, 6]:

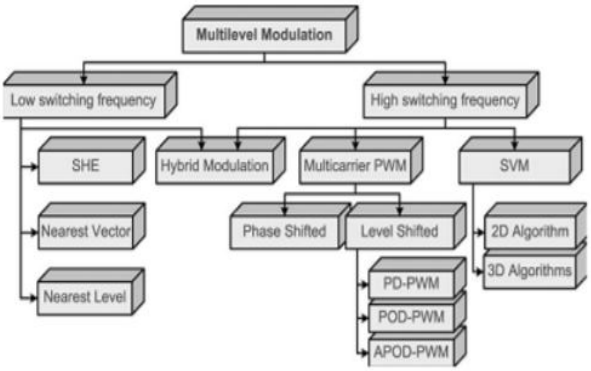

Figure 1: Multilevel converter modulation methods

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Level Shifted PWM (LSPWM)

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [7]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [8, 9]. Figure 2 shows the LS-PWM carrier arrangements.

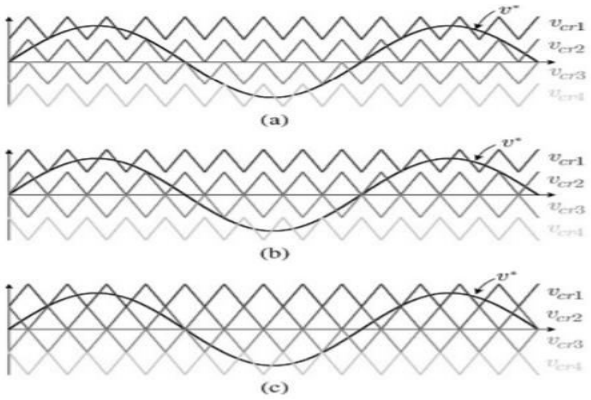

Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

Phase Shift Pulse Width Modulation

PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width [10]. There is one beat of settled extent in each PWM period. In any case, the width of the beats changes from period to period as indicated by a regulating signal. At the point when a PWM flag is connected to the entryway of a power transistor, it causes the turn on and kills interims of the transistor to change starting with one PWM period then onto the next PWM period as indicated by the same regulating signal and thus working of converter begins. The recurrence of a PWM flag must be substantially higher than that of the regulating signal, the major recurrence, with the end goal that the vitality conveyed to the heap depends generally on the tweaking signal. The control of yield voltage is done utilizing beat width balance [11, 12].

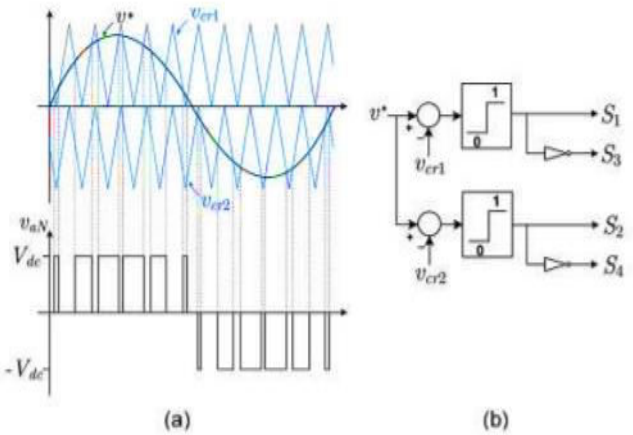

Figure 3: Phase Shift PWM

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by 90^{o}. Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal [13].

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Total Harmonic Distortion

The total harmonic distortion (THD or THDi) is a measurement of the harmonic distortion present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Distortion factor, a closely related term, is sometimes used as a synonym.

In audio systems, lower distortion means the components in a loudspeaker, amplifier or microphone or other equipment produce a more accurate reproduction of an audio recording.

In radio communications, devices with lower THD tend to produce less unintentional interference with other electronic devices. Since harmonic distortion tends to widen the frequency spectrum of the output emissions from a device by adding signals at multiples of the input frequency, devices with high THD are less suitable in applications such as spectrum sharing and spectrum sensing [14, 15].

In power systems, lower THD implies lower peak currents, less heating, lower electromagnetic emissions, and less core loss in motors.

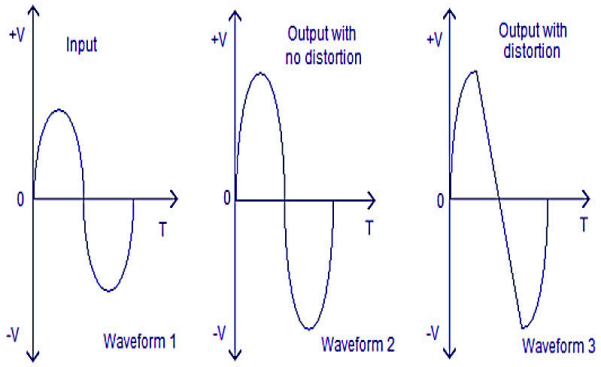

Figure 4: Output Waveform of Distortion

The advantages of using multi-level inverters over classic inverters will now be highlighted. Several advantages are associated with multi-level inverters, as high switching frequency pulse width modulation (PWM) is used by traditional converters (two-level). The utmost apparent characteristics of multi-level inverters are summed up below.

- Quality of staircase waveform: Apart from generating output voltages with negligible distortion, multi-level inverters also decrease the dv/dt stresses, thereby resulting in the reduction of electromagnetic compatibility (EMC) issues.
- Common mode (CM) voltage: The motor bearings stress, linked to a multi-level motor drive, could be decreased because smaller common mode voltage is generated by multi-level inverters. Moreover, advanced strategies of modulation, such as the one suggested in (Choi et al. 1991), can be employed in the termination of the CM voltage.
- Input current: The input current with a negligible distortion can be drawn by multilevel inverters.
- Frequency of switching: The functioning of multilevel inverters is possible at rudimentary switching frequency as well as high switching frequency (PWM). It is imperative to bear in mind that higher efficiency and lower switching loss can be derived from lower switching frequency.

There are certain disadvantages associated with multilevel inverters. The need of a large quantity of power semiconductor switches is a prominent shortcoming. An associated gate drive circuit is required by each switch despite the latent utilization of low voltage rated switches in multilevel inverters, consequently resulting in the increase of complicatedness and costs of the system. It is important to observe that the advantages of multilevel inverters outweigh the disadvantages, rendering them a definitive edge over conventional inverters.

IV. CONCLUSION

The presented research work has been focused on the construction of variable amplitude sinusoidal voltage using the different topologies. The first effort has been related to the development of new MLI topology using diodes and switching devices under symmetric and asymmetric mode. The advantage of the topology articulates any desired voltage level with a reduced total number of devices and sources over basic and similar topology. With the advancement and development of various industries and sectors at international as well as domestic levels, demands for high energy converters are continuously increasing. It can be said that the multilevel inverters are continued to gain

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popularity and importance for the applications of low as well as high power. This paper has presented and discussed eight categories of multilevel inverter topologies. Based on the review, conclusion can be done in the process of reducing the power switch count of multilevel inverters, is either by reducing or re-arranging the DC input voltages. Other than that, particular topological explanations and resolutions have been provided by various researchers considering the intended use of application.

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