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# Efficient VLSI Implementation of Linear Convolution using Baugh Wooley and KS Adder

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**ABSTRACT**- Of late all the organization of world are approaching the high speed processor towards the fast digital communication. In this paper we are going to propose a method to develop fast convolution technique. Convolution is the bottleneck technique for digital signal processing, image processing and other signal analysis. Proposing convolution method is comprised with multiplier and adder. With this concern we need to design a fast multiplier and adder which are also main components of processor design. In this paper, implementation of linear convolution using Baugh Wooley and KS adder is present. The Baugh Wooley multiplier is the sign multiplier and Kogge Stone adder (KSA) is the efficient adder. The implement linear convolution is simulated Xilinx software and calculated number of slice, look up table and delay.

**KEYWORDS**- Linear Convolution, Baugh Wooley, Kogge Stone Adder

## I. INTRODUCTION

With the advent of new generation of the digital devices speed of the processor must be high. Processor's speed can be enhanced by the aid of high speed multiplication and addition of the binary bits. With the latest advanced of VLSI technology we always keep in mind to increase the speed and reduce the area as possible as. Convolution and de-convolution techniques play an important role in digital signal processing and image processing. Convolution is a mathematical way of combining two signals to form a third signal. on the other hand convolution is the process to the calculate the output signal for given input signal by using impulse response signal. Convolution is basically used in digital filter and correlation applications. Convolution can be classified as linear, circular convolution and graphical convolution.

Graphical method is the best way to represent the convolve of two signals but it is the tedious method, so generally we use linear and circular technique in digital signal processing. Computation of convolution depends on multiplier and adder devices. So in this paper we are using Vedic multiplier which is based on Urdhva Triyagbhayanm Sutra and Kogge Stone high speed adder instead of traditional devices. Multiplication can be done by shifting and adding method but it gives high propagation delay. Another method is Wallace tree algorithm but it is not better than Kogge Stone adder regarding the less area.

$$y(n) = f(n) * g(n) \tag{1}$$

In above equation f(n) and g(n) are finite length sequence.

$$y(n) = \sum_{n=-\infty}^{+\infty} [f(k) * g(n-k)] \tag{2}$$

Linear Convolution can be calculated by using above equations. But this is lengthy process. This can be solved by several methods so cross multiplication is best method one of them.

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## II. APPROACHING HIGH SPEED CONVOLUTION METHOD

### A. Linear Convolution

Convolution of two discrete finite length signals can be calculated by several techniques and cross multiplication is one of them. By using Vedic mathematics typical calculation can be reduced with less time consuming [2]. Let us assume that f(n) is a finite length sequence of ($A_3$,$A_2$,$A_1$,$A_0$) and another finite length sequence is g(n) with variables ($B_3$,$B_2$,$B_1$,$B_0$) then output will be y(n) with finite length sequence ($Y_6$,$Y_5$,$Y_4$,$Y_3$,$Y_2$,$Y_1$,$Y_0$). For instance Input sequences are A(7,7,7,7) and B(7,7,7,7) then linear convolution output will be (49,98,147,196,147,98,49).

$$
\begin{aligned}
Y_0 &= A_0 * B_0 \\
Y_1 &= A_1 * B_0 + A_0 * B_1 \\
Y_2 &= A_2 * B_0 + A_1 * B_1 + A_0 * B_2 \\
Y_3 &= A_0 * B_3 + A_1 * B_2 + A_2 * B_1 + A_3 * B_0 \\
Y_4 &= A_1 * B_3 + A_2 * B_2 + A_3 * B_1 \\
Y_5 &= A_2 * B_3 + A_3 * B_2 \\
Y_6 &= A_3 * B_3
\end{aligned}
\tag{3}
$$

In these equations all the calculation of multiplication will be done by Urdhva Triyagbhayam technique and addition will be performed by Kogge Stone Adder. With the aid of this technique we can reduce the number of gates and area, as soon as numbers of slices are decreased, propagation delay or route delay automatically reduced [3].

Figure 1 shows, the fast linear convolution by using cross multiplication, here elements of each diagonal line are added together individually. Here bits of A group are putted in vertically way and bits of B group are putted in horizontal way. Now $A_0$ is multiplied with $B_0$ in partial product manner that is also called ANDing Operation. After this partial product $A_0$ is multiplied with other remaining bits such as $B_1$, $B_2$ and $B_3$.

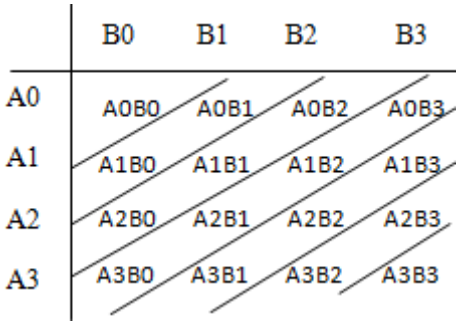


Figure 2: A matrix fast Linear Convolution by using cross Multiplication

Likewise $A_1$ is multiplied with $B_0$ in partial manner. $A_1$ is multiplied with $B_1$ and $B_0$. In the same manner other bit will be multiplied with remaining bits. The output will be found by adding of these partial products. Diagonally lines show the addition of the individual outputs. Eventually, convolution of the 4 bit provides the output of the 7 bit. This convolution method can be enhanced for 5, 6 and other bit sequences.

### B. Circular Convolution

Circular convolution is the most frequently used in filtering the noise and blurred signal in digital signal processing and image signal processing. Circular convolution has many applications and is usually applicable to electrical engineering students in a digital signal processing. A Vedic mathematics multiplication is a novel method for computing the circular convolution [4]. Circular convolution can be obtained by using the shifting and folding technique but it gives complex solution. So in paper we are using Vedic multiplication and CBL adder to compute the circular convolution sequence. Let us assume that f(n) and g(n) are finite length sequence then output of circular convolution y(n) is

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$$y(n) = f(n) * g(n) \tag{4}$$

$$y(n) = \sum_{n=0}^{N-1} [f(k)g(n-k)(ModN)] \tag{5}$$

Where, N is the length of the sequences. for instance one finite length sequence is ($A_3$,$A_2$,$A_1$,$A_0$) and another sequence is ($B_3$,$B_2$,$B_1$,$B_0$) then output sequence for circular convolution is ($Y_3$,$Y_2$,$Y_1$,$Y_0$)

$$\begin{aligned} Y_0 &= A_0 * B_0 + A_3 * B_1 + A_2 * B_2 + A_1 * B_3 \\ Y_1 &= A_1 * B_0 + A_0 * B_1 + A_3 * B_2 + A_2 * B_3 \\ Y_2 &= A_2 * B_0 + A_1 * B_1 + A_0 * B_2 + A_3 * B_3 \\ Y_3 &= A_3 * B_0 + A_2 * B_1 + A_1 * B_2 + A_0 * B_3 \end{aligned} \tag{6}$$

In circular convolution no carry out will be propagated to other equations.

## III. LOGICAL DESIGNING APPROACH OF HIGH SPEED LINEAR CONVOLUTION

Complex logical designing can be reduced by the Vedic mathematics calculation which is consisting with 16 sutras. Number of fan in, fan out pin and input output buffers can be minimized. For the high speed convolution, multiplier and adder must be high efficient and low area as possible as. For instance ($A_3$, $A_2$, $A_1$, $A_0$) and ($B_3$, $B_2$, $B_1$, $B_0$) are the finite length sequence. In the linear convolution total number of Vedic multiplier will be 16 for 4 bit multiplication. Each Vedic multiplier produces 8 bit output summation bits. So we need 8 bit adder for adding the two 8 bit sequence which is performed by low propagation delay CBL adder [6].

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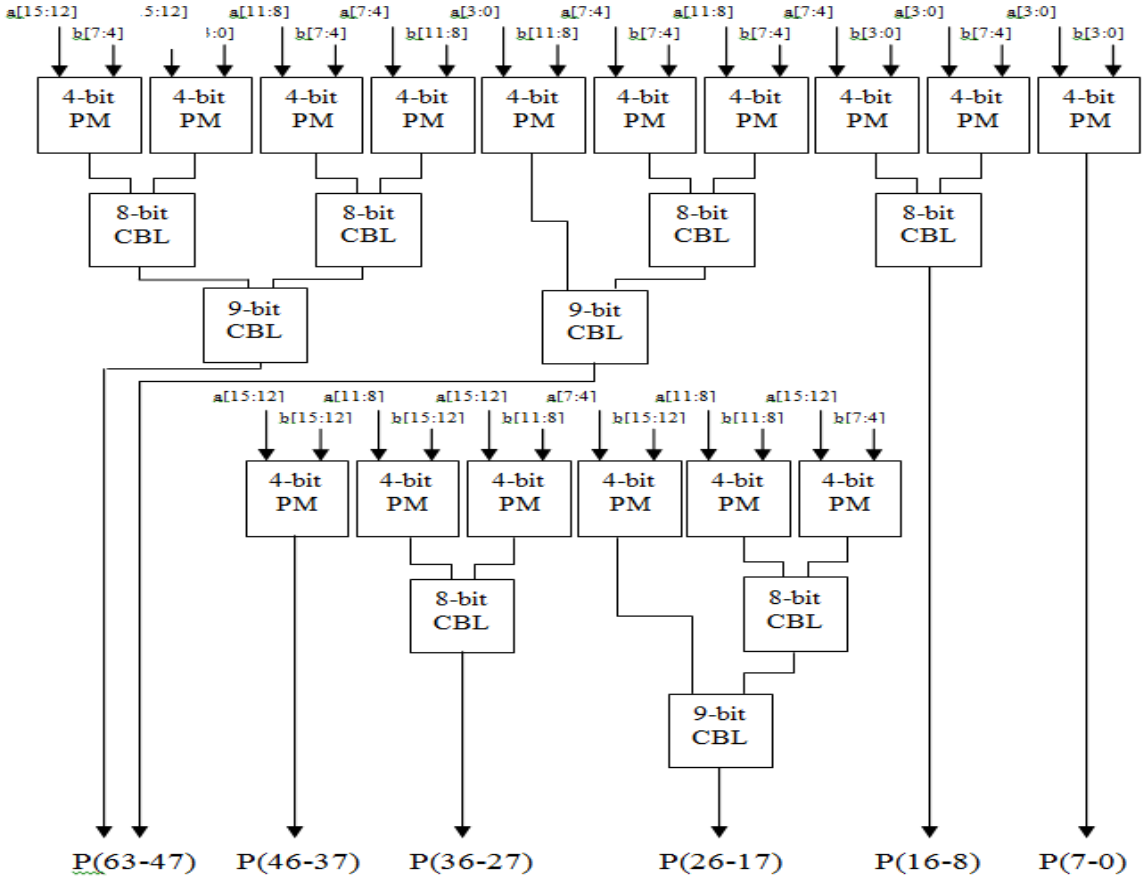


Figure 3: A 4 bit High Speed Linear Convolution

8 bit CBL Adder produces the 9 bit output. These bits are added by 9 bit CBL Adder which produces 10 bit output bit sequence. Hence total number of output bit for 4 bit high speed liner convolution is 64 uses the 4 bit Vedic multiplier, 8 and 9 bit CBL adder. Multiplication of convolution input sequence is different from ordinary binary multiplication [5]. In the multiplication of convolution input sequence no carry forwarded to next bit or addition will be performed individually. With other instance this technique can be made understand easy. If input sequence of convolution are (15, 15, 15, 15) and (15, 15, 15, 15) then output sequence will be (225, 450, 675, 900, 675, 450, 225). Here we are using 4 high bit for 4 input sequence so total number of bit for A input sequence are 16, like for B input sequence. Figure 3 shows the 4bit high efficient linear convolution logic design. In this figure number of inputs are 16. And first 4 bits are multiplied by using the 4 bit high speed Vedic multiplier which is abbreviated by VM. The output of the first Vedic multiplier gives the 8bit output that is the first 8 bit output of the linear convolution. Now the next 4 bit Vedic multiplier multiplies the different 4 bit inputs and outputs are connected to the 8 bit adder. This is special high speed CBL adder which provides the low combinational delay with less area. Third multiplier multiplies the 4 bit of a[7:3] and b[3:0] and this multiplies gives the 8 bit outputs. These output bits are connected to the 8 bit CBL added. So output bits of the second Vedic multiplier and output bits of third Vedic multiplier are connected to inputs of the 8 bit KSA. This adder provides the 9 bit output of the linear convolution and sequence would be P [16:8]. Same as previous step the output bits of the fourth and fifth Vedic multiplier are added by 8 bit CBL. And output bits of the 8 bit CBL are connected to the 9 bit CBL added. The CBL adder has one special property is that its propagation delay does not depend on the increased logic circuit. So propagation delay of the 8, 9, 10 and other than this are having same propagation delay. Vedic multiplier of the sixth number provides the 8 bit output and these bits are connected to the 9 bit CBL.

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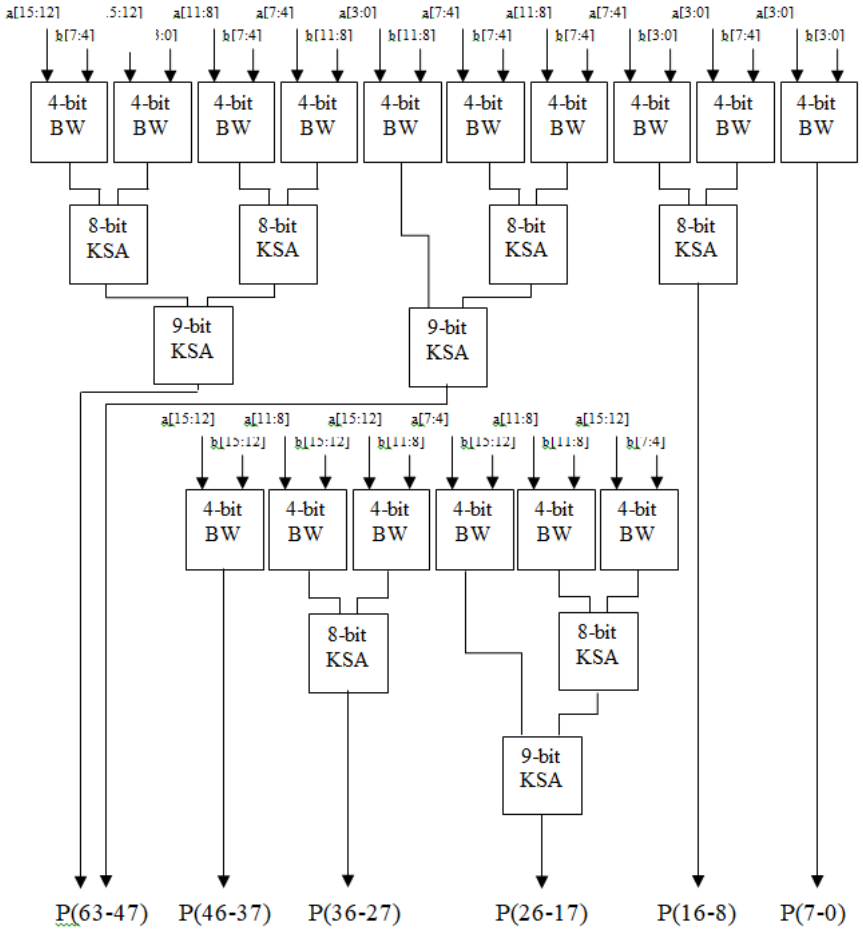


Figure 4: 4-bit High Linear Convolution using Baugh Wooley Multiplier and KS Adder

## IV. EXPERIMENT SETUP

All the experiment analysis is done by 14.2i Spartan 3 series Xilinx tool. This tool provides less propagation delay than to 6.2i and 9.2i Xilinx tool. The most important advantage of this tool is less memory with high speed analysis any complex logical circuit. Simulation and synthesize of convolution logical circuit can be enhanced by Xilinx design suit 14.2i Spartan 3 series and device XC3S400-5fg320.

Table 1: Comparison between Conventional adder and proposed adder

| 7 i/p Sequence | | | | |
|---|---|---|---|---|
| | Slices | LUTs | IOBs | MCPD |
| Sign multiplier with parallel adder | 276 out of 768 | 498 out of 1536 | 76 out of 124 | 6.076 ns |
| Sign multiplier with conventional adder | 234 out of 768 | 408 out of 1536 | 76 out of 124 | 4.998 ns |
| Proposed Baugh Wooley and KS Adder | 222 out of 768 | 296 out of 1536 | 76 out of 124 | 4.632 ns |

Table III, shows the comparison of the conventional and modified high speed convolution technique. The parameters are input, output sequence, slices, input output buffers, and look up table and propagation delay that is also called combinational path delay. According to this table input sequence is [3:0] that is 4 bit sequences.

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Table II: Comparison between Conventional adder and proposed adder

| 9 i/p Sequence | | | | |
|---|---|---|---|---|
| | Slices | LUTs | IOBs | MCPD |
| Sign multiplier with parallel adder | 438 out of 768 | 578 out of 1536 | 125 out of 124 | 6.789 ns |
| Sign multiplier with conventional adder | 388 out of 768 | 484 out of 1536 | 100 out of 124 | 5.356 ns |
| Proposed Baugh Wooley and KS Adder | 276 out of 768 | 322 out of 1536 | 100 out of 124 | 4.783 ns |

Table III: Comparison between previous algorithm and proposed algorithm

| **Parameter** | **Conventional method** | **Proposed method** |
|---|---|---|
| Elements used | Array Multiplier, HA and FA | Baugh Wooley and KS Adder |
| No of slices | - | 393 |
| No of IO Buffers | - | 100 |
| No of LUTs | 380 | 322 |
| Propagation Delay | 5.041 ns | 4.783 ns |

Number of slices of the conventional method is less than to modified convolution technique. Number of the input, outputs buffers is having same value for both. The main motive of this paper is to reduce the propagation delay. Propagation delay is an essential parameter to design the high speed convolution technique.

## V. CONCLUSION

Eventually, in this paper we have structured a fast linear convolution circuit which is based on Baugh Wooley multiplier and KSA adder. The path delay time and area of the proposed technique for convolution using Baugh Wooley algorithm is compared with that of convolution with simple multiplication is less. Designed high speed convolution technique can use for designing the filter to filter the blurred signal [8]. This can be used for image processing and digital signal processing technique. By using high speed multiplier ALU, GPU and CPU can be designed.

## REFRENCES

[1] Rahul Kamdi, Prasheel Thakre, Aniket Pathade and Sandeep Kumar Tiwari, “4 Bit and 8 Bit Convolution Using Vedic Multiplier”, International Conference on Emerging Trends in Engineering and Medical Sciences (ICETEMS), IEEE 2022.

[2] Rahul P. Kamdi, Sandip Kumar Tiwari, Aniket Pathode, “Design & implementation of fine ADC block in 8-b folding and interpolation”, Second International Conference on Artificial Intelligence and Smart Energy (ICAIS), IEEE 2022.

[3] Yongxiang Cao, Wan’ang Xiao, Jingdun Jia, Dehua Wu and Weixin Zhou, “Cordic-based Softmax Acceleration Method of Convolution Neural Network on FPGA”, International Conference on Artificial Intelligence and Information Systems (ICAIIS), IEEE 2020.

[4] Shubhi Shrivastava and Paresh Rawat, “High Speed and Delay Efficient Convolution by using Kogge Stone Device”, International Conference on Computer Communication and Informatics (ICCCI), IEEE 2017.

[5] I. Vinay B. Biradar, P. G. Vishwas, C. S. Chetan and B. S. Premananda, “Design and performance analysis of modified unsigned braun and signed Baugh-Wooley multiplier”, International Conference on Electrical, Electronics, Communication, Computer, and Optimization Techniques (ICEECCOT), IEEE 2017.

[6] AlaaEddin Loulou, Juha Yli-Kaakinen and Markku Renfors, “Efficient fast-convolution based implementation of 5G waveform processing using circular convolution decomposition”, IEEE International Conference on Communications (ICC), IEEE 2017.

[7] B. Shweta S. Tejal S. Kiran and G. Kamde Archana "Implementation of Modified Baugh Wooley Signed Multiplier" International Journal of Innovative Research in Computer and Communication Engineering (IJIRCCE) vol. 5 no. 2 pp. 2317-2321 Feb. 2017.

[8] Aiman Badawi, Ali Alqarni, Abdullah Aljuffri and Mohammed S. BenSaleh, “FPGA realization and performance evaluation of fixed-width modified Baugh-Wooley multiplier”, Third International Conference on Technological Advances in Electrical, Electronics and Computer Engineering (TAEECE), IEEE 2015.

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[9] K. Shao J. Alhava J. Yli-Kaakinen and M. Renfors "Fast-convolution implementation of filter bank multicarrier waveform processing" Proc. IEEE Int. Symp. on Circuits and Systems (IS CAS pp. 978-981 May 2015.

[10] M. Renfors J. Yli-Kaakinen T. Levanen M. Valkama T. Ihalainen and J. Vihriala "Efficient fast-convolution implementation of filtered CP-OFDM waveform processing for 5G" Proc. IEEE Globecom Workshops (GC Wkshps) pp. 1-7 Dec 2015.

[11] Pramod S. Aswale Mukesh P. Mahajan Manjul V. Nikumbh and Omkar S. Vaidya "Implementation of Baugh-Wooley Multiplier and Modified Baugh Wooely Multiplier using Cadence (Encounter) RTL" International Journal of Science Engineering and Technology Research (IJSETR) vol. 4 no. 2 pp. 293-298 Feb. 2015.

[12] C.S. Chetan Vinay B. Biradar P.G. Vishwas and B.S. Premananda "Performance Enhancement of 32-bit Carry Select Adder by Employing RTL Optimization Techniques" International Research Journal of Engineering and Technology IRJET vol. 2 no. 3 pp. 2273-2277 June 2015.

[13] Surabhi Jain and Sandeep Saini, "High Speed Convolution and Deconvolution algorithm (Based on Ancient Indian Vedic Mathematics)", 11th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), IEEE 2014.

[14] M. Renfors J. Yli-Kaakinen and F. J. Harris "Analysis and design of efficient and flexible fast-convolution based multirate filter banks" IEEE Transactions on Signal Processing vol. 62 no. 15 pp. 3768-3783 Aug 2014.

[15] B.S. Premananda Samarth S. Pai B. Shashank and Shashank S. Bhat "Design of Area and Power Efficient Complex Number Multiplier" Proceedings of Fifth IEEE International Conference on Computing Communication and Networking Technologies (ICCCNT) pp. 1-5 July 2014.

[16] Vivek V. Babu and S. Mary Vijaya Lense "Delay Optimized 16-Bit Twin Precision Baugh Wooley Multiplier" International Journal of Emerging Technology and Advanced Engineering (IJETAE) vol. 4 no. 3 pp. 90-95 March 2014.

[17] A. Jipsa and P. Jyotirmoy "Design and Implementation of High Speed Baugh Wooley and modified Booth Multiplier using Cadence RTL" International Journal of Research in Engineering and Technology (IJRET) vol. 3 no. 8 pp. 56-63 August 2014.

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