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Area Decreased With Compact Size Multiplier by Using Common Boolean Logic with Low Power Dissipation

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ABSTRACT: Nowadays multiplier plays an vital role in today's digital signal processing and other high performance system. With the help of multiplier nowadays various high speed, low power and compact system of VLSI implementation can be made. The conventional multiplier there is the reduction of delay, but the proposed multiplier will reduce the delay in each and every gate. By using the common Boolean logic, we can reduce the area,delay,power of the multiplier. And hence we can reduce the delay,area,power of each and every gates.

KEYWORDS: Digital signal processing, common Boolean Logic, conventional multiplier.

I.INTRODUCTION

The process of creating integrated circuits is by combining thousands of transistors into a single chip in the VLSI .there are many challenges in VLSI circuit which must be developed to make the VLSI in efficient manner. With the advances in the technology and also in the electronics, many researchers have tried and are trying for the various designs of multipliers which will offer for various targets such as high speed, low power consumption, regularity of layout, less area.

The multiplication method is mainly based on Add and Shift algorithm. The performance of the multiplier which determines the main parameter is that adding the number of partial products in the parallel multiplier. To reduce the partial products the modified booth algorithm is one of the most popular algorithms. Then Wallace tree multiplier reduces the sequential adding stages. However the no of shifts between the partial products and the intermediate sums to be added will increase which may result in reduced speed by increasing the parallelism in multiplier.

II.EXISTING SYSTEM

The CSLA partitions the adder into several groups, each of which performs two addition operations parallel. So two copies of ripple carry adder act as carry evaluation per block to select stage. One copy evaluates the carry chain assuming the block carry is zero, While another to be one. Once the carry signals are finally computed the desired sum and the carry will be simply select from the multiplex

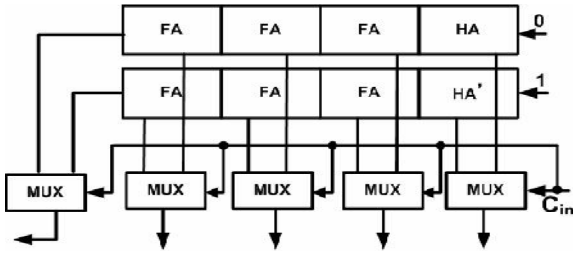

Fig 1. Conventional adder system with two carry inputs

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The carry generation of ripple carry generation is done in four stages

1. Half sum generation (HSG)
2. Half carry generation(HCG)
3. Full sum generation(FSG)
4. Full carry generation(FCG)

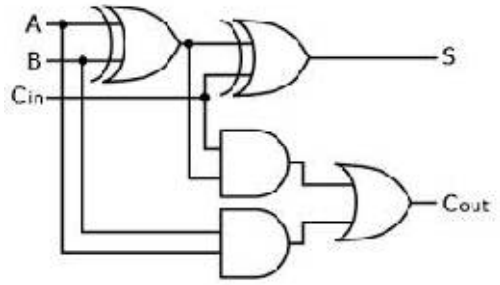

Fig 2.Full adder circuit

the circuit evaluation is done by total no of gates in the circuit and hence the circuit of multiplexer is given by,

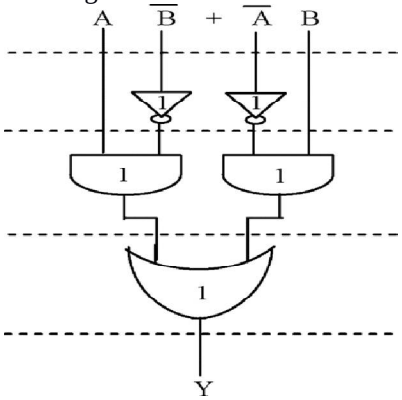

Fig 3.Circuit diagram of 2:1 multiplexer

The conventional multiplier does the operation of multiplication. The conventional system circuit consists of 8 full adder and 4 half adder.CSLA is not efficient because of using the multiple pairs of ripple carry adders. To generate the partial sum and carry by considering the carry inputs cin=0 and cin=1,then the final sum and the carry is selected by the multiplexer.

The four bit conventional CSLA is taken to achieve the low power ,low area and high speed with the slightly increase in the delay. The basic idea of the proposed system is to replace the full adder in the conventional multiplier by using the common Boolean logic algorithm. Here the four bit conventional multiplier diagram is shown below

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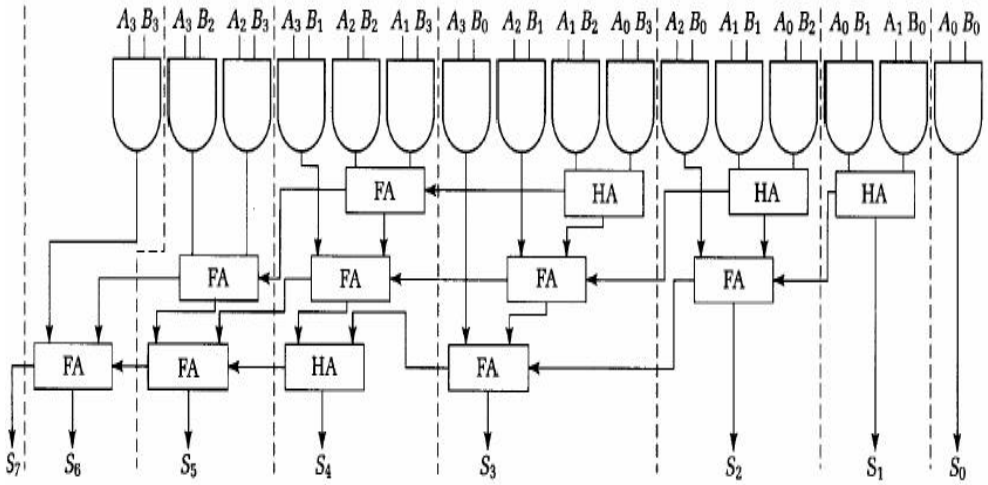

Fig 4. Conventional adder structure

Here the inputs are given as A0,A1,A2,A3,B0,B1,B2,B3.The desired partial products are mentioned as S0,S1,S2,S3,S4,S5,S6,S7.FA is the full adders in the circuit .HA is the half adder in the circuit. We are going to replace the full adders by using the common Boolean logic.

III.PROPOSED SYSTEM

The delay of the circuit is reduced initially by replacing the full adders in the conventional CSLA and hence the process is more efficient by the replacement. To overcome this problem we introduce CBL in proposed methodology;

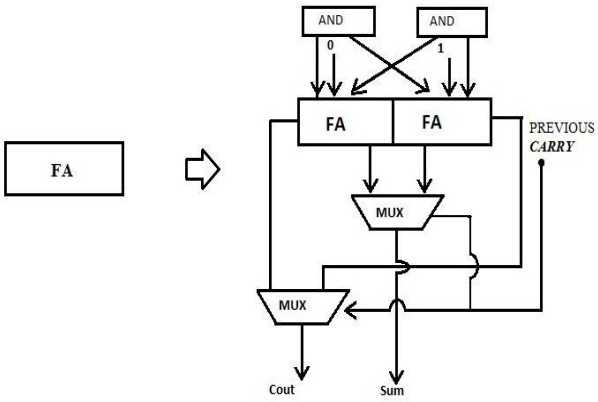

Fig 5.Replacement of full adder

Using this replacement the propagation delay is reduced but the size of the circuit and power dissipation is increased. to reduce this disadvantage ,an efficient carry select multiplier should be made by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder so the transistor counts is reduced and achieve low power.

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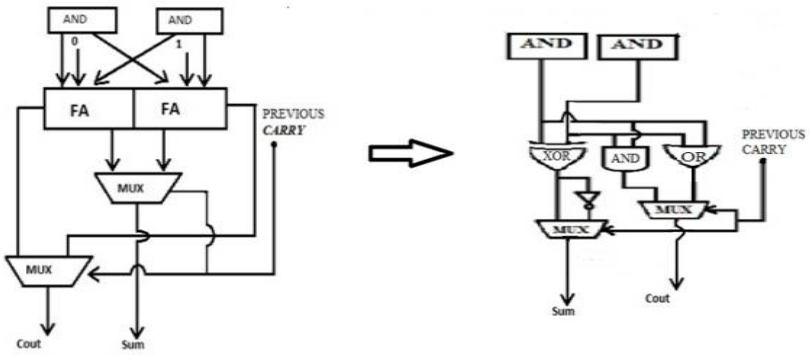

Fig 6. Replacement of conventional full adder with proposed full adder

By analysing the truth table of a single bit full adder the output of summation signal as carry –in signal is logic ¨0¨is the inverse of itself as carry-in signal is logic¨1¨.to share the common Boolean logic term it only needs to implement one OR gate with one INVERTER gate to generate the carry signal and summation signal pair. The truth table and the circuit of proposed system is given below

TABLE 1.Truth table of Carry select adder.

Cin (Carry In)	A	B	S0 (Sum Out)	C0 (Carry Out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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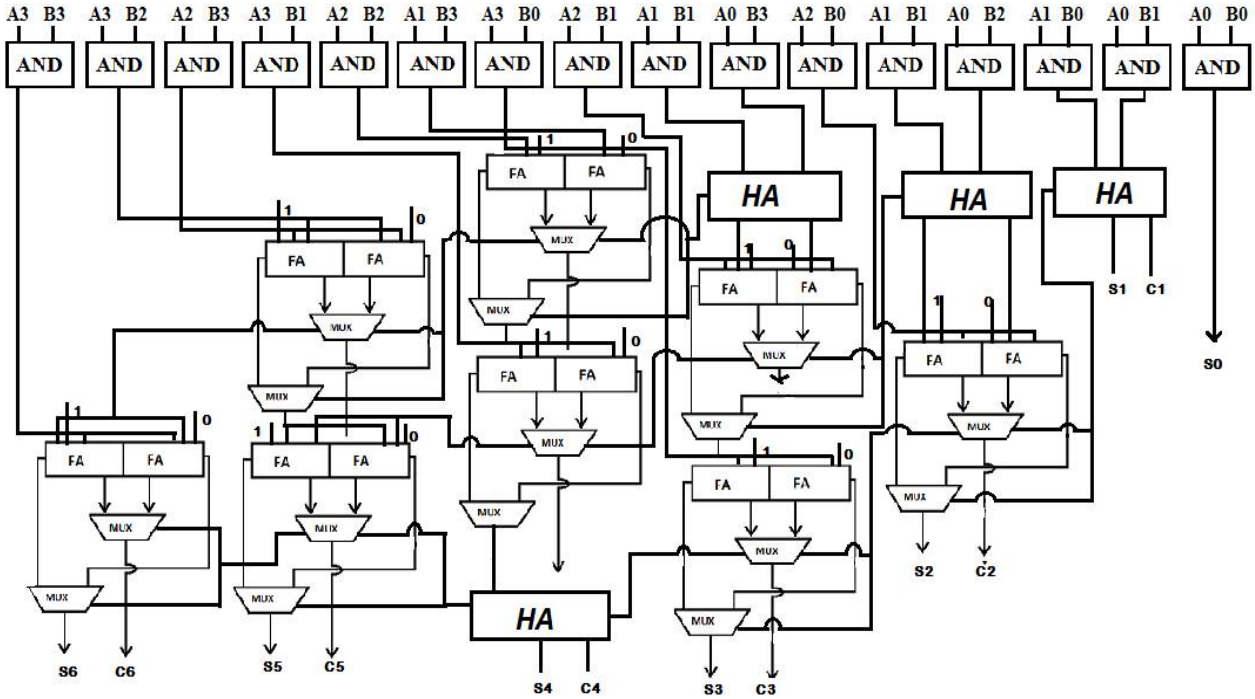
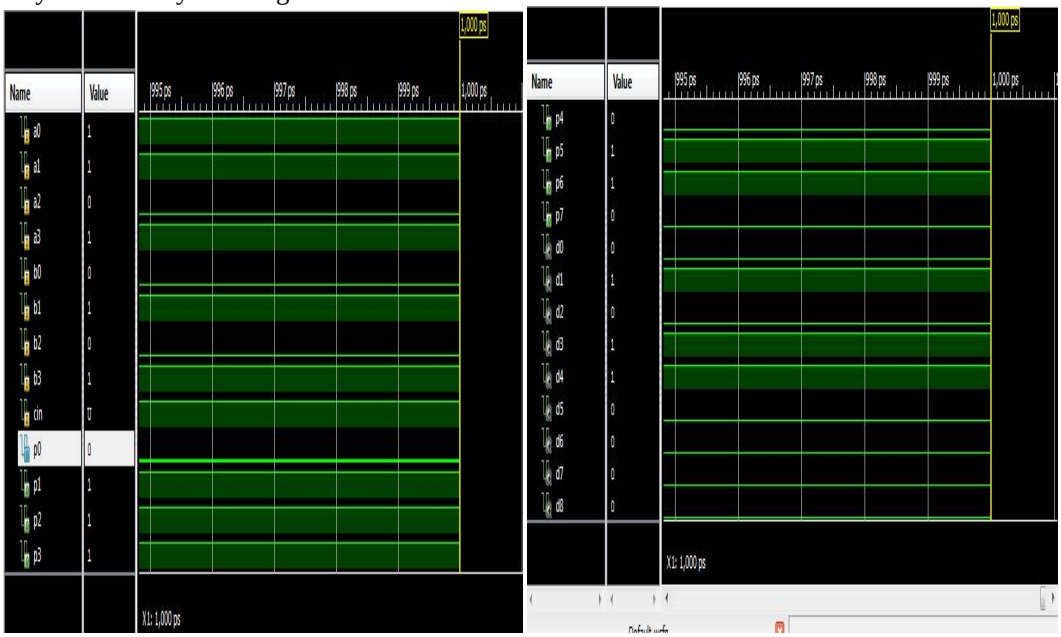


Fig 7. Proposed multiplier

IV. SIMULATION AND RESULTS

The circuit were simulated by using XILINX ISE design suit 12.1 and it is implemented in VHDL design language and microwind for power dissipation. Depends upon the total number of gate in the circuit the total area consumed can be calculated. Hence by reducing the gates the area consumed is minimised .so the computational speed is considerably increased by reducing the area in the circuit.



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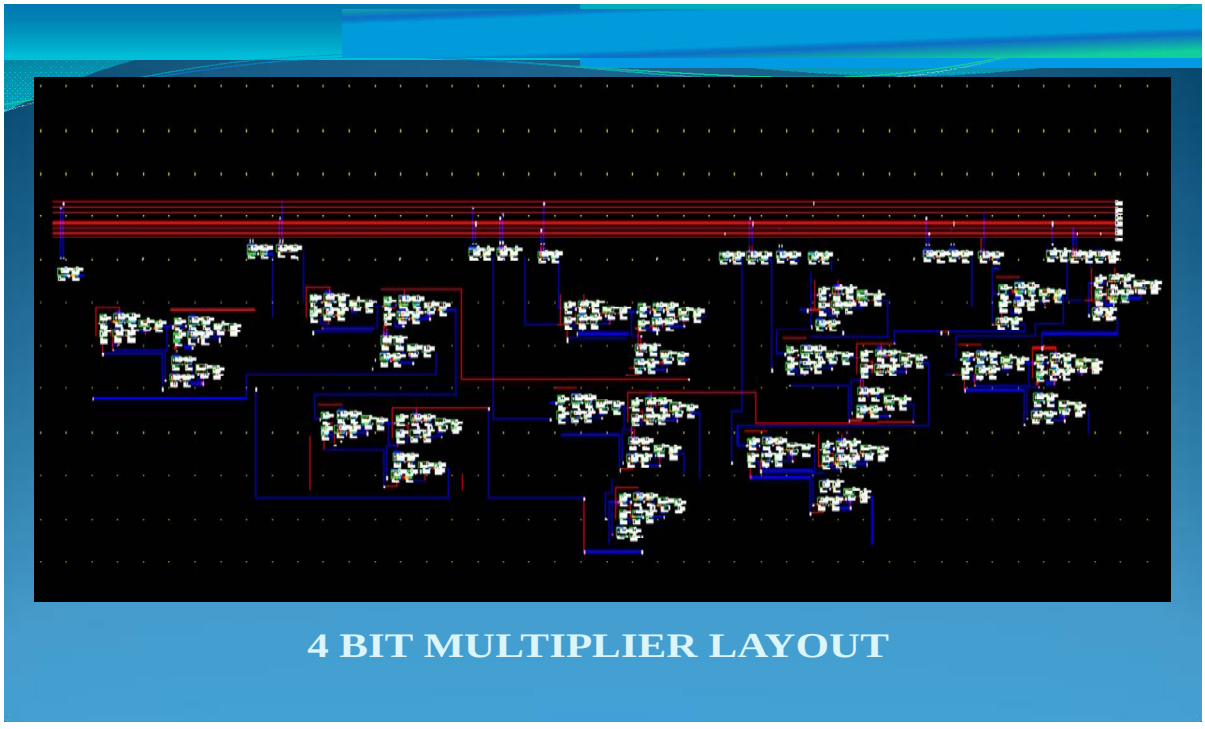
Output by using microwind to find the power dissipation of the circuit is shown below .The following diagram represents the four bit conventional multiplier and the proposed system by using common Boolean logic by using the microwind.



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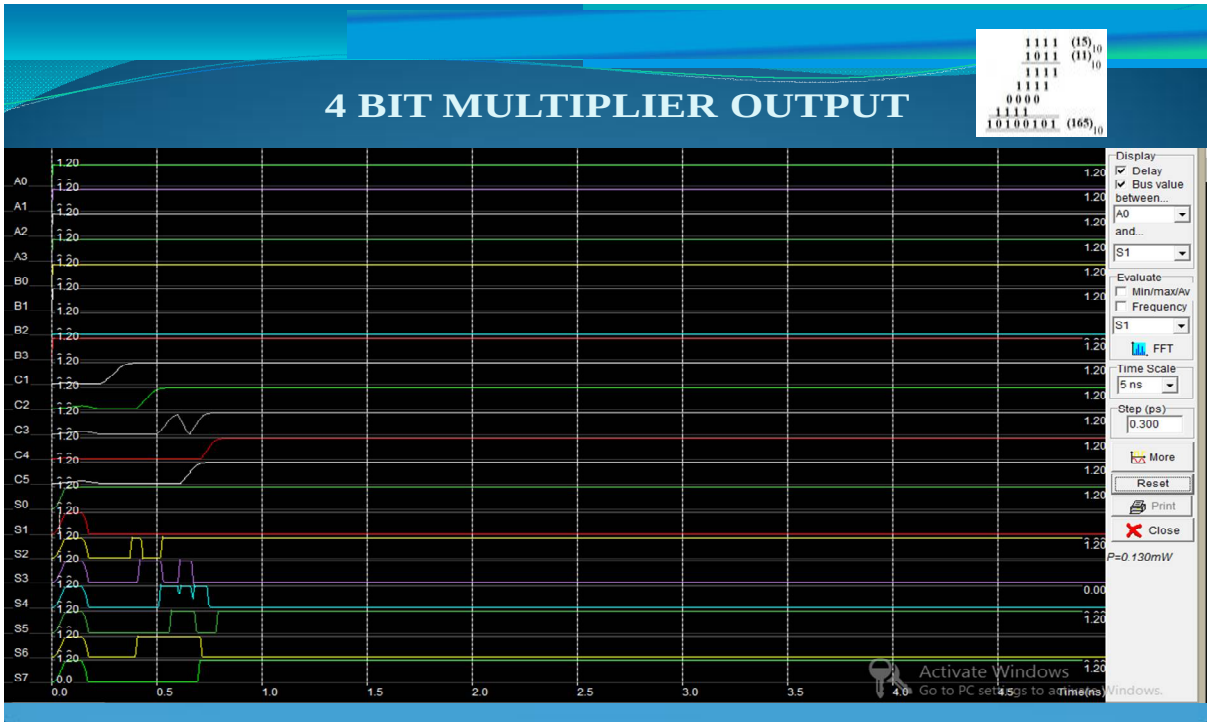

OUTPUT COMPARISON BETWEEN MULTIPLIERS

FACTORS	4 BIT MULTIPLIER	4 BIT CONVENTIONAL MULTIPLIER	4 BIT PROPOSED MULTIPLIER
AND GATE NOT GATE XOR GATE OR GATE HALF ADDER FULL ADDER MULTIPLEXER	16 00 00 00 04 08 00	16 00 00 00 04 16 16	24 08 08 08 04 00 16
NO. OF GATES REQUIRED (TOTAL AREA)	(16*1)+(4*6)+(8*13) =144	(16*1)+(4*6)+(16*13)+(16*4) = 312	(24*1)+(8*1)+(8*5)+(8*1)+(4*6)+(16*4) =168
POWER DISSIPATION	0.130 mW	0.295 mW	0.155mW

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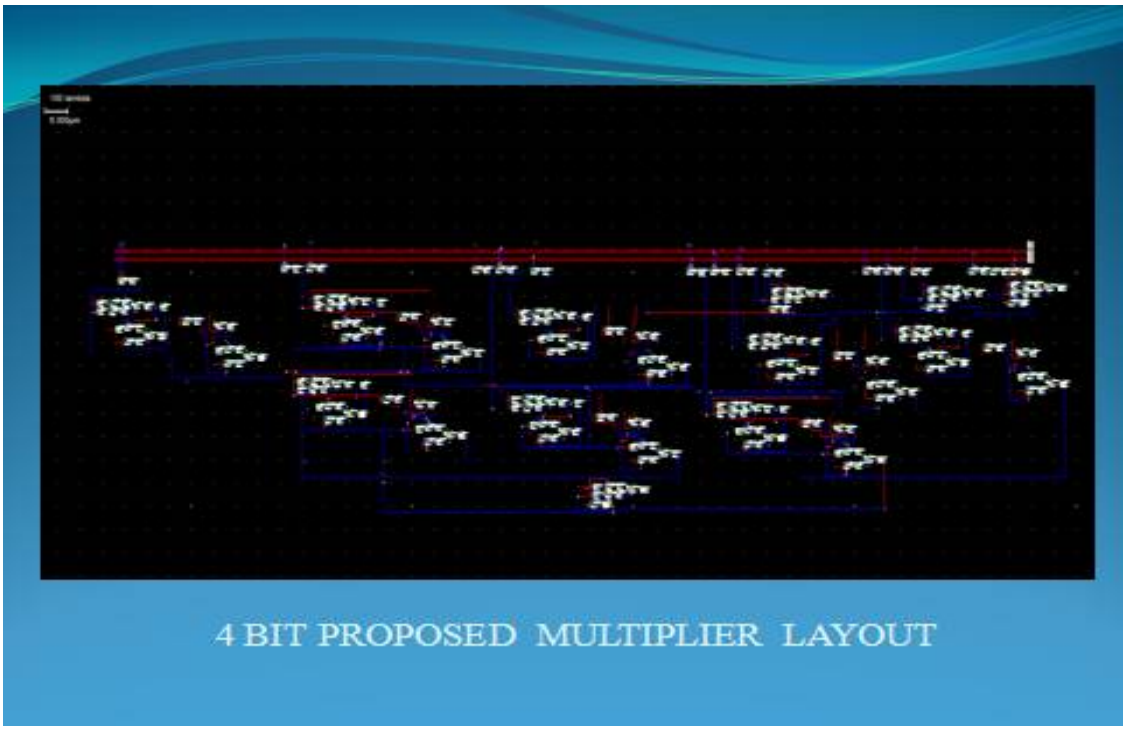

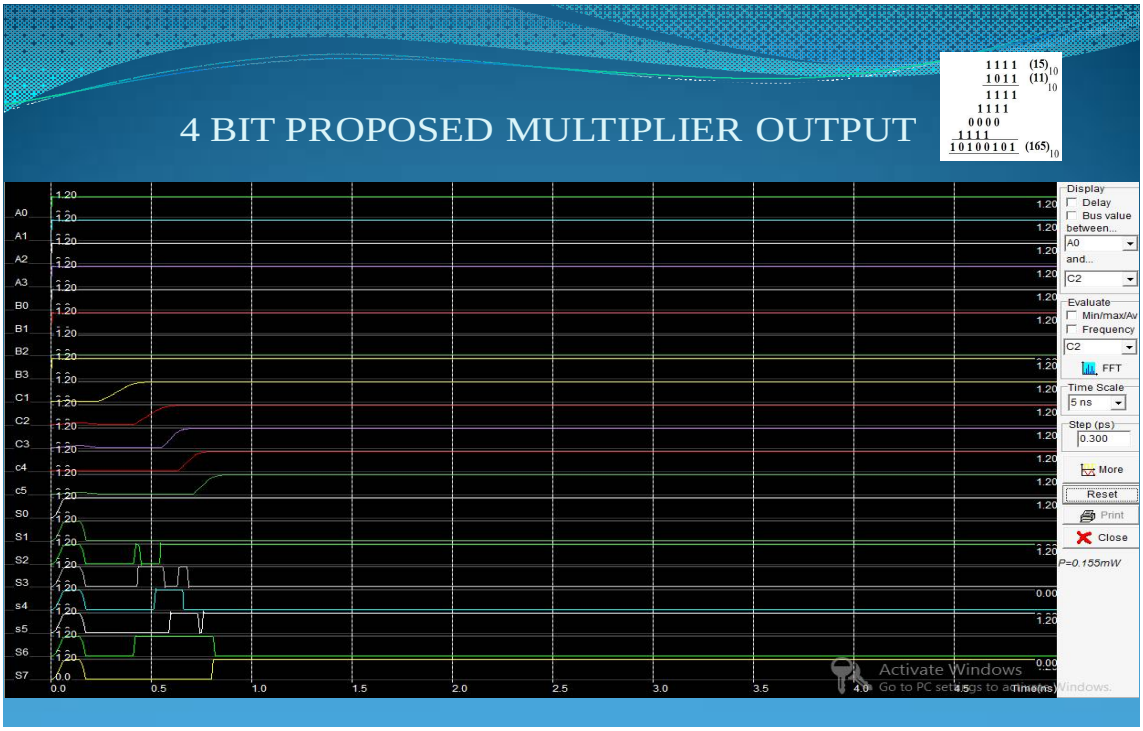

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V.CONCLUSION

A new multiplier is designed by using CBL logic it achieved area and speed higher than that of the existing multiplier, with an area requirement comprisable with the CSLA demonstrated .These multiplier could propagate a carry signal and sum signal with low power dissipation and propagation delay. In addition because of adopted basic logic and layout strategy number of clock cycle required for completing the elaboration was limited and hence it reduce the power dissipation. The area and the propagation delay should be reduced by using CBL logic. Finally the multiplier has been designed efficiently in terms of low area, less propagation delay and low power dissipation.

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