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Design of a 16-Bit SAR ADC that is Power Efficient

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ABSTRACT: This research investigates the feasibility of employing a 16-bit architecture to construct a SAR_ADC. The SAR_ADC configuration is favored for applications demanding high decision-making due to its simplicity and low power utilization. The design incorporates several key elements, including sample-and-hold circuitry, an ADC, a comparator, a voltage reference, a subsequent approximation registers and among others. Various design strategies and electrical system layouts are utilized to enhance accomplishment and fulfill the necessary specifications. The comparator is engineered to accurately identify the analog input voltage while ensuring swift operation. The successive approximation register employs a binary search method to determine the digital equivalent of the input voltage. The architecture is implemented using gate diffusion input technique at 250nm, with simulations and verifications conducted through the Tanner EDA tool. Findings show that the developed 16-bit SAR_ADC fulfills the targeted decision-making and satisfies the outlined accomplishments benchmarks. The ADC demonstrates efficient power usage and satisfactory operational accomplishment. This architecture finds utility in a board spectrum of fields, including telecommunications, scientific measurement equipment, and medical imaging, where precise ADC conversion is Imperative.

KEYWORDS: SAR ADC, ADC, power consumption, D-flip flop.

I. INTRODUCTION

Analog to digital converters serve an essential role in discrete digital conversion from continuous analog formats, which are fundamental building blocks of modern electronic systems. As the need for enhanced decision- making and precision in signal processing continues a rise, the design of high decision-making ADCs has emerged as a pivotal area of research and innovation across numerous applications. The SAR_ADC architecture was chosen for its capability to deliver outstanding decision marking alongside a reasonable degree of complexity. To generate a precise digital output, the SAR_ADC employs a binary search methodology for the conversion process. Digital to Analog converters are integral to the design of the sequential approximation register ADC. A key element involved in capturing the continuously varying voltage of an analog signal is the test and retain circuit, sometimes known as a sample and follow circuit. The circuit recovering the signals voltage and maintains it at a steady level for a predefined duration. The voltage reference serves as a standard against which the input voltage is measured, offering a consistent and accurate point. Achieving high precision and linearity in the DAC is facilitated through various techniques, including the use of binary weighted capacitor arrays.

ANALOG TO DIGITAL CONVERTER:

Analog to digital converters functioning as electrical devices, possess the ability to compute, manage, and transform the myriad analog signals found in everyday environments into a quantized or binary form. These converters are indispensable elements within any system engaged in digital signal processing or digital image processing, as computers exclusively handle binary signals.

II. RELATED WORK

The successive approximation register an analog to digital converter that converts analog input signals into digital formats is known as a SAR. This method has seen extensive application in prior studies and advancements. SAR_ADCs are noted for their moderate speed, low power usage, and relatively uncomplicated architecture, making them versatile and widely adopted. Successive approximation ADCs come in various decision makings and are particularly sought after for their affordability, making them suitable for medium to high decision-making applications.

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Their small SAR_ADCs are perfect for use in battery operated, portable devices because of their small size and low power consumption. The SAR_ADC comprises key elements including SAR logic determines each bit, a DAC gets the analog value of the SAR outcome a circuit(S/H) records the reference signal, and a comparator evaluates the analog input signal.

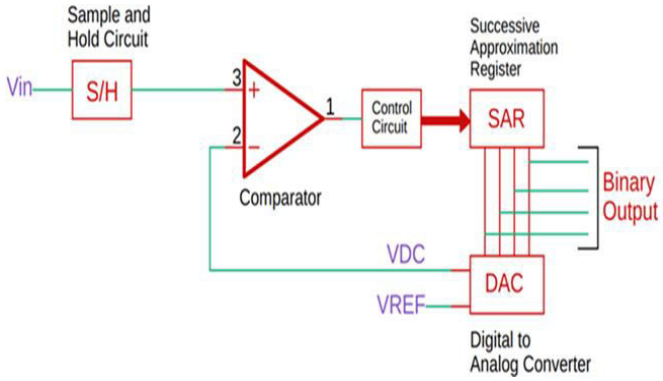

Fig: 1 SAR ADC

Sample & Hold circuit:
A sample and hold circuit uses a predefined span to receive continuously varying voltage analogue signals while locking at a predetermined constant voltage value [10].

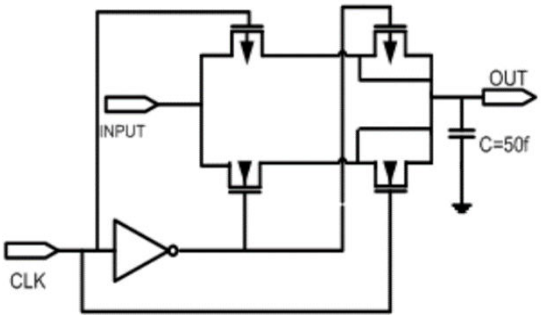

Fig: 1.1 Circuit for sampling and holding

In this sample and hold circuit, a condenser maintains an electrical charge. One switching component—such as an active amplifier or a transistor with a field effect—is all that needs to sample and store the input data before passing it to the comparator.

Comparator:
A comparator refers to an electrical circuit or component tasked with producing an output based on the comparison of two input voltage and its result. The SAR_ADCs are widely utilized across various applications, such as analog to digital conversion, detecting voltage levels, and circuitry for threshold sensing.

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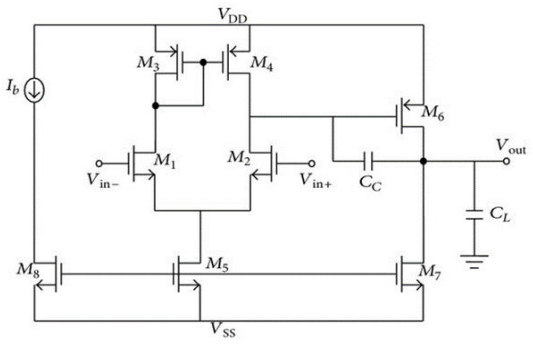

Fig 1.2 illustrates two-stage op-amp.

The two-stage op-amp consists of two differential amplifier stages connected in series. Each stage typically consists of a differential amplifier followed by a gain stage. This configuration is commonly used in op-amp designs to achieve high gain with improved linearity, and increased bandwidth compared to single-stage op-amps [7].

III. PROPOSED METHOD

The advantages of both static CMOS (Complementary Metal-Oxide Semiconductor) and dynamic logic are combined in the logic style known as GDI (Gate-Diffusion Input), which is employed in the construction of digital circuits. Comparing GDI logic to traditional CMOS logic designs, the former offers better power efficiency, less area overhead, and easier circuit design. An explanation of GDI logic is provided below:

Basic Components: A GDI cell, or P-type metal-oxide semiconductor (PMOS) transistor and N-type metal-oxide semiconductor (NMOS) transistor coupled in series, is the fundamental component of GDI logic. When the source and gate of the PMOS transistor are connected, a "diffusion" input is produced. The NMOS transistor's drain is its output. Contrary to conventional CMOS, GDI logic does not directly use the input signal to regulate the transistors' gate voltages. Instead, it uses a gate-input structure. The diffusion input of the GDI cell is instead controlled by a binary-encoded input signal. The number of stacked transistors in the diffusion input determines how many bits are encoded in binary. Operation:

Pull-Down Operation: The NMOS transistor is off when the input signal is "0," while the PMOS transistor is switched on. This enables the output to be pushed down to the low voltage level (ground), with the PMOS transistor acting as a switch between the output and the high voltage supply.

Pull-Up Operation: The NMOS transistor is switched on when the input signal is "1," while the PMOS transistor is off. As a result, the output can be switched between the low voltage level (Vdd) and ground using the NMOS transistor, which also serves as a switch.

GDI Logic's benefits include:
Reduced Area Overhead: GDI logic has a reduced area footprint than traditional CMOS logic since fewer transistors are needed.

Power Efficiency: By GDI logic's reduced switching activities and the amount of transistors actively engaged in logic operations, power efficiency is improved. Circuit design is made easier by GDI logic's use of a consistent GDI cell structure, which makes it simpler to build and optimize complex digital circuits.

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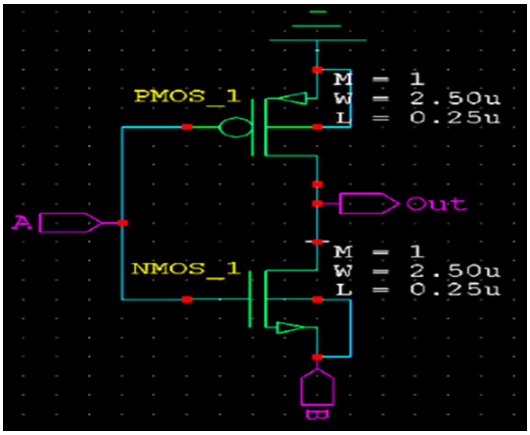

Fig: GDI for NOR gate

DAC:

A DAC is a device or circuit that converts a digital signal into an analog signal by utilizing discrete digital values. It generates a continuous analogue output that is proportionate to the input digital value by taking a succession of discrete digital values—typically expressed as binary numbers—and converting them into discrete digital values.

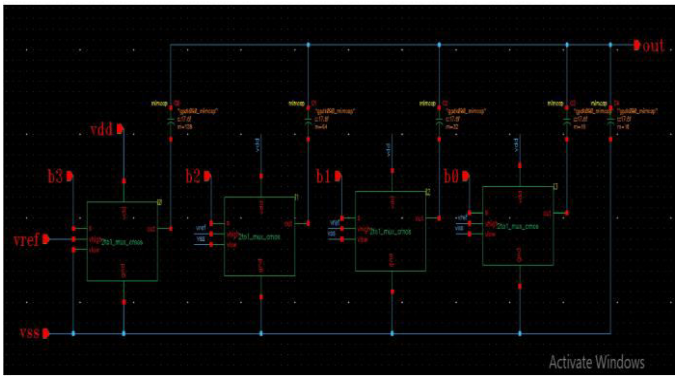

FIG: 4 DAC Schematic of 2:1 mux in CMOS

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COMPARISON TABLE:

In existing method, we used CMOS technology but compared to that GDI technique gives less power consumption and delay.

METHOD	AREA	POWER	DELAY
EXISTING METHOD	1130	0.991mw	14.43ns
PROPOSED METHOD	1130	23.3µW	34.46ns

Table 1: comparison between proposed and existing method

IV. CONCLUSION

This paper16-bit successive Tanner 250nm GDI technology simulates the ADC approximation functionally. As the SAR ADC consumes more power, to achieve minimum power consumption, a low-power comparator and DAC are utilized. In the domain of biomedical applications, it was believed that the SAR ADC was more appropriate. Providing a summary of the SAR ADC brings this endeavor to a close. The outputs supplied with this logic are quite solid, according to the GDI-based SAR ADC, and they have less area, latency, and power. As technology continues to evolve, SAR ADCs are expected to further advance in terms of resolution, speed, power efficiency, and integration capabilities. These advancements will enable SAR ADCs to meet the increasing demands of modern applications, ensuring accurate and reliable conversion from analogue to digital for a variety of technologies in various industries.

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