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Survey on Reversible Arithmetic Logic Unit using Programmable Reversible Gate

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ABSTRACT: In today's world reversible arithmeticlogic unit is one of the very important parts of any system having many applications in computers, mobile, calculators etc. Reversible logic is useful in mechanical applications of nanotechnology, given that the friction generated by contacting corpuscles within a confined volume can be significantly reduced by eliminating sliding contact using mechanical reversible logic.
We have reviewof reversible arithmetic logic unit based on reversible programmable gate. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. Reversible arithmetic logic unit are consisting of different gate.

KEYWORDS: Reversible Gates, Reversible Arithmetic Logic Unit, VHDL Implementation

I. INTRODUCTION

An Arithmetic and Logic Unit (ALU) is a combinational circuit that performs logic and arithmetic micro-operations on a pair of n-bit operands (ex. A[3:0] and B[3:0]). The operations performed by an ALU are controlled by a set of function-select inputs. In this lab you will design a 4-bit ALU with 3 function-select inputs: Mode M, Select S1 and S0 inputs. The mode input M selects between a Logic (M=0) and Arithmetic (M=1) operation. The functions performed by the ALU are specified in Table 1.1.
When doing arithmetic, we need to decide how to represent negative numbers. As is commonly done in digital systems, negative numbers are represented in twos complement [6]. This has a number of advantages over the sign and magnitude representation such as easy addition or subtraction of mixed positive and negative numbers. Also, the number zero has a unique representation in twos complement.

Table 1.1: Functions of ALU

M =0 Logic				
S1	S0	C0	Function	Operation
0	0	X	A_i. B_i	AND
0	1	X	A_i + B_i	OR
1	0	X	A_i \$ B_i	XOR
1	1	X	A_i !\$ B_i	XNOR
M =1 Logic				
S1	S0	C0	Function	Operation
0	0	0	A	Transfer A
0	0	1	A+1	Increment A by 1
0	1	0	A+B	Add A and B
0	1	1	A+B+1	Increment the sum of A and B by 1
1	0	0	A+B'	A plus one's complement of B
1	0	1	A-B	Sub-tractor B from A (i.e. B'+A+1)
1	1	0	A'+B	B plus one's complement of A
1	1	1	B-A	B minus A (or A' + B +1)

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There are different ways to design a bit-slice of the ALU. One method consists of writing the truth table for the one bit ALU. This table has 6 inputs (M, S1, S0, C_0, A_i and B_i) and two outputs F_i and C_{i+1}. This can be done but may be tedious when it has to be done by hand.

An alternative way is to split the ALU into two modules, one Logic and one Arithmetic module. Designing each module separately will be easier than designing a bit-slice as one unit. A possible block diagram of the ALU is shown in Figure 1. It consists of three modules: 2:1 MUX, a Logic unit and an Arithmetic unit.

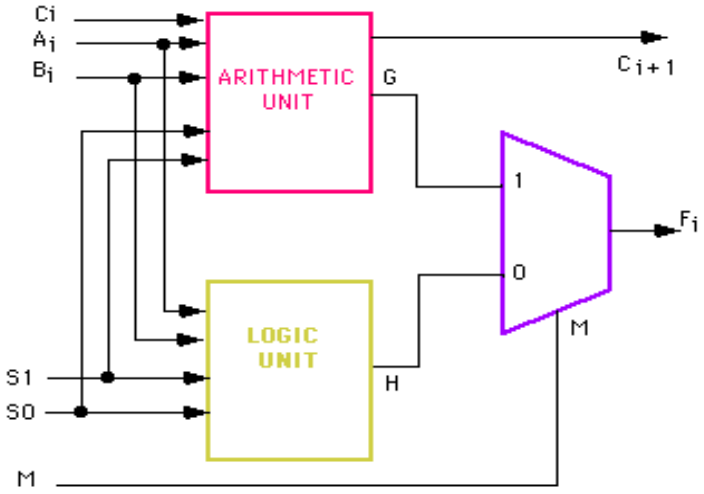

Figure 1: Block diagram of a bit-slice ALU

II. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

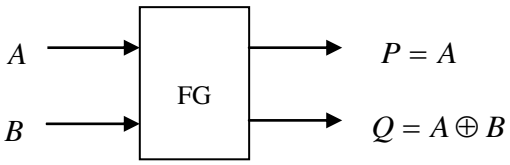

Figure 2: Feynman gate

In figure 3, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

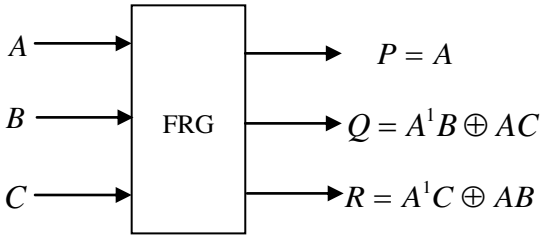

Figure 3: Fredkingate

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Figure 4 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

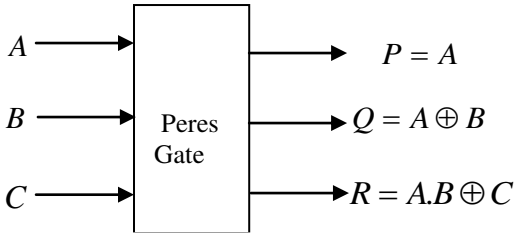

Figure 4: Peres gate

The HNG gate, presented in fig, produces the followinglogical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 5.

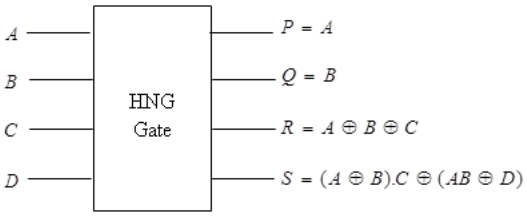

Figure 5: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

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Fig. 6 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

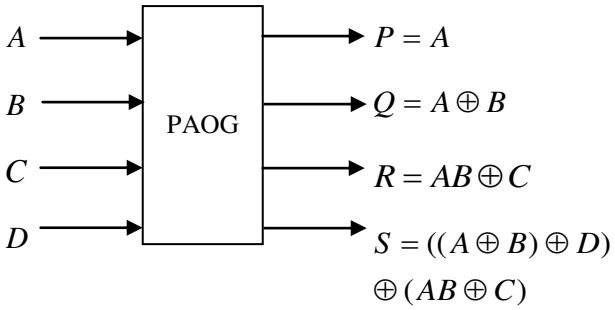

Figure 6: Block Diagram of the PAOG

Several 4x4 gates have been described in the literature targeting low costand delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the followinglogical output calculations:

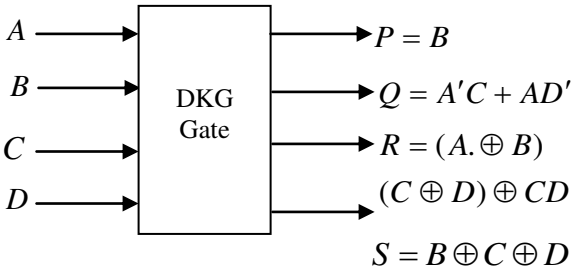

Figure 7: DKG Gate

$$P = B \quad (9)$$

$$Q = A'C + AD' \quad (10)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

III. LITERATURE REVIEW

S. Nagaraj et al. [1],an Arithmetic logic Unit (ALU) is used in arithmetic, logical function in all processor. It is also an important subsystem in digital system design. Arithmetic Logic Unit (ALU) is one of the most important components of any system and is used in many appliances like calculators, cell phones, and computers .A 32-bit ALU was designed using Verilog HDL with the logical gates such as AND and OR for each one bit ALU circuit. The design was implemented in Xilinx. It can work fast than the ALU processor using less power. The design of an ALU and a Cache memory for use in a high performance processor was examined. ALU which are designed using non reversible logic gates consume more power. So there is a need for lesser power consumption and the reversible logic has been playing vital role during recent years for low power VLSI Design techniques. This technique helps in reducing power consumption and power dissipation. This paper presents an implementation of ALU based on reversible logic while comparing it to ALU architecture with the normal logic gates. All the modules are simulated in modelsim SE 6.4c and synthesized using Xilinx ISE 14.5. ALU which is designed using non reversible logic gates consume more power of about 0.312 mw and the implementation of ALU based on reversible logic reduces the power consumption during operations to about 5.1 percentages.

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Behrouz Safaiezadeh et al. [2], quantum dot cellular automata (QCA) technology is considered as one of the most suitable replacements to reduce the CMOS-based digital circuit design problems at the nanoscale due to its tiny size, fast, latency and very low power consumption. One of the main components of microprocessors is the arithmetic logic unit (ALU) and in other words, it acts as the heart of microprocessors. This paper presents a QCA technology-based reversible ALU unit using basic reversible blocks and a novel reversible block namely BS1 Block. The proposed block performs logic and arithmetic operations in the proposed scheme. The simulations of the proposed design are carried out by QCA Designer. According to the simulated results, the proposed structure has a 35%, 27% and 30% improvement in quantum cost, the number of cells and the occupied area in comparison to the previous conducted researches, respectively.

Hari M. Gaur et al. [3],the emerging technology of reversible circuits offers a potential solution to the synthesis of ultra low-power quantum computing systems. A reversible circuit can be envisaged as a cascade of reversible gates only, such as Toffoli gate, which has two components: k control bits and a target bit (k-CNOT), $k \geq 1$. While analyzing testability issues in a reversible circuit, the missing-gate fault model is often used for modeling physical defects in quantum k-CNOT gates. In this paper, we propose a new design for testability technique for quantum reversible circuits in which the gates of a circuit are grouped into different sets and the gates from each set are attached to an additional input line via an extra control. Such arrangement makes it possible to test the gates belonging to a set separately. Our algorithm exploits the feature of many reversible circuits in which the high quantum cost gates have target on the same line and this line is devoid of any control of other gates. All these gates skip addition of extra control for testing. The proposed technique offers less quantum cost in comparison to other DFT techniques published so far.

ParthKhatter et al. [4],reversible logic have received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. ALU is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, ALU based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output DPeres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. These Reversible ALU has been modeled and verified using Verilog and Quartus II 5.0 simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

S. M. Swamynathanet al. [5],an Arithmetic logic Unit (ALU) is used in arithmetic, logical function in all processor. It is also an important subsystem in digital system design. Arithmetic Logic Unit (ALU) is one of the most important components of any system and is used in many appliances like calculators, cell phones, and computers .A 32-bit ALU was designed using Verilog HDL with the logical gates such as AND and OR for each one bit ALU circuit. The design was implemented in Xilinx. It can work fast than the ALU processor using less power. The design of an ALU and a Cache memory for use in a high performance processor was examined. ALU which are designed using non reversible logic gates consume more power. So there is a need for lesser power consumption and the reversible logic has been playing vital role during recent years for low power VLSI Design techniques. This technique helps in reducing power consumption and power dissipation. This paper presents an implementation of ALU based on reversible logic while comparing it to an ALU architecture with the normal logic gates. All the modules are simulated in modelsim SE 6.4c and synthesised using Xilinx ISE 14.5. ALU which is designed using non reversible logic gates consume more power of about 0.312 mw and the implementation of ALU based on reversible logic reduces the power consumption during operations to about 5.1 percentages.

Kamarajet al. [6],in the current scenario, power consumption, speed, size and heat dissipation are the huge challenge in the semiconductor industries. When the size of the single computing element is reduced then the speed can be improved and also if the power dissipation is reduced then the heat dissipation will be less. The possible solution for these two problems is the Reversible Logic and Quantum Cellular Automata (QCA). The Reversible Logic is considered to be the promising technology to the future Quantum computer technologies. The Reversible Logic gates prune the power dissipation to a larger extent. In this paper Novel Reversible Gates are proposed with Reversibility and Universality. The Arithmetic and Logic Unit (ALU) is designed with the proposed Reversible Gates in Reversible

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Logic. The designed Arithmetic and Logic unit is evaluated in QCA with the required specifications. The Arithmetic and Logic Unit is designed by setting the control inputs for each unit. The parameters taken into account are Quantum Cost (QC), Garbage Outputs (GO), Constant Inputs (CI), Area, Number of Cells and Simulation Time. The proposed ALU adopting Novel gates finds utilization in low power applications. Also it can be used as the module in the Quantum computers due to its reduced Quantum Cost and Garbage outputs. The Proposed design extends its applications over Quantum Computing, Optical Computing, Nanotechnology and DNA mapping.

Gopi Chand Naguboina et al. [7],reversible logic is the emerging field for research in present era. The aim of this paper is to realize different types of combinational circuits like full-adder, full-subtractor, multiplexer and comparator using reversible decoder circuit with minimum quantum cost. Reversible decoder is designed using Fredkin gates with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and many more. Reversible logic is defined as the logic in which the number output lines are equal to the number of input lines i.e., the n-input and k-output Boolean function F(X1, X2, X3,…,Xn) (referred to as (n, k) function) is said to be reversible if and only if (i) n is equal to k and (ii) each input pattern is mapped uniquely to output pattern. The gate must run forward and backward that is the inputs can also be retrieved from outputs. When the device obeys these two conditions then the second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back are not allowed in Logical Reversibility. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI Etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption. The comparative study in terms of garbage outputs, Quantum Cost, numbers of gates are also presented. The Circuit has been implemented and simulated using Xilinx software.

Michael Nachigal et al. [8], the design of encoder/decoder can be analyzed in terms of quantum cost, garbage outputs, constant inputs. Reversible computational work totally differs from traditional computation, as it preserves information while manipulating it. Various reversible combinational and sequential designs have been implemented based on reversibility nature of the circuit. Very little focus has been done on reversible encoder/decoder design. The author proposed a novel design, where 2:4 encoder and decoder are implemented by using Friedkin gates whose quantum cost associated is 5 instead of peres gate whose quantum cost is 4. This work also represents the improvement in garbage output that is added to a multiple output function to make it reversible. Implemented or proposed design for decoder/encoder improves over existing design in terms of performance metrics except for the delay.

Md. Shamsujjoha et al. [9], by stating that a fault tolerance gate (F2G) itself work as 2 to 1 reversible decoder. A fault tolerance reversible decoder has its application in Multiple-symbol differential detection, parallel circuits, network components etc. One F2G and two FRG are used to realize 2 to 4 fault tolerance reversible decoder. Further design can be extended to 3 to 8 reversible decoder using FRG gates and Feynman double gate. Similarly a reversible 4 to 2 encoder design which behaves like a traditional encoder i.e., exactly one of its four inputs will have the value of logical 1 at any point. The design has zero constant inputs and two garbage outputs. Constructed circuits can detect any type of single bit error for stuck-at fault. This technique also minimizes the garbage outputs during the process of conversion to testable, but the design is not much optimized in terms of quantum gates, constant input, and delay.

Nusrat Jahan Lisa et al. [10], designs a 2 to 4 decoder, which generates all four necessary AND functions using 1 Peres gate and 3 CNOT gate, therefore a total number of quantum gates are seven. The design can be extended to 3 to 8 decoder using 2 to 4 decoder circuit and four Fredkin gates and 4 to 16 decoder circuit using three 2 to 4 decoder and eight fredkin gates. Also, represent the properties of n to the 2^n reversible decoder with a generalized algorithm. Design greatly improves over a conventional design of decoder can be constructed to improve the garbage output comes at the cost of a slightly higher quantum cost. Arvind Kumar et al. [9] concluded that the 2 to 4 decoder uses fredkin gates. Since all three fredkin gates are reversible in nature thus having less power dissipation. Design can be extended up to n to 2^n decoder. A 4 to 16 decoder has been designed uses 15 constant inputs and 4 garbage outputs. This work is quite effective in terms of performance with three fredkingate; total delay will be more which in turn leads to more power dissipation claims that this design is not an effective approach.

I. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog. VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated

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circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).
Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-
Gate Count (GC): The number of gates used to realize reversible circuit
Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.
Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.
Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.
Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

IV. CONCLUSION

This thesis mainly focuses on a novel design of reversible processor components. Internal architecture components i;e, ALU, CU, register files and PC having better performance with proposed circuitry as compared to previous counterparts. Also, registers and the memory for program and data fall into the category of improved performance with reduced delay. Memory access pattern, execution, and complexity of instruction are kept in mind improve the execution time by using Harvard architecture instead of von Neumann. Power dissipation is also less about negligible since an overall system is designed using reversible nature of logics. With all above demonstration, using proposed designs improve the performance of CPU and execution time will be faster.

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