ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

Design, Implementation & Performance of Vedic Multiplier for Different Bit Lengths

Vishikha Sharma[1], *Aniket Kumar[2]

M. Tech Scholar, Department of Electronics Engineering, Shobhit University, Meerut, India[1]

Assistant Professor, Department of Electronics Engineering, Shobhit University, Meerut, India[2]

ABSTRACT: This paper describes the design of Vedic Multiplier based on Urdhva Trigbhyam technique of multiplication. It is one of the ancient Vedic sutras for multiplication it means vertical & crosswise. The paper compares the design of Vedic Multiplier for different bit lengths based on Ripple Carry Adder & Kogge Stone Adder. For the highly efficient processor, multiplier plays an important role. It has been found that Kogge Stone Adder is fastest Parallel Prefix Adder, hence the delay in Vedic Multiplier based on Kogge Stone Adder is less as compared to that based on Ripple Carry Adder. The proposed algorithm has been designed using VHDL. Implementation has been done using Xilinx 14.4 with family Spartan6, device as xc6slx45, package csg324 with speed grade of -3.

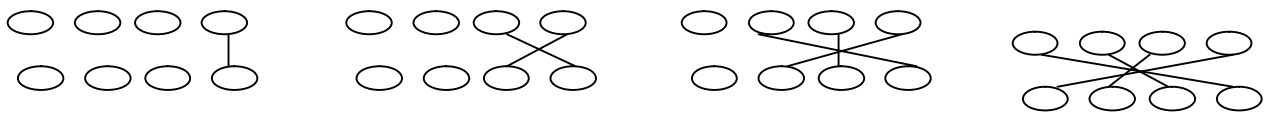
KEYWORDS: KSA, RCA, Urdhva Trigbhyam, Vedic Multiplier

I. INTRODUCTION

Multipliers play an important role in the arithmetic operation. In microprocessor and most of the digital signal processing algorithm, many instructions perform operations like addition and multiplication, therefore these operations play a vital role in execution time. In present time the demand of computer and signal processing application is increased so the demand of high speed processor is also increased. In order to achieve desired performance in real time applications, the performance of multiplier must be high with low power consumption, delay and area. Vedic multiplier has become more popular technique and it is widely used where high speed and low power are major concern. It is nothing but a sequence of additions carried out on partial products as suggested by Jagadguru Swami [1]. In this paper, the multiplier has been designed using URDHVA TRIGBHYAM sutra one of the 16 Vedic sutras based on ancient Vedic mathematics [2]. The used adders are Ripple Carry Adder and Kogge Stone Adder.

II. RELATED WORK

Urdhva Tiryakbhyam, Multiplication is based on a technique that is called Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula which is applicable to all types of multiplication. The Sanskrit term means “Vertically and crosswise”. It requires less amount of time for any computation as suggested by M. Poornima [3] than other Vedic sutras like Ekadhikina Purvena, Nikhilam Navatashcara-mam Dashatah etc .It is employed as one of the ancient Vedic multiplication technique [4]. A general method of multiplication is as shown below:-



Step I Step II Step III Step IV

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

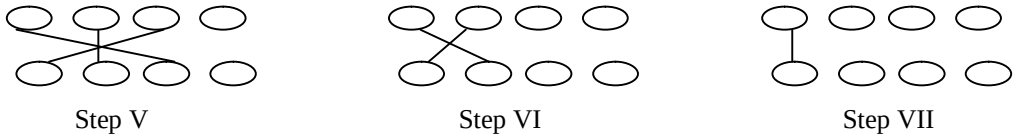


Fig. 1 Four Bit Vedic Multiplier

In fig.1, this method shown the Vedic multiplication of 4 bits, as the number of bits increases area and gate delay increases at a fader rate in Urdhva multiplication as compared to other techniques, therefore the techniques has been employed here for Vedic multiplication.

III. PROPOSED ALGORITHM

1. Ripple Carry Adder

Ripple Carry Adder is one of the digital adder [5, 6] used in many logic circuits. In this adder circuit the carry and sum bits are produced alongside, in which the *carry*-out of each full adder is the carry in of the following next most significant full *adder*. It is called a *ripple carry adder* because each carry bit gets rippled into the next stage. Fig. 2 shows the basic hierarchical block diagram of 4 bit adder using 1 bit adder.

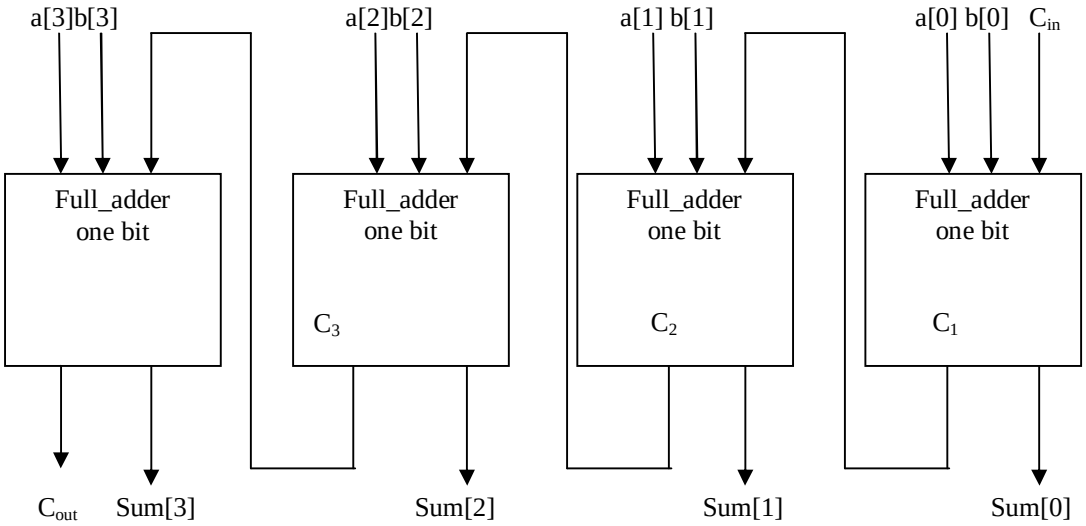


Fig.2 Four bit Ripple Carry Adder

2. Kogge Stone Adder

It is one of the fastest parallel prefix adder. It generates the carry signals in O (log n) time[7-8]. It uses group generate and propagate functions. It uses three stages

i) Pre-processing
ii) Carry look-ahead network
iii) Post-processing

In Pre-processing stage, propagate (p) and generate (g) functions are calculated as

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

p=a xor b;
g=a and b;

In Carry look-ahead network, group propagates and generates functions are calculated as:-

cp[i]=p[i] and p[i-1]
cg[i]=g[i] or (g[i-1] and p[i])

In Post-processing network, sum and cout is calculated

sum[i]=p[i] xor cg[i-1]

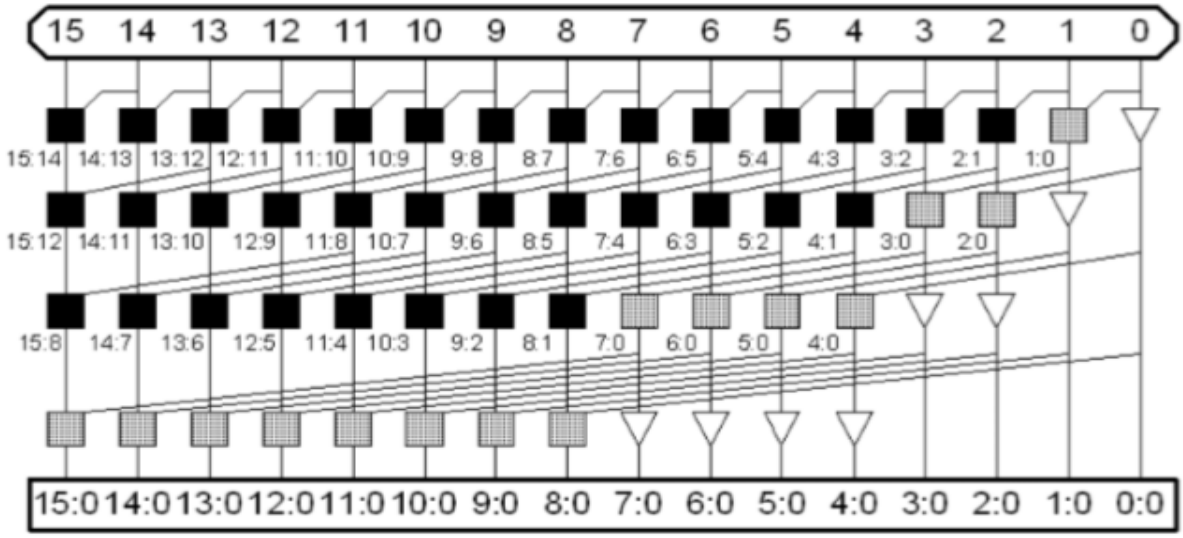


Fig.3 16 bit Kogge Stone Adder Network

3. Vedic multiplier

Multiplication methods that many of processors are using today has inspired by Vedic multiplier introduced in Indian Vedas with different 16 sutras. Vedic multiplier uses bit-wise multiplication with simultaneous product term finding and it's column-wise addition. It is one of the best benchmark for fast multiplication algorithm.

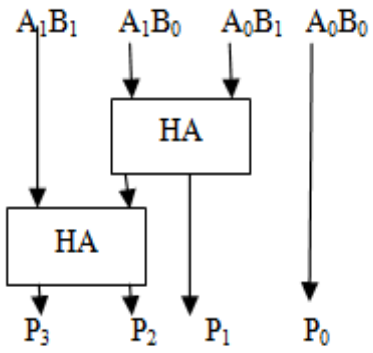


Fig.4 2X2 bit Vedic basic element

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

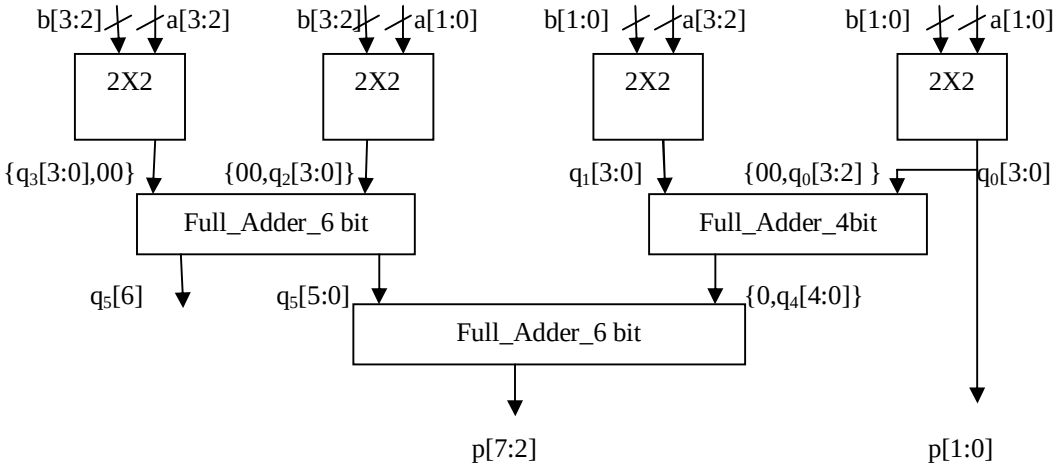


Fig.4 4x4 bit Vedic basic element

Firstly the 2 bit Vedic Multiplier has been designed using two half adders [9, 10] & four AND gates. Next the four 2 bit Vedic Multipliers and three Ripple Carry Adders & also by Kogge Stone Adders each of 4 bit, 6 bit, 6 bit are needed for design of 4 bit Vedic Multiplier.

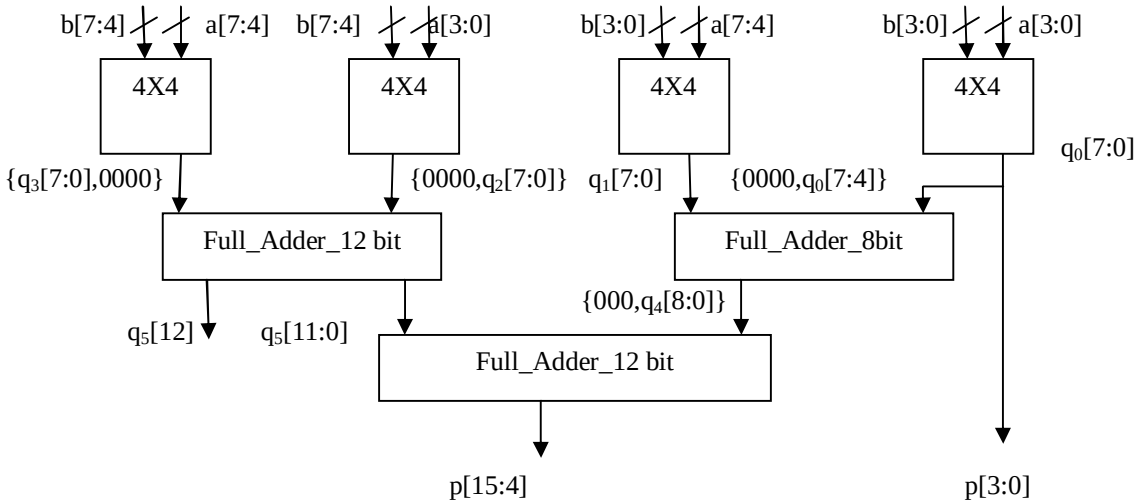


Fig.4 8x8 bit Vedic basic element

The 8 bit Vedic Multiplier has been designed using four 4 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 8 bit, 12 bit.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

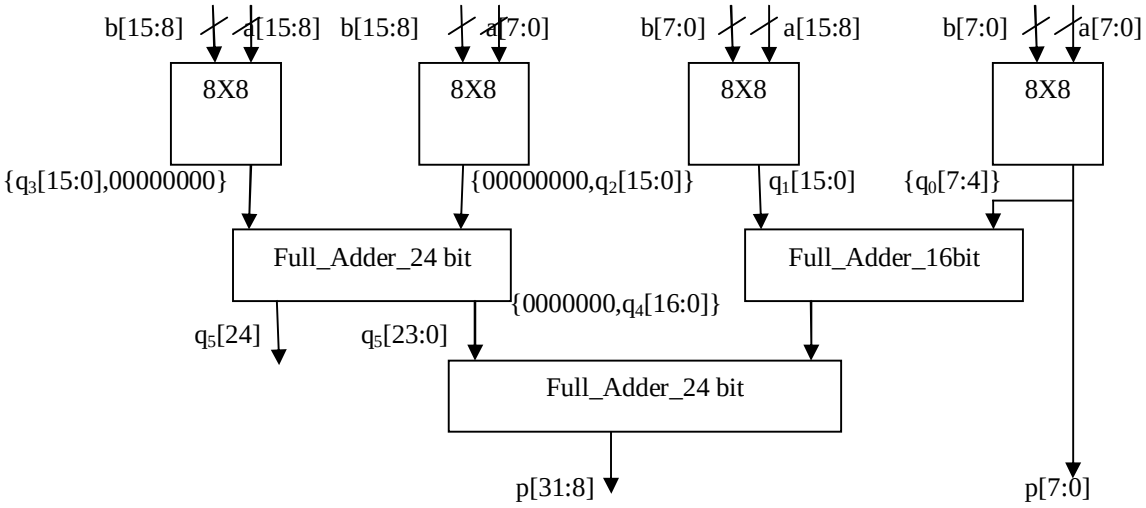


Fig.4 16x16 bit Vedic basic element

The 16 bit Vedic Multiplier has been designed using four 8 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 16 bit, 24 bit, 24 bit. It is found that as the number of bits increases in the multiplier the performance of the system increases.

IV. SYNTHESIS & SIMULATION

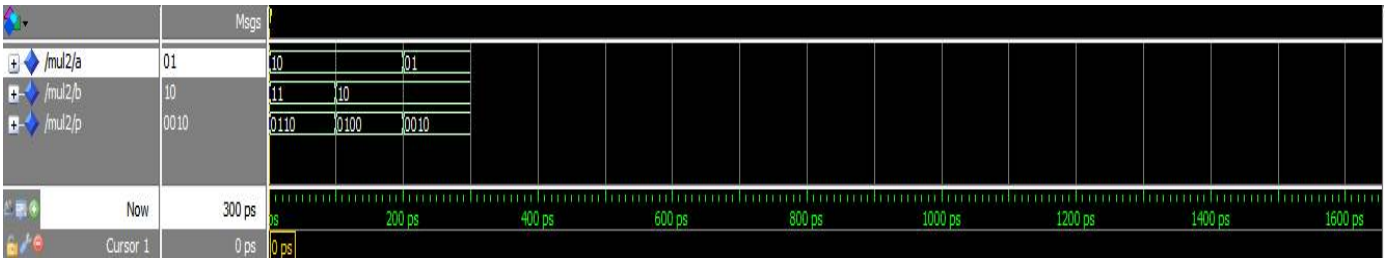


Fig. 5 Simulation Result of 2-bit Vedic Multiplier

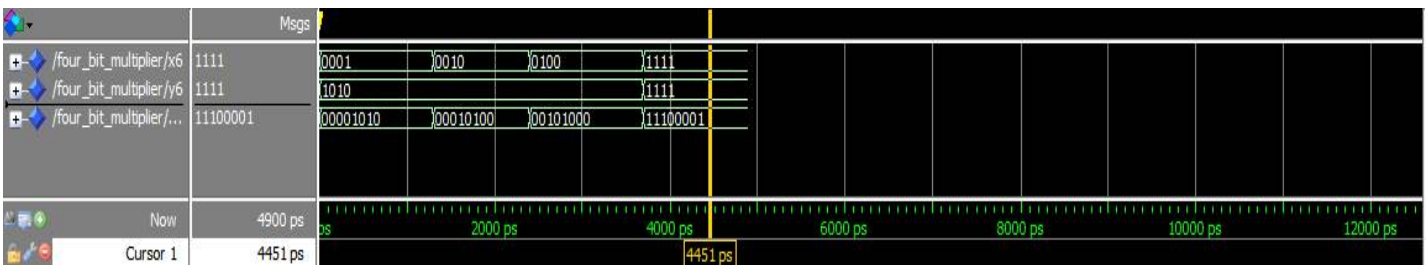


Fig. 6 Simulation Result of 4-bit Vedic Multiplier

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

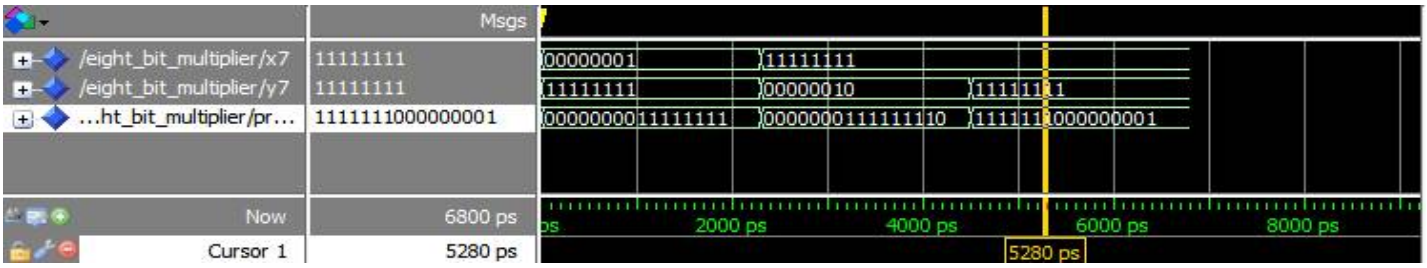


Fig. 7 Simulation Result of 8-bit Vedic Multiplier

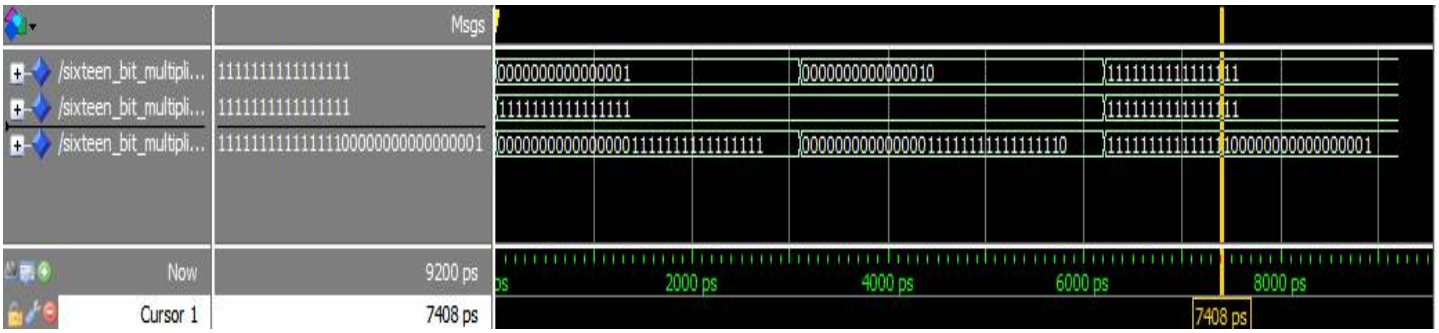


Fig. 8 Simulation Result of 16-bit Vedic Multiplier

V. IMPLEMENTATION

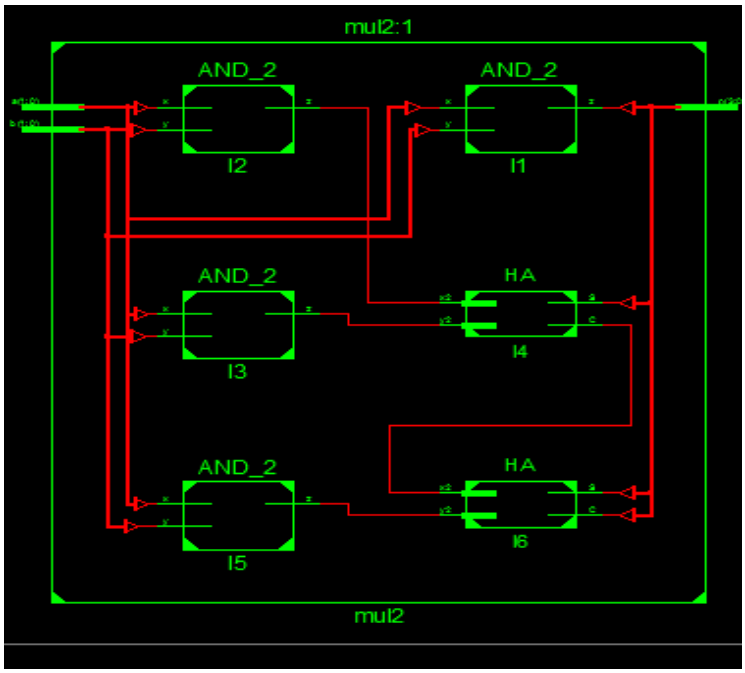


Fig.9 RTL Schematic for 2 bit Vedic multiplier

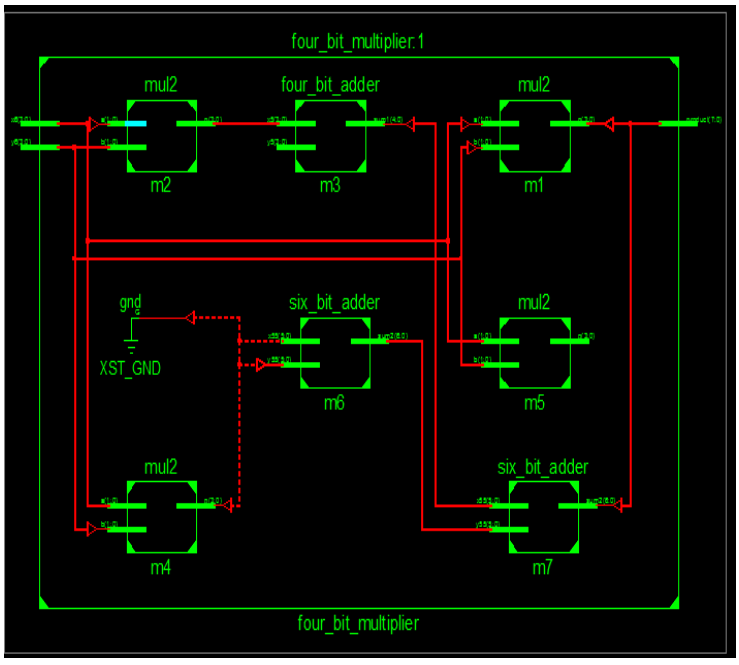


Fig.10 RTL Schematic for 4 bit Vedic multiplier

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

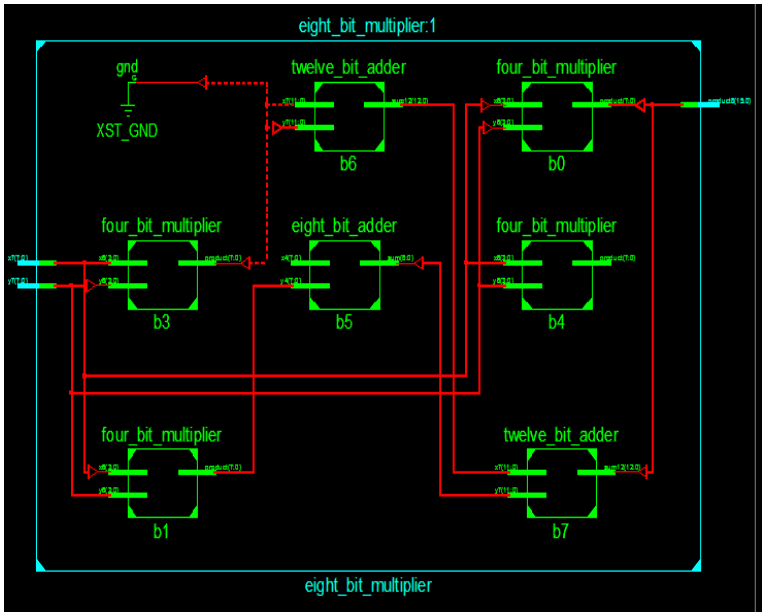


Fig.11RTL Schematic for 8 bit Vedic multiplier

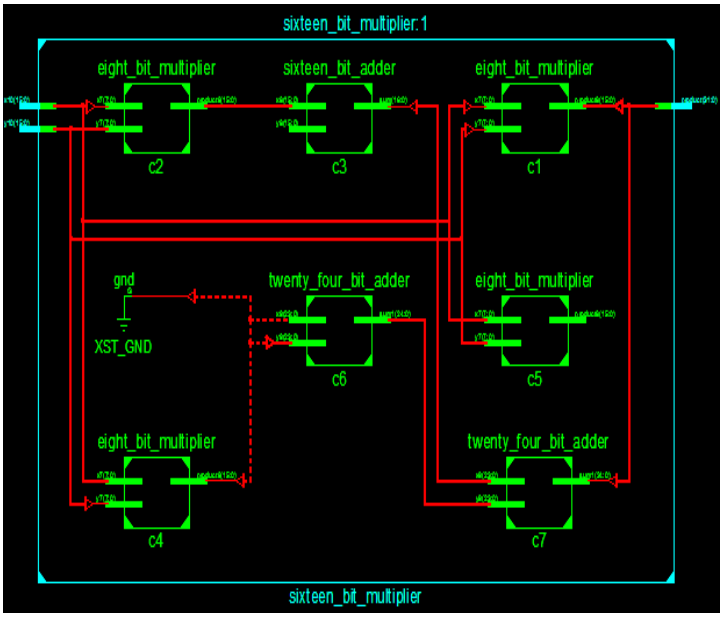


Fig.12 RTL Schematic for 16 bit Vedic multiplier

Simulation has been done on Model-Sim Altera Edition 6.6d & Implementation has been done using Xilinx 14.4 with family Spartan6, device as xc6slx45, package csg324 with speed grade of -3. Synthesis report obtained for the above multiplier provides us many parameters such as Delay, Levels of Logic, Memory , No. of slice, no. of LUTs and many more for comparative analysis of vedic multiplier for different bit-lengths.

Table I Comparative Analysis

Device-Spartan6 XC6SLX45-CSG324	**Using Ripple carry adder**				
Vedic Multiplier	**Delay (ns)**	**Levels of Logics**	**No. of slice LUTs**	**Memory (KB)**	**Fan Out**
2-Bit	6.494	4	6	258052	10000
4-Bit	7.942	5	7	255024	500
8-Bit	18.270	15	121	257988	100000
16-Bit	27.278	23	656	259076	100000

VI. Conclusion and Future Work

From implementation, simulation & comparative results, it is concluded that delay in 16 bit vedic multiplier is 27.278 ns & memory used is 259076 KB. Look-up table (LUTs) is maximum for 16-bit multiplier & hence lowers packaging density, Similar work can be performed for Kogge Stone Adder, Array multiplier, Wallace Tree and Shift & Add Multiplier etc. that would led us to make a conclusion , which multiplier is best ,if speed is critical thing , if Packaging is the concern area & similar conclusions.

References

1. Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja “Vedic Mathematics or Sixteen Simple Mathematicle Formulae from the Veda, Delhi(1965)”, Motilal Banarsidas Varanasi, India.
2. Kumar G., “Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques”, International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012, pp. 1-5.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 4, April 2017

3. Prabir Saha, Arindham Banerjee, Partha Battacharyya, Anup Dhandapat, "High speed design of complex multiplier using Vedic mathematics", Proceedings of the 2011 IEEE students technology symposium, IIT Kharagpur, pp. 237-241, Jan. 2011.
4. Shripad Kulkarni, "Discrete Fourier Transform (DFT) by using Vedic Mathematics"Papers on implementation of DSP algorithms/VLSI structures using Vedic Mathematics, 2006, www.edaindia.com, IC Design portal
5. Laxman S, Darshan Prabhu R, Mahesh S Shetty ,Mrs. Manjula BM, Dr. Chirag Sharma, "FPGA Implementation of Different Multiplier Architectures", International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, Volume 2, Issue 6, June 2012
6. Dr. Ravi Shankar Mishra,Prof. Puran Gour,Braj Bihari Soni, "Design and Implements of Booth and Robertson„s multipliers algorithm on FPGA." International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622.
7. Sunjoo Hong, Taehwan Roh and Hoi-Jun Yoo, "a 145w 8×8 parallel multiplier based on optimized bypassing architecture", department of electrical engineering, Korea advanced institute of science and technology (KAIST), Daejeon, Republic of Korea, IEEE, pp.1175-1178, 2011.
8. Vadivel Sandeep Shrivastava*, Jaikaran Singh* and Mukesh Tiwari*, "Implementation of Radix-2 Booth Multiplier and Comparison with Radix-4 Encoder Booth Multiplier," International Journal on Emerging Technologies 2(1): 14-16(2011) ISSN : 0975-8364
9. Wen-Chang Yeh and Chein-Wei Jen, "High-speed Booth encoded parallel multiplier design", IEEE Transaction on Computers, vol. 49, pp. 692-701, July 2000.
10. Ravindra P Rajput , M.N.Shanmukha Swamy, "High speed Modified Booth Encoder multiplier for signed and unsigned numbers," IEEE International Conference On Modelling and Simulation , 2012