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Review on Low Voltage Dynamic Comparator for High Speed ADC's

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ABSTRACT: Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Opamp. Comparators are mostly used in analog-to-digital converter (ADCs). The need for low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In order to achieve high-speed of comparator, to compensate the reduction of the supply voltages the larger transistors are required, which also means that more die area and power is needed.This paper presents the systematic review of different types of dynamic comparators, comparator architecture their design parameter, study about offset voltage and sources of power and their estimation and reduction technique are discussed. This paper help the practicing engineers/ beginners in this field, able to know what are the significant parameters to design low power dynamic latched comparator and its use in various applications.

KEYWORDS: Dynamic Comparators, Double Tail comparators, high-speed analog-to-digital converters (ADCs), low power analog design, power consumption.

I. INTRODUCTION

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0.

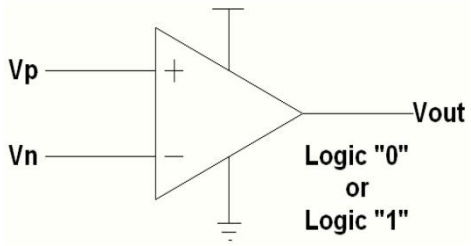

Fig.1: Comparator operation

Comparators are one of the most widely used components in electronic circuits and play a basic role in most applications such as analog to digital convertors (ADC). A comparator, by definition is "a circuit that compares two analog input signals and decodes the difference into a single digital output signal. Depending on the nature, functionality and inputs, comparators are classified into different types such as voltage and current comparators, continuous and discrete time comparators and so on. By another classification there are two different kinds of comparators open loop comparator and regenerative comparator.

These applications often requirethe comparators having features like low power, low-offset[4, 6], high speed with small area. While low poweroperation is achieved from technology scaling, thereduction of supply voltages leads to

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less transistor currentsand results in large delay times. Hence designing highspeed comparators is more challengingissue by using ultralow supply voltage. In other words, in a given technology,large transistors are used to compensate the reduction ofsupply voltages to achieve high speed and thus it meansthat more die area and power is needed.

The main purpose of this paper is to have a systematic review of different types of comparators, its design and analysis. Also this paper presents the comparison of different techniques used for dynamic comparators.

II. RELATED WORK

In this literature review, we will discuss about various type of comparator architecture. The static and dynamic characteristics & advantages and disadvantages of pre-amplifier based comparator are analyzed.

A. Pre-Amplifier Based Comparator:

The comparator consists of three stages

i. input preamplifier stage
ii. latch stage
iii. output buffer stage

The preamplifier stage consists a differential amplifier with active loads. The preamp stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage. It also can reduce the input referred latch offset voltage. The sizes of Ml and M2 are set by taking into consideration the input capacitance and the diff-amp trans-conductance. The trans-conductance sets the gain of the stage, while the size of Ml and M2 mosfets determines the input capacitance of the comparator. Here gm1= gm2.

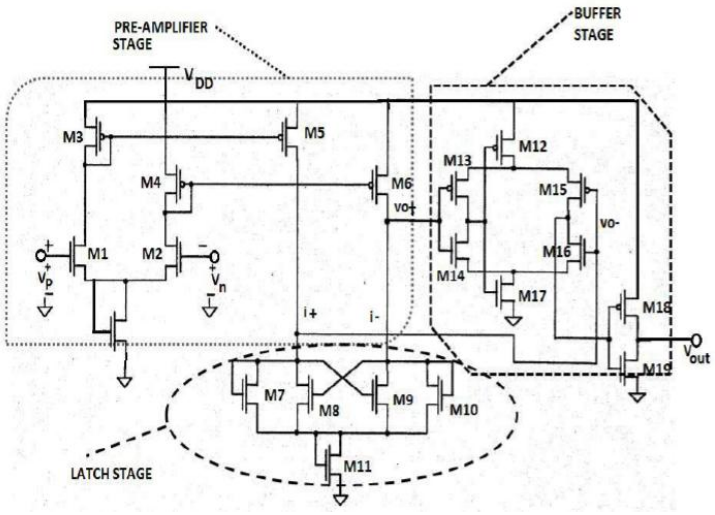

Fig. 2: Pre-amplifier based comparator

The positive feedback latch stage is used to determine which of the input signals is larger and amplifies their difference. The output buffer stage consists of a self-biased differential amplifier followed by an inverter which gives the digital output. It converts the output of the latch stage to a full scale digital level output (logic 1 or logic 0). The output buffer stage should accept a differential input signal and not have slew-rate limitations.

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B. Double-Tail Latch Type Voltage Sense

Figure 3 shows the schematic diagram of the Double-Tail latch type voltage sense amplifier. Double-Tail is derived from the fact that the comparator uses one tail for input stage and another tail for latching stage. It has less stacking and therefore it can operate at lower supply voltages. Large size of the Transistor M14 draws large current at latching stage which is completely independent of common mode voltages at inputs. Also small size of M1 offers lower supply voltages resulting lower offset.

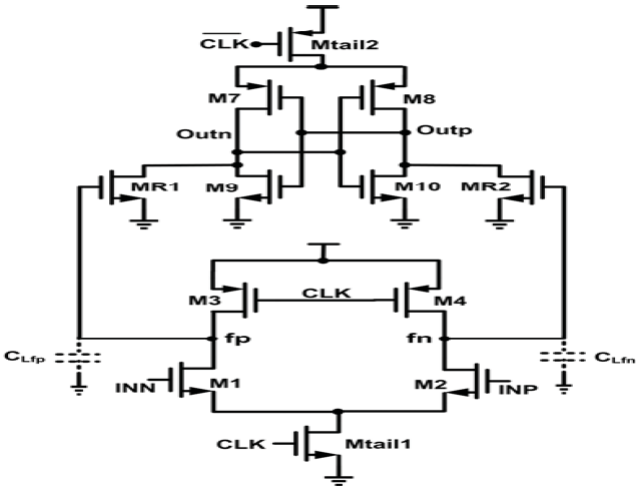

Fig. 3: Double-tail latch type voltage sense amplifier

During reset phase (clk=0V), M4 and M5 charges to VDD which in turn charges Ni (regenerative nodes) nodes to VDD. Then M10 and M11 turns on and discharges output nodes to GND. During evaluation phase (clk=VDD), the transistors M1 and M14 turns ON. So Ni nodes common mode voltage decreases gradually and one input dependent differential mode voltage generates. M10 and M11 pass this differential node voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough for M10 and M11 to clamp the outputs to ground. M10 and M11 also provide additional shielding which reduces kickback noise.

The circuit exhibits the several drawbacks. clk and clkb requires high accuracy timing. The reason is that the latch stage has to regenerate the differential input voltage coming from input stage at very short period of time. Now if we replace the clkb with the inverter whose input is clk signal then clk has to drive heavier load in order to drive largest transistor M14 in a smallest possible delay. Now if clkb leads clk, then comparator will undergo increased power dissipation and if clkb lags clk, it results in increased delay means less speed of operation due to short circuit current path from M14 to M10/M11 through M12/M13.

C. Dynamic Comparator

Figure 4. Shows the Self-Calibrating Dynamic Comparator. This comparator resolved the high accuracy timing between clk and clkb problem by replacing clkb signal with Ni nodes. But it results in increased delay because the transistor M16 and M17 use Ni node voltages as their input signal. Also due to this, the current drivability of the output node decreases. The input referred latch offset is also reduced in this circuit since the output latch stage takes load from the M10, M11 and M16, M17. Maximum drive current of the output node also decreased to half since the supply voltage VDD has been divided into two transistors.

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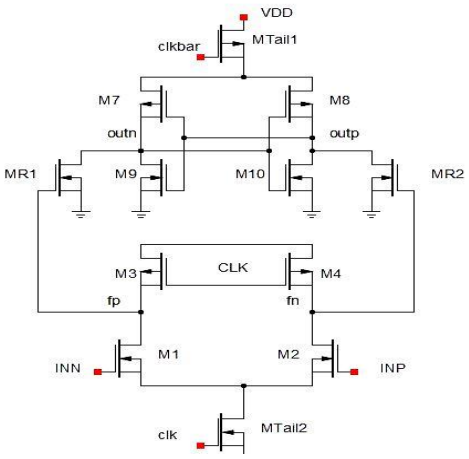

Fig. 4: Schematic of Conventional Double Tail Dynamic Comparator

D. Modified Double Tail Dynamic Comparator

The comparators with double tail structures give betterperformance in low power applications. The schematic of theproposed double tail comparator [2] is shown in the Fig. 12. Inthe reset phase, when the clk is low, the transistors Mtail1 andMtail2 turned off and this process helps to reduce the staticpower consumption. The transistor M3/M4 turned on, fp and fnnodes pre charged to VDD. The control transistors MC1 andMC2 are turned off. Now the intermediate transistors MR1 andMR2 pull the output nodes to the ground potential. In theregeneration phase, when the clk goes high, Mtail1 and Mtail2 getturned on and make the fp and fn nodes discharge at differentrates depending on the inputs. The switching transistors SW1,SW2 are used to avoid the common mode voltage problems. The switching transistors make the control transistors toincrease their voltage difference. If the clock frequency is increased then the speed of the comparator is also increases.

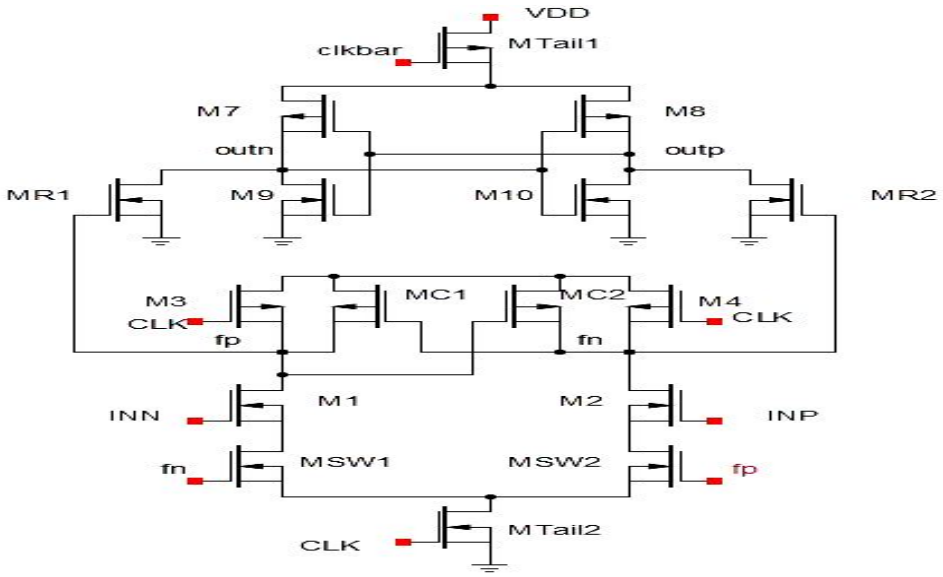

Fig. 5: Schematic of Modified Double Tail Dynamic Comparator

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III. PROPOSED LOW VOLTAGE DYNAMICCOMPARATOR

The schematic of the proposed ultra low voltage body driven comparator, is shown in the figure Fig. 5. Theoperation of the comparator is as follows. In reset phase, clk ishigh and Mtail is off, transistors M5 and M6 reset both theoutput nodes to ground. The input voltages are applied to thebody terminal of the transistors (INN and INP). In thecomparison

phase, clk is low, transistors M5 and M6 are offand Mtail is on and the output nodes outp and outn gets chargedwith different rates depending on the inputs. When INP>INN,outp is charged faster than outn. The cross coupled invertersM3 and M4 initiate the regeneration phase when outp ischarged to threshold voltage of M4. When M4 turns on, it willPull the outn to ground potential. Therefore outp is charged to VDD and outn discharged to ground.

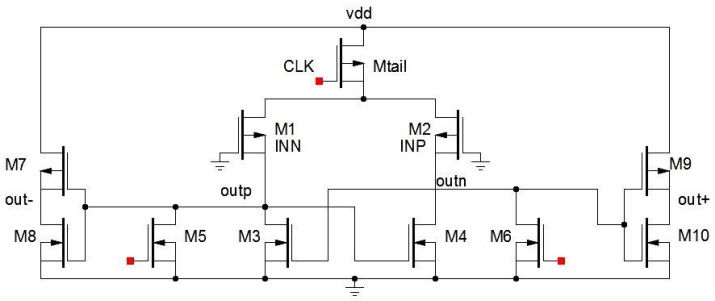

Fig. 5: Schematic of Proposed body driven Dynamic Comparator

A. *Design Considerations:*

- Accuracy (offset, noise, resolution)
- Settling time (tracking BW,regeneration speed)
- Sensitivity (gain)
- Metastability (any decision isbetter than no decision!)
- CMRR
- Power consumption

B. *Power Estimation Techniques*

The power estimation design technique for low power problem cannot be achieved without accurate power prediction method and optimization tools or without power efficient gate technology. Therefore, there is a critical need for software analog design tools for virtually calculate the power of circuit or estimate power dissipation during the design process to meet the power budget without having to go through a costly redesign effort and enable efficient hardware design and characterization of the design libraries. Various techniques for power estimation at the circuit, logical level and behavioural levels will be reviewed. These techniques of power estimation are divided into two categories, simulation based and non-simulation based. These technique of simulation applied on the design before hardware design of that circuit for measuring different parameter like power, offset voltage and propagation delay.

C. *Power Minimization Techniques*

To address the challenge to reduce power consumption in circuit design, mainly four factor works.

i. *Reducing chip capacitance and and package capacitance:* This factor of reducing chip and package capacitance can be achieved through development process like SOI with fully depleted wells or partially depleted wells, CMOS circuit scaling to submicron device sizes, and advanced substrates are interconnected such as (MCM) Multi-Chip Modules process. This approach of simulation based calculation can be very effective but it is also very expensive and has its own place of development as well as introduction to the market segment.

ii. *Scaling supply voltage*: This approach of scaling supply voltage can be very effective in reducing the power dissipation circuit design, but itrequires new(integrated circuit) IC fabrication process - ing. This Supply voltage

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scaling also requires a suppotring circuitry for lowvoltage operation including DC/DC converters and level-converters.

iii. Better design techniques: The designing approach of circuit is very efficient or to be very successful because the investment to reduce power by designing technique is relatively small compared with the other three approaches of circuit design and because it is relatively untapped in potential.

iv. Power management strategies used: One of the another power estimation technique used is power management strategies. The power savings that can be achieved by various static power and dynamic power management techniques are used and all these are very application dependent factor , but can be significant.

IV. CHALLENGES IN LOW POWER DESIGN

The basic need for lower power systems is being driven by many market segments. There are many no. of approaches that can be used to reducing power consumption is discussed above. Unfortunately designing for low power circuit another dimension in circuit to the already complex design problem; the design has to be optimized by mainly three parameter for Power, Performance and Area. To conclude this discussion, to summarize the major challenges is that, we have to be addressed if we want to keep power dissipation within this bounds in the next generations of the designing of digital integrated circuits.

• A low supply voltage and circuit design technique, targeting the supply voltages are taken around 1 Volt or lower than 1V and operating with reduced thresholds voltage.

• Low power interconnect, using reduced activity or advanced technology, reduced swing approaches.

• Dynamic power management techniques, are varying with the supply voltage and the execution of design speed according to activity measurements. This can be achieved by the whole design should be divided into sub-circuits whose energy levels also can be independently controlled and by powering down sub-circuits which are not in used.

V. SIMULATION RESULTS

The simulation studies involve, In Fig. 6. [10]the delay analysis for different comparators has been analyzed with respect to supply voltage.The proposed body driven comparator is shown in the Fig. 16 [10] which is chosen for low voltage operation and this comparator provides the maximum sampling frequency of 0.33GHz in 90nm CMOS and V_{DD}=0.5V.

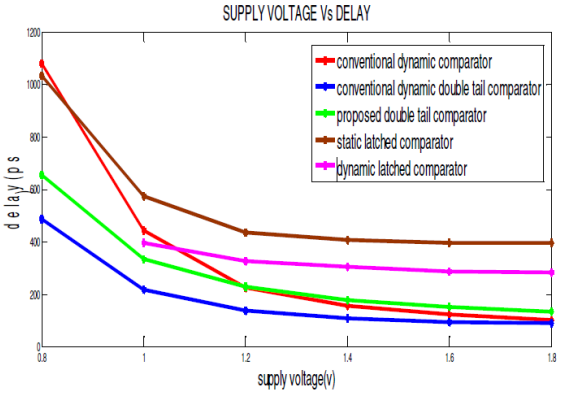

Fig. 6. Comparison of different comparators

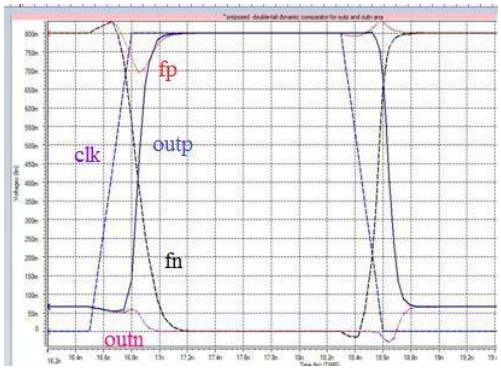

Fig. 7.Simulation of proposed body driven Dynamic Comparator

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V. CONCLUSION AND FUTURE WORK

In this paper offset parameter and limits of the low power comparator designtechniques have been provided and alsodiscussed about sources of power,estimation and reduction method of power.The comparator action depends uponvarious factors like power supply,technology area etc. However of variousthings our aim is to achieve a low powerdesign so compromise with other factors isto be made. In next, we will present the implementation and comparison of proposed body driven dynamic comparator. Also we will further reduce the size of this comparator in terms of transistor count so as to reduce area and propagation delay and increase the speed.

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