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Review on High Speed Convolution and Deconvolution Algorithm Using Indian Vedic Mathematics

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ABSTRACT*:*To implementing convolution and deconvolution the basic blocks are multipliers and a divider is used. The main purpose is to improve the speed of the digital circuits like multiplier. The multiplier and adder are the important in digital signal processors, microprocessors and filters etc. So we always try for a high speed multiplier that increases the performance as well as the efficiency of the system. In this paper, Vedic multiplier based on Urdhva-Tiryagbhyam algorithm multiplier architecture is used. The conventional methods such as graphical, novel shift and add methods etc. are time consuming compared to proposed methods. UrdhvaTiryagbhyam, Nikhilam sutra are used for multiplication and division purpose. It requires less time, power and gives results faster.

KEYWORDS: Convolution, Deconvolution, Vedic multiplier, Urdhva-Tiryagbhyam, Nikhilam.

I. INTRODUCTION

For the new candidate it is quite difficult to perform convolution by simple convolution method is prolonged and consumes so much time. For performing Discrete Convolution so many methods are proposed, one of a tough approach is a Graphical method [1] it is quite sophisticated and systematic but, it is very lengthy and time consuming. The paper presents a direct method. Direct method is used for computing the discrete linear convolution, circular convolution and deconvolution and the main purpose of the proposed method is to develop a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhva-Triyagbhyam and Nikhilam algorithm [2]. The implementation of linear convolution and circular convolution using Vedic mathematics is more efficient in terms of area and speed.

II. LITERATURE REVIEW

This paper describes a method how to compute the discrete linear convolution, circular convolution and deconvolution [2]. The approach is easy to study because of the similarities to computing the multiplication of two numbers and the proposed method is used for developed a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras. The result is efficient in terms of area and speed compared to conventional multiplier & divider architectures.

This paper, gave very easy and simple method for DSP operation for small length of sequence the importance of multiplication in DSP operation e.g. correlation [3]. The proposed algorithm is implemented in MATLAB and the author performed all the operations on single Graphical User Interface (GUI) window. It reduces the 40-60% processing time from inbuilt function.

This paper**,** describes a method of two finite length sequences that is implemented using direct method to reduce deconvolution processing time [4]. The performance of the circuit has a delay of 84.262 ns from input to output. Since 4×4 bit multiplier is need of this project. This design approach is efficient in terms of area. Division operation is implemented by using Non-restoring division algorithm while to obtain partial products Vedic multiplier is used. For parallel hardware implementation delay is about 17 ns.

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This paper, proposed a multiplier accumulator unit (MAC) [5]. The multiplier used in MAC is based on Vedic mathematics sutra Urdhva-Tiryagbhyam. Approach is good for digital signal processing because it requires less power. The outcome of the proposed method is efficient as compared to modified booth Wallace multiplier.

FFT architecture needs multipliers to be implemented [6], if multipliers are made faster enough, the processing speed of FFTs can also be increased which means many applications in digital signal processing can be processed with high speed. By using ancient Vedic mathematical formulae (sutras) this can be done. The result shows that the multiplier based on Vedic sutras had execution delay of almost half of that of binary multiplier (partial products method).

This paper, investigates new multiplier and square architecture based on algorithm of ancient Indian Vedic Mathematics, applicable for low power and high speed applications [7]. It generates all partial products and their sums in one step. The result shows that the Vedic multiplier is faster than other multiplier.

This paper, proposed a high performance, high throughput and area efficient architecture for the convolution [8]. The multiplier architecture is based on Vedic mathematics sutra Urdhva-Tiryagbhyam and uses OLA and OLS methods. The coding is done in VHDL. The execution time for block convolution using FPGA reduces from 0.12s to 36.85ns. Also the result shows that the designs are efficient in terms of area and speed.

III. CONVOLUTION USING VEDIC MULTIPLIER

Convolution is the arithmetical way of combining two signals to obtain a third signal. Convolution helps to calculate approximately the output of a system. In this section, novel multiplier architecture [9] based on Urdhva- Triyagbhyam Sutra of Ancient Indian Vedic Mathematics is surrounded into proposed method of convolution to improve its efficiency in terms of speed and area[2].

In this paper a systematic Vedic multiplier using Urdhva-Tiryagbhyam sutra is used for multiplication. Among all multiplier faster multiplication performs using Vedic multiplier and required less area. In the proposed convolution method the Multiplier is based on Urdhva- Tiryagbhyam (vertically and crosswise) [9]. Urdhva-Tiryagbhyam is general multiplication formula applicable for all types of multiplication [10]. In this algorithm the small block can be used for designing NxN multiplier. For higher no. of bits little change is necessary. So first divide the no. of bit in the inputs equally in two parts. Let's analyze 4x4 multiplications, say U3U2U1U0 and V3V2V1V0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide U and V into two parts, say U3U2&U1U0 for U and V3V2&V1V0 for V. Using basic of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication as shown [13].

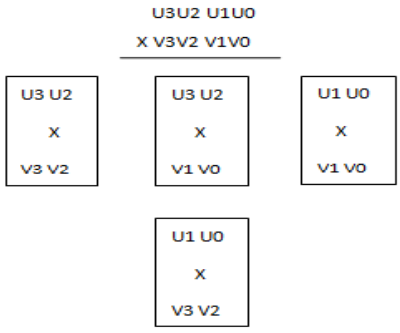

Fig.1 Block Diagram presentation for 4X4 Multiplication

Each block as shown in above fig.1 is 2x2 multiplier. First 2x2 multiplier inputs are U1U0 and V1V0. The last block is 2x2 multiplier with inputs U3U2 and V3V2. The middle one shows two, 2x2 multiplier with inputs U3U2 and V1V0 and U1U0 and V3V2. So the final result of multiplication (8 bit), S7S6S5S4S3S2S1S0, can be written as given below.

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U3U2	U1U0	U1U0	U1U0
V3V2	V1V0	V3V2	V1V0
S33S32S31S30	S23S22S21S20	S13S12S11S10	S03S02S01S00

Assuming the output of each multiplication is as given above [2] Add the middle term along with the term shown below, for the final result.

P33	P32	P31	P30	0	0	P01	P00
		P23	P22	P21	P20		
		P13	P12	P11	P10		
		0	0	P03	P02		

The first two outputs P0 and P1 are same as that of P00 and P01. Add the middle terms and add the result of middle terms two, 4 bit full adders will forms output line from P5P4P3P2. One of the full adders will be used to add (P23P22P21P20) and (P13P12P11P10) and then the second full adder is required to add the result of 1st full adder with (P31P30P03P02). The respective sum bit of the 2nd full adder will be P5P4P3P2. Now using half adder add the carry generated during operations of 1st full adder and 2nd full adder. So the final carry and sum to be added with next stage i.e. with P33P32 to get P7P6. The same can be extended for input bits 8, 16, 32 [2].

IV. CIRCULAR CONVOLUTION

Circular convolution is easily modified from above part. This method of computing circular convolution is best illustrated by example. Let X(n) = (1 2 3 0) and Y(n) = (2 4 5 1). The circular convolution of X(n) and Y(n) is given by

$$Z(n)= X(n)*Y(n)$$
$$Z(n)= \sum_{k=0}^{N-1} X(n)Y(n-k)mod(N)$$

Y (n) = (23 19 11 19) where N is the length of the sequences. This circular convolution calculation is same as that of linear convolution from above part. The multiplier architecture is implementing using Vedic algorithm. The location of the triangle of bold faced numbers is repositioned for circular convolution compared with linear convolution [14]. The far left value in the circular convolution solution corresponds to y (N - 1) where N is the length of the sequence [2].

1	2	3	0
X 2	4	5	1
1	2	3	0
10	15	0	5
12	0	4	8
0	2	4	6
23	19	11	19

Fig. 2 Circular Convolution by proposed method

V. DECONVOLUTION USING VEDIC DIVIDER

Nikhilam algorithm which is based on Vedic mathematics is used for Division operation. To obtain partial products Vedic multiplier is used. The Nikhilam sutra goes as follows:

Nikhilam Navatascaramam Dasatah, that means all from 9 and the last from 10 [6]. To describe this method by an example as follows (123/8),

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Fig. 3 Deconvolution by proposed method

In this method the first line shows denominator followed by its 10's complement (2 is 8's 10's complement) and numerator is divided by"|" such that there are many digits to the right of the"|" as there are digits in the denominator [2]. First put a zero under the first digit of the numerator. Then add the digits in that column of the numerator to get a sum of 1(1 + 0 = 1). Now multiply it by the 10's complement to get 2 (1 x 2 = 2) and put that answer under the second digit of the numerator and then add the digits so we get the 4 in second column. By multiplying this by the 10's complement get 8 and put that 8 under the third digit of the numerator, right of the"|". Now add all the numbers under the columns. There is no carry from the right of the"|" to the left of it. This method is extended for other numbers also. Nikhilam division algorithm just involves the addition of numbers which is very much different from the traditional division technique including multiplication of big numbers by the trial digit of the quotient at each step and subtracts that result from dividend at each step [11].

VI. CONCLUSION

The main focus of this paper is to establish a method for calculating the linear convolution, circular convolution and deconvolution using Vedic algorithms that is easy to learn and perform. Also circular convolution using Vedic multiplier introduced which has less delay and area than the conventional method and also introduced a simple approach to performing the deconvolution.

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