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NEM Relay Based Low Power Design

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ABSTRACT: Today's integrated circuit designs are equally limited by the dynamic and leakage power components halting the trend of further supply scaling. A device with a steeper sub-threshold slope is needed in order to continue the scaling trends beyond those of CMOS technology. One such device is a Nano-electromechanical (NEM) relay consisting of an electrostatically actuated beam that can be positioned to either allow conduction between the source and drain or leave them open-circuited. Because a physical connection determines conduction, relay devices can achieve zero off current and effectively an infinite sub-threshold slope. However, unlike CMOS technology where delay is largely set by the charging and discharging of capacitances, the mechanical motion of the actuated beam largely dominates the delay of relay-based circuits. The zero leakage operation has generated lot of interest in low power logic design using these relays. A NEM-relay device is modelled using cadence virtuoso platform and its characteristics where discussed. An inverter is constructed and compared using both NEM relay and CMOS. Also a Weak Conditioned Half Buffer, a circuit commonly used in asynchronous communication, is implemented using NEM-relay as an example for a complex circuit.

KEYWORDS: NEM Relay, low power, Verilog-A

I. INTRODUCTION

Over the past decades, CMOS technology scaling has been the dominant driver in improving energy efficiency of transistors. As the voltage supply is decreased, dynamic energy consumption decreases. Since the scaling of voltage supply results in reduced source-drain currents, the threshold voltage needs to be scaled accordingly as well to avoid any performance penalty. However, decreasing the threshold voltage inevitably increases the leakage currents and we have already reached a point where CMOS technology scaling is no longer sufficient to reduce power consumption..

In the era of mobile and wearable computing, power consumption of electronics is a pressing challenge in designing increasingly smaller battery-operated devices. New methods in architecture, circuit design, devices and materials must be adopted to continue lowering power consumption. More parallel and less high-performance circuit architectures are emphasized, resulting in a shift to multicore computing within the last decade. Alternate technologies must be explored to replace CMOS [1].

NEM relays are a very energy-efficient alternative to CMOS. It consisting of an electrostatically actuated beam that can be positioned to either allow conduction between the source and drain or leave them open-circuited. Because a physical connection determines conduction, relay devices can achieve zero off current and effectively an infinite sub-threshold slope.Numerous NEM relay implementations have been proposed recently that show significant energy efficiency improvements over CMOS circuits while operating at low frequencies. A cantilever beam based NEM relay has been reported in [2], which has been further improved to a suspended gate NEM relay in [3]. A laterally actuated NEM relay device is reported in [4] in which a poly-silicon beam is laterally actuated to realize the mechanical switch. Carbon-nanotube based NEM relays are reported in [5]. Even though this work is based on suspended gatebased NEM relays, the concept can be extended to any relay technology that provides parallel plate capacitances.

In this work a NEM relay device is modelled including its electrical as well as electro-mechanical behaviour and its various characteristics where analysed. As a comparison, an inverter circuit is constructed using both NEM-relay and CMOS. Also a Weak Conditioned Half Buffer (WCHB) is constructed as an example of complex asynchronous circuit.

The rest of the paper is organized as follows. Section II introduces the NEM relay device, its structure and definition of relay parameters.Section III explains the Verilog-A model of the NEM relay that has been used in this

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work. Section IV describes how NEM relay can be used for circuit implementation. Also inverter and WCHB circuits were implemented in this section using NEM relay and compared with that of CMOS as examples.Section V concludes the paper.

II. BACKGROUND

A. Structure of NEM Relay

A NEM relay is an electrostatically actuated mechanical switch whose state of operation is set by the voltage difference between a movable gate terminal and a fixed body terminal. Figure 2 shows the cross-sectional and top views of this device. The cantilever gate electrode attaches to the metallic channel via an insulating gate dielectric (cross-sectional view). In the off state, where the gate to body voltage ($|V_{gb}|$) is less than a characteristic "threshold" voltage (V_{th}), an air gap separates the channel from the metallic source and drain. Since there is no path for current to flow, I_D=0. In the on state, where $|V_{gb}|>V_{th}$ electrostatic force is sufficient to bend the cantilever gate enough that the metallic channel comes into contact with the source and drain, allowing for current to flow. Since the device exhibits no leakage current and experiences an abrupt turn-on, it has an extremely steep effective sub-threshold slope.

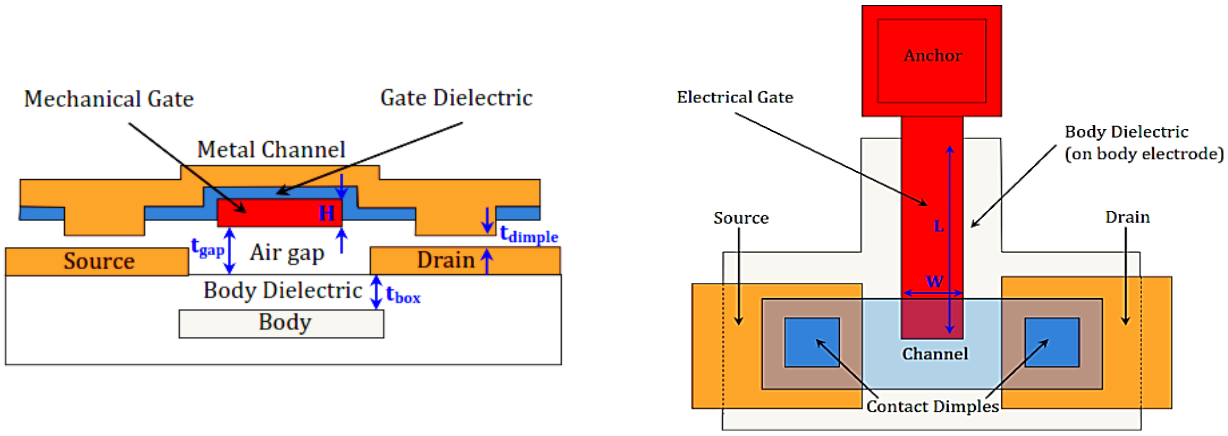

Fig. 2. Cross section and top views of NEM Relay

B. Definition of NEM Relay parameters

Pull-in voltage V_{pi} is the voltage applied between gate and base above which the electrostatic force overcomes the spring-mass-damper system and the relay turns ON. Release voltage V_{rl} is defined as the voltage below which the relay opens and the switch is OFF. The NEM relay exhibits a hysteretic property for the pull-in and release threshold voltages. The pull-involtage (V_{pi}) is larger than the release voltage (V_{rl}) as inFigure 3. The mechanical delay involved

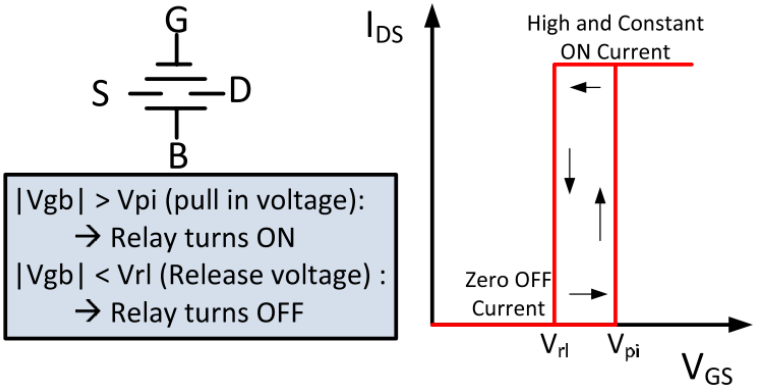

Fig.3. NEM Relay Symbol and voltage transfer characteristics

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in switching ON the relay is denoted as t_{mon}.

The mechanical delay involved in switching OFF the relay is denoted as t_{moff}. The mechanical delay is an order of magnitude larger than the electrical delay of the relay (t_e). As an example, the mechanical delay of the suspended gate relay used in this work is of the order of hundreds of nanoseconds, whereas the electrical delay is of the order of tens of picoseconds.

III. VERILOG-A MODEL OF SUSPENDED GATE RELAY

As we describe next, these basic equations were used to develop the Verilog-A model for the 4-terminal relay, and this model was used to enable the subsequent simulation study of NEM relay circuit design and energy-performance characteristics.

A. Beam Dynamics and Relay Threshold Voltage

The gate cantilever beam can be modeled as a linear spring-damper–mass-system, as shown in Fig4. Although this lumped electro-mechanical model is clearly simplified, it provides useful insight for switch design and has been previously shown to closely match experimental results [2].Using this simplified model, the dynamics of the motion of the gate can be described by the equation*:*

$$m\ddot{x} = F_{elec} - b\dot{x} - kx \qquad eq.(1)$$

where*x* is the displacement of the beam from its nominal position, *b* is the linear damping factor caused by the displacement of air molecules and anchor losses, *m* is the mass of the beam, and *k* is the spring constant of the beam.

For a beam of width *W*, thickness *H*, and length *L*, the mass of the beam *m* is equal to ρWHL, where ρ is the density of the beam material. Similarly, the spring constant is $k=\gamma EW(H/L)^3$, where γ is an empirical constant equal to ~0.25 for a cantilever, and *E* is the Young's modulus of the beam material.

The relay is actuated by placing a voltage V_{gb} across the gate-to body capacitanceC_{gb}, which can be expressed as:

$$C_{gb} = \frac{\varepsilon_0 WL}{d_{eff} - x} \qquad \text{eq.(2)}$$

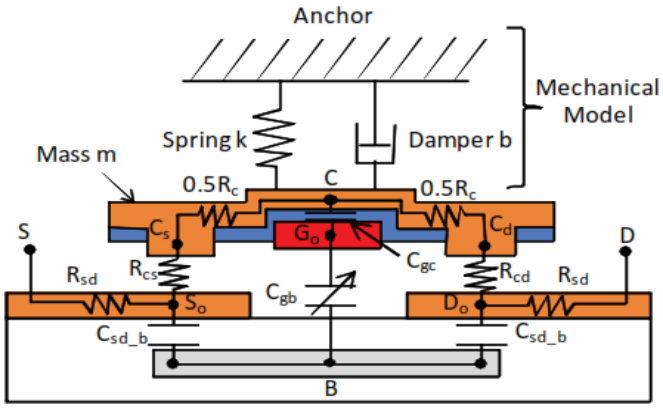

Fig.4.Relay circuit model implemented in Verilog-A

Here, d_{eff} = t_{gap}+(t_{gap}/ϵ_{box}) where t_{gap} and t_{box} refer to the physical thickness of the air gap and the body dielectric thickness, respectively, and ϵ_{box} is the relative permittivity of the body dielectric. In order to reduce the beam travel distance and hence the mechanical delay of
the switch, the 4-terminal design employs a smaller air-gap of thickness t_{dimple} in the source/drain contact regions. The electrostatic force F_{elec}resulting from V_{gb} attracts the gate towards the body, and is equal to:

$$F_{elec}=\frac{\varepsilon_0 (WL) V_{gb}^2}{2(d_{eff} - x)^2} \text{eq.(3)}$$

While the electrostatic force increases quadratically with increasing displacement, the spring restoring force $F_{spring}=kx$(which counteracts the electrostatic force) increases only linearly with displacement. Hence, by setting the

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dynamic terms in (1) to zero, it can easily be shown that there is a critical displacement equal to $d_{eff}/3$ beyond which F_{elec} is always larger than F_{spring}, causing the gap to close abruptly. This critical displacement has a corresponding value of $|V_{gb}|$ known as the "pull-in" voltage V_{pi}:

$$V_{pi} = \sqrt{\frac{8\gamma E H^3 d_{eff}^3}{27\varepsilon_0 L^4}} \quad \text{eq.(4)}$$

As it will impact the I/O circuits described in Section IV, it is important to note here that a relay exhibits hysteretic switching behavior, so that the value of $|V_{gb}|$ required to switch the device *off* can be significantly smaller than the value required to switch it *on*. This is especially the case if the relay is operated in pull-in mode, i.e. if $t_{dimple} > d_{eff}/3$. Simply, once the relay has been pulled-in, the effective gap is smaller than $d_{eff}/3$, making F_{elec} unconditionally larger than F_{spring} at significantly lower $|V_{gb}|$. It is important to note that this hysteresis voltage is also directly impacted by surface forces; since the hysteresis voltage sets a lower limit for V_{dd}, these surface forces should be minimized.

Note that if t_{dimple} is less than $d_{eff}/3$ (i.e., the relay is not operated in pull-in), then V_{th} is less than V_{pi}. Nonetheless, V_{pi} sets an upper limit for the gate-to-body voltage required to turn on the relay, and thus in this paper we will use $V_{th} = V_{pi}$ as a conservative estimate. As can be seen from Equation (4), V_{pi} is a strong function of the beam length. Since the beam length is set lithographically, circuit designers can directly tune the threshold voltage of the device. Due to the relay's abrupt turn-on behavior and the fact that it does not exhibit any leakage current (as long as the contact dimple gap is greater than ~2 nm to avoid significant direct tunneling), the threshold voltage and hence the supply voltage can both be reduced to minimal levels to improve energy efficiency. The minimum $V_{th}$for a given relaytechnology is set by the requirement that the spring restoring force is able to overcome surface forces.

B.Parasitic Resistances and Capacitances

Since the relay is electrostatically actuated, its input impedance is largely capacitive in nature (like a MOSFET). In the *off*-state, the input capacitance of the relay is dominated by the gate-to-body capacitance C_{gb}. When the relay is in the *on*-state, the capacitance between the gate and the channel C_{gc}also appears directly as input capacitance:

$$C_{gc} = \frac{\kappa_{gateox}\ \varepsilon_0 (W L_{channel})}{t_{gateox}} \quad \text{eq.(5)}$$

wheret_{gateox} and κ_{gateox} are the physical thickness and relative permittivity of the gate dielectric, respectively, and $L_{channel}$ is the length of the overlap between the gate and the channel.

The *on*-resistance (R_{on}) of the 4-terminal relay is the sum of the source/drain resistances ($2R_{sd}$), the channel resistance (R_c), and the channel-to-source and channel-to-drain resistances (R_{cs} and R_{cd}, respectively). The electrode resistances can be simply approximated as:

$$R_{sd} = \rho_{sd}\frac{L_{sd}}{H_{sd}W_{sd}} \text{and } R_{ch} = \rho_{ch}\frac{L_{ch}}{H_{ch}W_{ch}} \quad \text{eq.(6)}$$

where the symbols ρ, *L*, *H*, and *W* represent the sheet resistance, length, thickness, and width of the electrode. The values of these electrode resistances are obviously highly material dependent. However, since these electrodes are all metallic, and since the electrodes intrinsic to the device can be relatively short, these resistances are typically very small (~1 Ω or less).

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C. Electromechanical Section Implementation

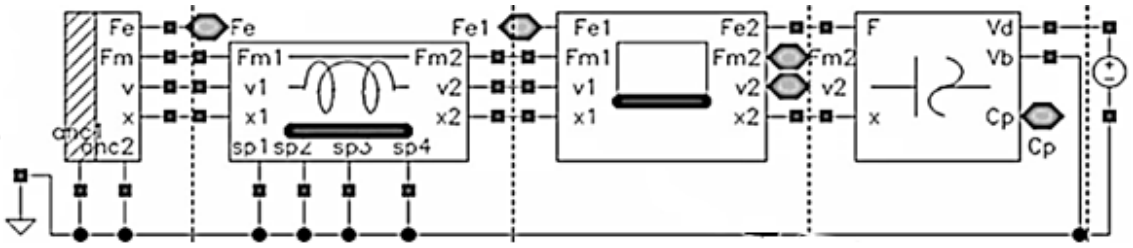

Fig. 5. Electromechanical system sub modules

The analytical model has been translated into an equivalent circuit model in the Cadence Virtuoso environment to find a displacement value as a function of the applied voltage as shown in figure 5. Module I is a sub-circuit model for the parallel-plate electrostatic actuator, and it has been designed to calculate the electrostatic force as current output as a function of drive voltage(s). Module II is for the viscoelastic suspension to calculate the restoring force as electrical current output. Module III, which has been inserted between the viscoelastic suspension and the electrostatic actuator, is the EOM co-solver to calculate the velocity and the displacement x as function of the impinging electrostatic and restoring forces. Module IV is the mechanical anchor.

We used Verilog-A, which is an HDL that can handle various mathematical operations, including derivation and integration as well as logical expressions such as an if–then–else clause. It also has versatility of defining the input and output ports in either the electrical current and voltage modes. Apart from our previous publications, in which we used cascaded electrical capacitors to analog compute the second-order integral equation, Verilog-A description can be placed in a more straightforward manner by using mathematical expressions. For instance, electrical current I is written as a derivation equation of charge q as

$$I = ddt(q) \qquad \text{eq.(7)}$$

whereddt is a mathematical function of Verilog-A for temporal differentiation, which is useful to describe a current flowing in and out from an electrical capacitance. Also, integration is used to calculate mechanical displacement (as voltage V) from velocity (as current i) as

$$V = idt(i,i_c,y) \qquad \text{eq. (8)}$$

whereidt is another Verilog-A function for temporal integration. Parameter y is a programmable logical condition to force the output value reset to ic when the conditional y is fulfilled. We define mechanical force and velocity as electrical current and voltage, respectively, following the analogy between mechanical and electrical systems [8].

Parallel Plate Module: This module is used to calculate the electrostatic force acting on the gate beam. Since the electrostatic force is a function of potential difference between gate and body, the module receives three inputs-gate potential (V_g), body potential(V_b) and the position of the beam(x). The force is given as output current through the terminal F. The capacitance between gate and body is also calculated.

EOM module: EOM module calculates the actual position and velocity of the electrostatic beam. It receives the electrostatic and restoring forces as input current. From Newton's relation, **F=ma**, acceleration of beam can be calculated. By integrating the acceleration using idt function in Verilog-A, velocity can be find out. One more integration gives the beam position. The values of displacement and velocity can be read out as voltages.

Viscoelastic suspension module: The sum of the elastic restoring force and the viscosity friction is calculated from the displacement and velocity given by EOM module. The spring constant, k of the viscoelastic suspension module is

$$k = 4Y_g w_k \left(\frac{t_k}{l_k}\right)^3 \text{ eq. (9)}$$

Anchor module: Anchor module is used to give a mechanical constraint to the suspension by pulling down the displacement and velocity ports to null (GND). A virtual resistance of a finite value, i.e., 1Ω, is set between the GND and the anchoring port; this resistor does not affect the computation accuracy but isused due to the requirement of Verilog-A protocol. The resistor also works as a terminator for the suspension module, by draining the restoring force imprinted onto the electrical current [8].

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IV. CIRCUIT DESIGN USING NEM RELAY

Since NEM relays can be made complementary with the appropriate choice of body voltage, many of the logic styles used in CMOS can be directly extended to relay-based designs. However, the electrical characteristics and behavior of NEM relays are significantly different than that of CMOS transistors. Thus, as we will describe next, an optimized relay-based design will make use of gate and logic network topologies very different from the same logic function optimized for a CMOS implementation.

Following are some interesting properties of NEM relays that can be used in relay based logic design:

1) I-V Characteristics

The sub-threshold slope of CMOS as well as that of NEM Relay are shown in the figure 6. Clearly NEM Relay has abrupt sub threshold slope results in zero leakage current. Hence only dynamic power consumption is present for NEM relay, which can be reduced by scaling power supply.

2) As Switch

A relay can be turned on by applying a positive or negative V_{GB} beyond V_{pi}, i.e. the relay turns on for $|V_{GB}|>V_{pi}$. Thus, the same relay can be operated as an "NMOS" or a "PMOS" transistor by biasing the body node at 0 or V_{DD}, respectively.At same time independent of CMOS, both N-relay and P-relay can conduct a good zero as well as a good 1. So a NEM relay is much suited for pass transistor logic implementation that requires minimum number of transistors.

3) $t_{moff}<t_{mon}$

Due to the hysteretic property of relays as explained, there is an asymmetry in the on/off mechanical delay through the relay and this asymmetry can be used to eliminate simultaneous conduction thereby mitigating short circuit current.

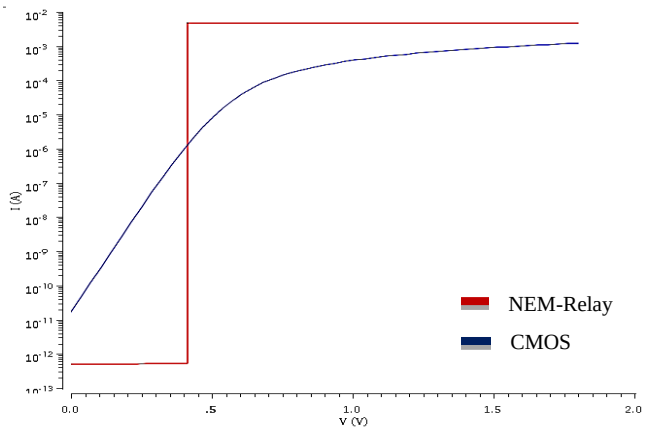

Fig. 6. I-V Characteristics

4) Intrinsic capacitance

A true parallel plate capacitor exists between gate and base (C_{gb}) in both the cantilever beam relay and the suspended gate relay. The small overlap area between gate and source/drain also creates small parallel plate capacitances C_{gs} and C_{gd}. It is reported in [6] that $C_{gb}$is of the order of 1-2fF and contributes ~ 60% of the total relay self-capacitance. The relay based DRAM design shown in [6] uses the intrinsic capacitor to store the charge in the bit cell. Due to the near zero leakage in the relay, charge stored in these capacitances is retained very efficiently.

5)Mechanical Delay

Optimized relay logic can be designed by understanding that the relay's mechanical motion dominates its delay. Due to this dominance, unlike traditional CMOS logic design in which gates are cascaded to construct more complex functions, an optimized relay design arranges for all mechanical motion to occur simultaneously. In other words, each cascaded relay gate on a given path would incur an additional mechanical delay and thus, relay-based designs should instead use a single, large complex gate to implement logic. Figure 8 shows an example.

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Although this design style ensures minimal mechanical delay, each extra series relay increases the electrical delay quadratically because both the path resistance and the capacitance increase. Although many series relays are required for the electrical delay to approach the mechanical delay, it needs to be taken into consideration should the design become very complex.

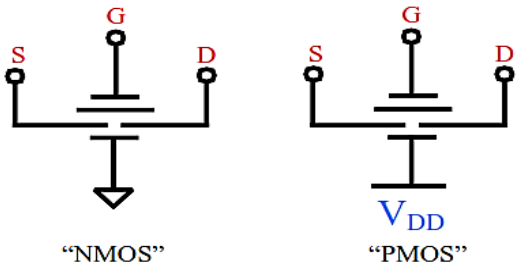

Fig. 7. Relay switch as an NMOS and PMOS

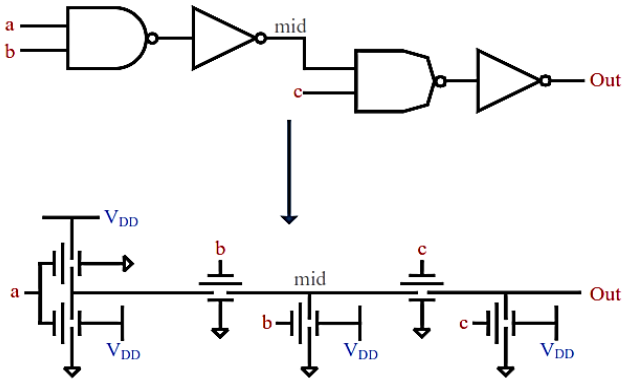

Fig. 8. Logic Implementation using NEM Relay

A.NEM Relay inverter

Unlike circuits built with emerging devices that are stillessentially field-effect in nature, relay-based circuits are implemented in a significantly different fashion than CMOScircuits. Thus, any comparisons between the energy-performancecharacteristics of CMOS designs and NEM relay designs must bemade at the circuit level (rather than at the device level). Forexample, although the mechanical delay of a relay may besignificantly larger than that of a CMOS inverter, a completeCMOS logic block will typically require 10-20 gate delays,whereas the relay-based circuit may comprise of only a single stageand hence require only one mechanical delay.

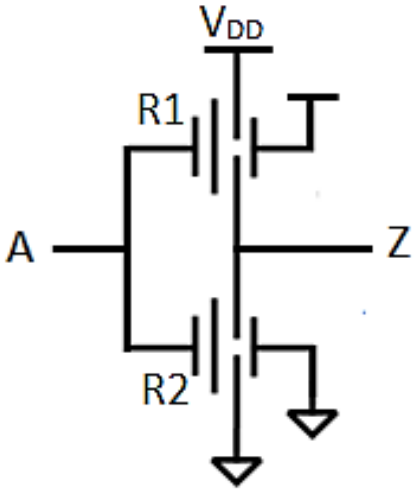

Fig. 9. NEM Relay Inverter

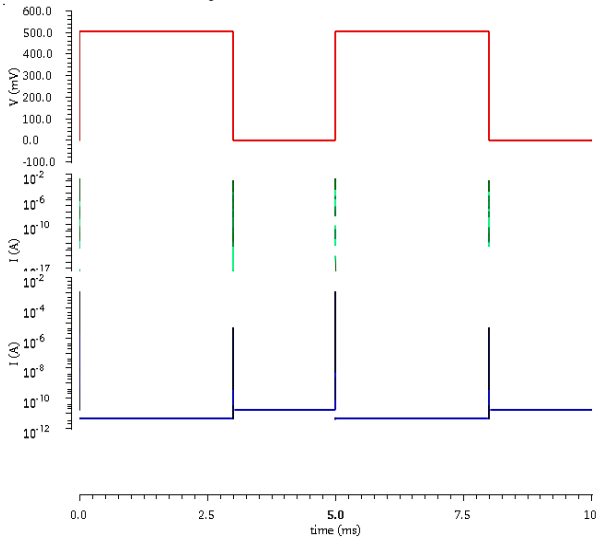

Fig. 10. Total power consumption

Consider an inverter circuit for comparison. Fig.9 shows a NEM Relay based inverter. The body terminal of relay R1 is connected to $V_{DD}$and hence it act as a P-relay. Similarly R2 act as N-relay since its body connecctd to GND. When input A is high, R2 turns ON due to the development of an electrostatic force across gate and body. R1 remains OFF since zero potential difference across its gate and body terminals. So the output Z will be connected to GND through R2 and obtain a low output. Similarly Z will be connected to V_{DD}through R1 when input is low.

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Table.1. Average power consumption

DEVICE	Technology	Power
NEM-Relay	180 nm	**790 E -12**
	90 nm	**230.1 E -12**
CMOS	180 nm	**405.2 E -12**

Figure 10 shows the total power consumption by NEM Relay and CMOS inverters with a 10pF capacitive load. For NEM Relay based inverter, the power consumption is only due dynamic activity. That is why power is shown only when the input switches. This dynamic power consumption can be reduced by scaling the power supply. But in the case of CMOS inverters, leakage power consumption is also present which is shown when input remains ideal at any one state. Table1 shows the average power consumption of both inverters derived from graph shown in figure 10. By technology what means here is that the minimum lithographically definable size. 180nm based relay is operated at 5V V_{DD} while 90nm Relay at 1.8V along with CMOS inverter. So the table conveys both less power consumption compared to CMOS as well as reduction in power with scaling of power supply.

B. Weak-Conditioned Half Buffer

NEM relay can be used to implement any complex digital just like CMOS.As an example a Weak-Conditioned Half Buffer (WCHB) is implemented.

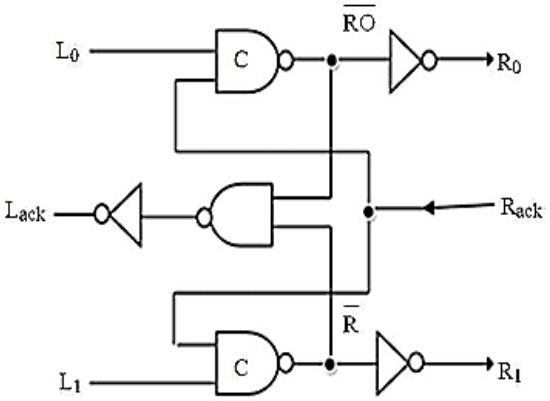

Fig. 11. WCHB circuit

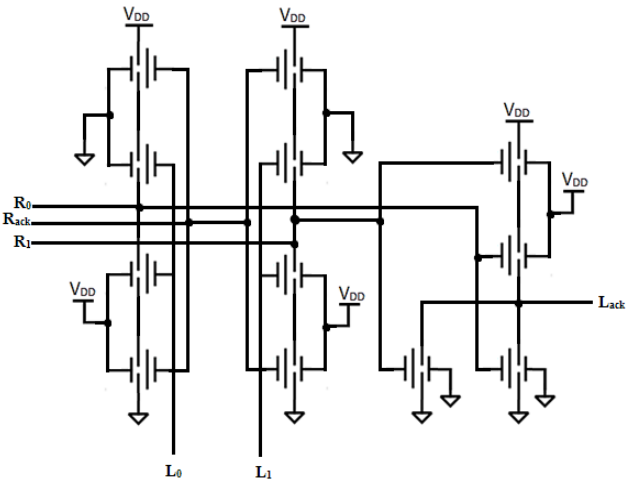

Fig. 12. WCHB using NEM Relay

An asynchronous communication channel is a bundle of wires and a protocol to communicate data between a sender and a receiver. The Quasi-Delay-Insensitive (QDI) model is a compromise to delay-insensitivity with the addition of isochoric forks. It allow signals to travel to many destinations and be acknowledged by only one. Isochoric forks are forks in wires where, if the acknowledging target has seen a transition on their end of the fork, then the transition is assumed to have happened on the other ends of the fork too. WCHB is an example for QDI communication The Figure 11 shows the template for Weak-Conditioned Half Buffer (WCHB). WCHB template with a Left (L) and Right (R) channel for a linear pipeline and an optimized WCHB dual rail buffer. The false and true dual rail inputs and outputs are L0 and L1, R0 and R1 respectively. Rack and Lack are active low acknowledgments signals. The operation of the buffer is as follows. The Buffer is reset, all data lines keep low and acknowledgment lines, Lackand Rack,are made high. When data comes from one of the input rails going higher, the respective C-element output will go low, lowering the left-side acknowledgment Lack. Once the data is propagated through inverters to the outputs, the right environment would assert Rack tolow, acknowledging that the data has been received. Once the input is reset, the template raises Lackand resets the output. Since two distinct token cannot be put into hold by L and R channel the circuit is said to be a half buffer or has stack ½.

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V. SIMULATION RESULTS

In CMOS, the WCHB has a forward latency of two transitions and a cycle time of 10 transitions. It is one among fast and popular implementation of buffer. On the other hand, WCHB implemented with NEM relays have a forward latency of one transition and a cycle time of 4 transitions. The ability of NEM relays to implementing non-inverting logic directly

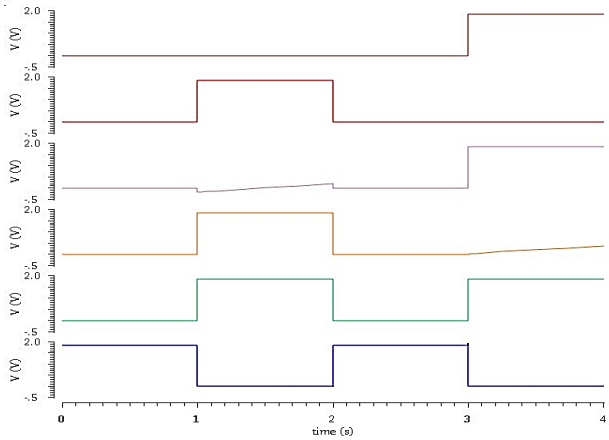

Fig. 13. Output waveform for WCHB

allow it to achieve the minimal possible number of transitions. Figure 12 shows a NEM relay implementation of the WCHB with 1-bit input (L) and 1-bit output (R). The number of relay required is 12 while at least 18 PMOS or NMOS transistors are required in the case of CMOS implementation. It also shows another advantage. The zero leakage property clearly contribute to low power [1].Fig. 13 shows the output waveform of the WCHB circuit.

Table 2. Comparison of WCHB using CMOS and NEM relay

Implementation	Forward Latency	Cycle time	No. of transistors
CMOS	2 transitions	10 transitions	18
NEM- relay	1 transition	4 transitions	12

VI. CONCLUSION

The sub-threshold leakage scaling causing, current CMOS designs to be limited by their total power consumption. An alternative switch with more ideal behaviour is therefore needed. The electrostatically actuated NEM relay is proposed to meet this need. A relay has zero leakage current because the source and the drain electrodes are physically separated in the off state. In addition, since on/off switching is based on making and breaking physical contact, a relay's switching characteristic is hyper-abrupt (sub-threshold swing (SS) is near zero), in contrast to a transistor's switching characteristic that is limited by the thermal voltage (*SS* = 60 mV/dec at room temperature).

In this work, a NEM relay device was modelled and observed its characteristics also observed how a NEM relay can act as an ideal switch. Finally, simple relay-based circuits are demonstrated to assess the viability of this technology for digital ICs. A complementary inverter circuit is characterized and compared with that of CMOS inverter. Also WCHB circuit implemented using NEM Relay

Since NEM relay can provide low power circuit operations, we can use such a device to implement highly complex embedded systems. As a basic we can think about microprocessors, controllers, FPGA and memory of NEM relay. It should be more advantageous if CMOS-NEM relay integration happens. We may hope for the beginning of a relay based low power era, which may not be far from now.

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