ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijircce.com

Vol. 5, Issue 6, June 2017

Low Power and High Speed CI_CSKA Design

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ABSTRACT: In consumer market for any portable application, low power is generally the mostdramatic issue.Adders form an almost obligatory component of every contemporaryintegrated circuit.In this paper, a high energy efficient Carry skip Adder (CSKA) is presented. The proposed structure of carry skip adder is able to achievevery high speed while maintaining the power consumption at a significantly low level. The proposed CSKA structure is appraised with the existing adder techniques by comparing their speed and power. These adder structures are analyzedusing VIVADO Design Suite, and Vivado® Synthesis tool is used to transform the design from RTL to gate-level netlist to implement it in a Xilinx® FPGA.

KEYWORDS: Energy efficient;Concatenation and Incrementation (CI) scheme; Carry Skip Adder (CSKA); Concatenation and Incrementation Carry Skip Adder (CI_CSKA); Hybrid Adder Structure; Parallel Prefix Network

I. INTRODUCTION

Higher speed and lower power consumption are the two main aspects one has in mind while starting to design a microprocessor. Arithmetic and LogicUnit (ALU) is one of major component in the microprocessor structure and completely responsible for the speed of the system functioning. By Reducing the time taken to perform the arithmetic operation one can increases the speed of processor. And main purpose of energy efficient design is to maximize the portable devices battery lifetime.

Several people have worked in this field to optimize the speed and power consumption of the adders and other arithmetic units i.e. subtractor, multiplexers etc.Some of the work which is carried out on addershas been reported in [1]-[3]. In literature we have several adder families/structures, having different speed, power and area requirement. One possible way to optimize these constraints is using these different structures. Examples of some families are Ripple Carry Adder (RCA), Carry lookahead Adder (CLA), Carry Skip Adder (CSKA) and Parallel Prefix Adders (PPAs). The characteristics and detailed architectural description of these familiesmay found in [1]-[5].

These structures are not just to minimize the total energy consumption by the system but also to minimize the time taken in each arithmeticoperation to increase the systemoperating speed. A power and area efficient adder is presented in [6], known as CSKA. Total path delay of the carry skip adder is much smaller than that of RCA and CLA. Area of CSKA is more compared to RCA and CLA, whereas its power delay product is less among the three.

II. RELATED WORK

Since the main focus of this paper is carry skip adder, we first review the prior work related to this adder structure. Then we will discuss the technique to improve the time and power specification for the same.

The conventional CSKA structure is made up of FAs chain and skip logic blocks. Skip logic consist logic gates and multiplexer. CSKA can be made in one or more level by placing the 2:1 multiplexer in different levels [7]. In the CSKA architecture number of full adders in each RCA block has significant impact on its speed [8]. [7]-[10] have proposed several methods to find the optimal number of full adders in each stage.

In [9] authors proposed a modified structure of CSKA.The proposed structurecombine concatenation and incrementation scheme that was used to increase the speed and enhance the energy efficiency of the adder.The use of CI scheme gives an opportunity to replace the multiplexer based skip logic by simple AOI/OAI compound gates. In The proposed structure of CI_CSKA, propagation of carry bit through the skip logics complement it. Therefore, at the output of theeven stages skip logic, the complement of the carry is generated. They have also proposed a hybrid

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variable latency adder based on the suggested carry skip adder. According to their equation total critical path delay time is proportional to the sum of (1) path delay of full adder chain (2) skip logic delay and (3) delay of the FA chain in last stage.

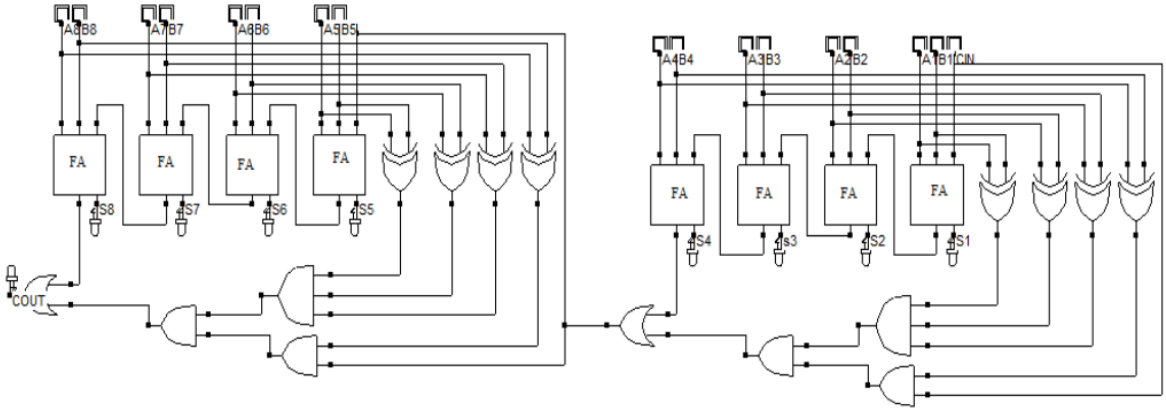

Fig.1. Schematic of 8-bit CSKA

Figure 1 shows the basic structure of the carry skip adder, which consist of FAs chain and some logic gates to determine the skip action. When carry bit has to propagate through all the FAs in that case ripple carry adder suffers from the worst case delay and the carry output is similar to that of input. It means that the delay will be proportional to the number of FAs in that chain. In the carry skip adder, skip logic is used to detect this kind of situationsand made the carry bit is available for the next stage instead of waiting for the computation of carry from FAs chain as in case of RCA. FAs in CSKA formed smaller group of FAs chain results in number of stages. Each stage contains an RCA block with skip logic. Carry output of FAs chain and carry input of each stage are two inputs of the skip logic. Whether the carry will be propagate or not depends on the select signal, select signal is product of the propagation signal of that stage.

The carry skip adder may be designed using fixed state size (FSS) and variable state size (VSS) structures. Variable state size structure will give the highest speed [7], [10]. By the state size we means number of full adders in CLA block, i.e. state size is the same as the CLA block size.

III. PROPOSED STRUCTURE

Based on the structure that is proposed in [11] the total delay of the CSKA is reduced by minimizing the delay of the Skip logic block. The skip logic delay is significantly reduced by using the AOI/OAI logic in place of the multiplexer circuit.To eliminate the need of an inverter and delay produced by it we use both AOI and OAI architecture as the skip logic. By using the static gates to form the skip logic we are also reducing the area required and power consumed. Because multiplexer based skip logic will acquire the area equal to 12 transistors while an AOI/OAI structure will need the area of only six transistors. The structure is designed using the Conventional carry skip adder and concatenation & incrementation schemes; hence, we will denote it as CI_CSKA.

Hybrid CI_CSKA using CLA Block:

Another way to reduce the delay of the CSKA is to use the CI_CSKA structure with the replacement of RCA blocks by CLA blocks. CLA block in the first stage will reduce a significant amount of the delay which is there due the ripple carry adder in the [11]. If the first stage size is small or in other words first block is less than four bit wide in that case it is not necessary to use all large number of gates of the carry lookahead logic block. But if someone is designing an adder for a large number of bits than using the CLA logic with CI_CSKA structure will give very high speed in comparison with the CI_CSKA designed using the RCA logic blocks.

In the figure 2, it is shown that the carry input of each CLA block, except from the first block carry input which is C_i, is zero. This will result in the concatenation of CLA blocks. Since each CLA block do not need to wait for the carry

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from previous stage, all CLA blocks work simultaneously. Due to this parallel processing during the computation of the summation for first block and C_1, other blocks results in the $C_j$and intermediate signals [i. e., $\{Z_{K_j+M_j}, \ldots, Z_{K_j+2}, Z_{K_j+1}\}$ for$K_j = r_j$-11 Mr (j = 2, . . . , Q)]. The incrementation block uses these intermediate signals produced by CLA blocks and output signal from previous Skip logic stage to calculate the final sum output of the stage. The final carry is also calculated from skip logic instead of calculating it from incrementation block, to save the time.

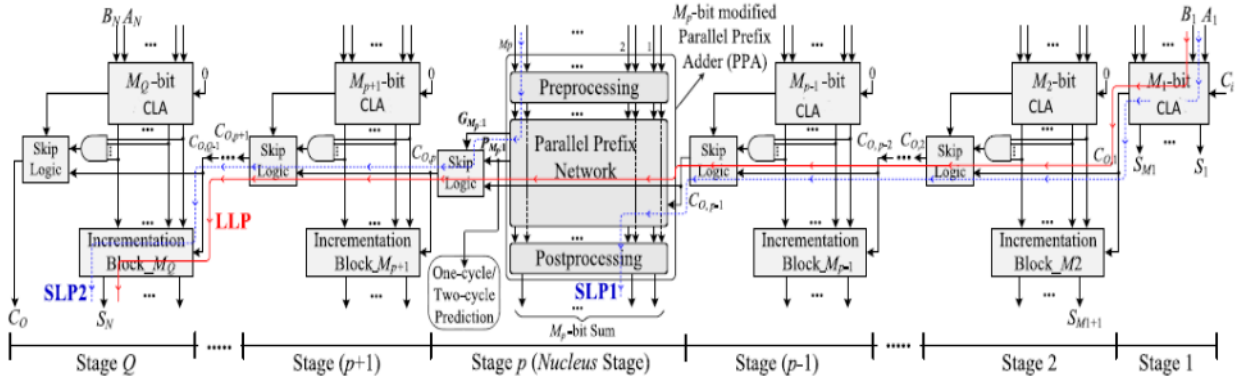

Fig.2. Proposed Hybrid CI_CSKA Structure

To further increase the speed of CLA based CI_CSKA a hybrid structure can be used. By the term hybrid, we mean that the structure will have both CLA blocks and a parallel prefix network in the middle stage. Parallel prefix network is used to reduce the computation time. Since the Kogge Stone parallel prefix network gives best compromise between the speed and area requirement.

The Parallel prefix network that we have used is placed in the central stage of adder. Kogge Stone adder is the fastest parallel prefix adder structure but it cost more when it comes to area occupied by PPA. Delay produced by the Kogge Stone PPA network can be as-

$$T = log_2 K$$

Here,

K represents the number of bits

IV. SIMULATION RESULTS

The simulationsare done by VIVADO Design Suite 16.2 and the targeted family of FPGA is Artix-7. This work involves the designing of a Hybrid CI_CSKA structureusing severalsmall size CLA blocks along with a PPA block as shown in Fig.2. The proposed energy efficient algorithm is implemented using VHDL language. The structure presented in this paper is compared on the basis of mainly two performance metrics path delay and total on chip power. Results that we have obtained clearly shows that both of the performance metrics i.e. the path delay and total on chip power for the proposed structure arebetterthan the basic carry skip adder, and CI carry skip adder proposed in [11].

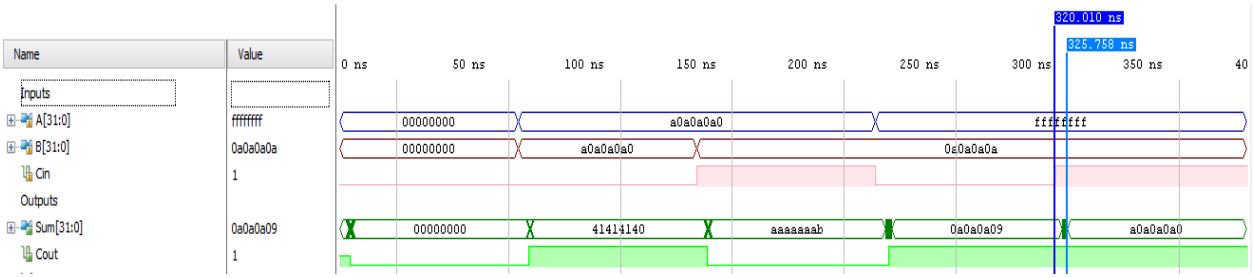

Fig.3. Output waveform of Hybrid CI_CSKA

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The simulation results are shown in Fig.3. Waveforms shown in Fig.3 are simulation result of the synthesized adder structure. The ambiguity present at the starting of the output waveforms are due to the delay produced by the adder. When we are using CLA blocks for addition the delay that is present is mainly because of the routing used for each gate.

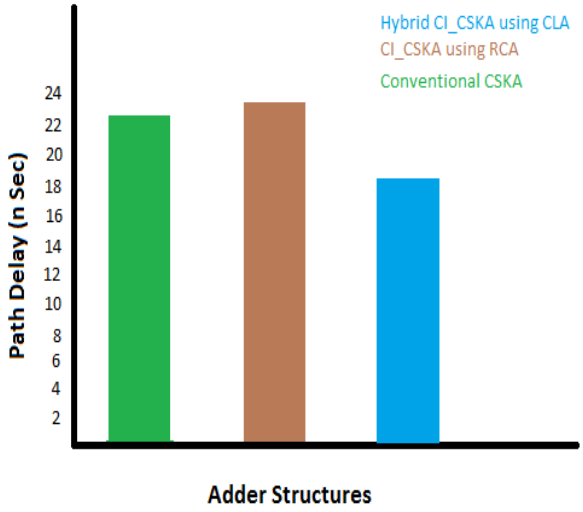

Fig.4. Path Delay Comparison

Graph in Fig.4 is showing the comparative time delay introduced by each of the structure i. e. Carry Skip Adder, CI_CSKA adder using RCA blocks and Hybrid CI_CSKA using CLA blocks. Comparison of on chip power consumed by each one of these structures is presented in Fig.5.

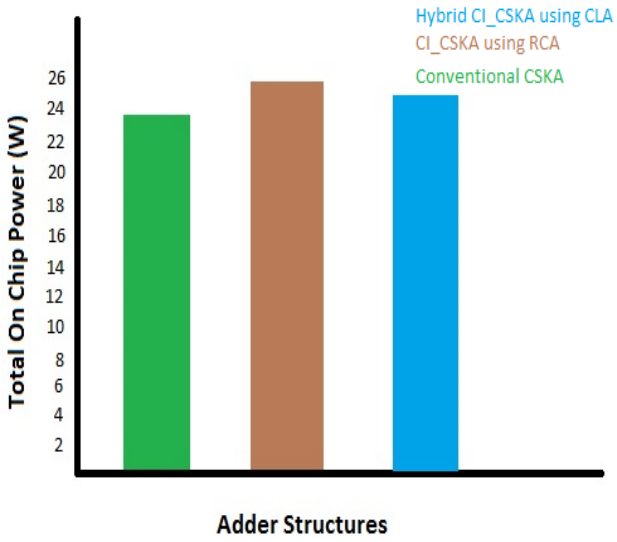

Fig.5. Comparison of On Chip Power dissipation

V. CONCLUSION AND FUTURE WORK

Low power and high speed architecture of Hybrid CI_CSKA is proposed in this paper. The simulation results showed that the proposed architectureis better in terms of speed and power consumption compared to the existing one.

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The proposed structure is an energy efficientstructure for addition using the fixed state size of CLA blocks. Hybrid CI_CSKA has very low delay but because of the CLA blocks it needs extra gates, which will cost us in term of area requirement. With some modifications in design structure area, delay and power can be the metrics that can be used to analyze in future work for the performance analysis of the CI_CSKA.We have done analysis for 32 bit adder. One can increase the number of bit and analyze the performance.

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BIOGRAPHY

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