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Review Paper on Hybrid Square Kogge Stone Adder and Vedic Multiplier Technique

Vivek Gupta, Prof. Vaibhav Jindal

M. Tech. Scholar, Department of Electronics and Communication, SISTech. Gandhinagar, Bhopal, India

Assistant Professor, Department of Electronics and Communication, SISTech. Gandhinagar, Bhopal, India

ABSTRACT: In this Technical era the high speed and low area of VLSI chip are very- very essential factors. Day by day number of transistors and other active and passive elements are growing on VLSI chip. In Integral part of the processor adders play an important role. In this paper we are studied of hybrid kogge-stone adders and Vedic multiplier for binary addition to reduce the size and increase the efficiency or processor's speed.Hybridkogge stone adder and Vedic multiplier provides less components, less path delay and better speed compare to other existing kogge stone adder and other adders. Here we are comparing the kogge stone adders of different-different word size from other adders.

KEYWORDS: KoggeStone Adder, Ripple Carry Adder, Hybrid Kogge Stone Adder

I. INTRODUCTION

The processor's speed mostly depends on adder design techniques. Adder is the device by which two or more than two bit information can be added. For the high speed processing of the data transfer area must be less of the passive and active element. Adder has two outputs specially sum and carry. For making fast adder carry can be reduced and replaced in different ways. The propagation delay or gate delay of a gate is basically the time interval between the application of the input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. Propagation delay should be minimizing as possible as, for high efficient addition. For instance 4 bit addition generally propagation delay is occurred highly.
When we add one high bit to another high bit carry is occurred due to normally addition operation, shown in figure 1. This carry propagates to next bit and now bit addition is performed by 3 bit adder. So carry will propagate to the next bit over and over, this cause propagation delay will be occurred. On the other hand propagation delay can be reduced by the aid of suitable structural designing process. For instance full adder can be designed with one XOR gate, three AND gate and one OR gate. That type of designingwill provide 8.326 ns propagation delay. On the other hand full adder can be design by using two half adder and one OR gate.This type of designing will provide only 8.036 ns propagation delay. Carrypropagation delay can be reduced by using ripple carry adder, fast adder that is also called look a-head carry generator, parallel adder, and specially kogge stone adder.
Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) unit and inner products are some of the frequently used Computation- Intensive Arithmetic Functions currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filter circuits and in microprocessors in its arithmetic and logic unit (ALU). Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.
In this work we have put into effect a high speed Vedic multiplier using barrel shifter. The sutra was implemented by modified design of "Nikhilam Sutra" due to its feature of reducing the number of partial products. The barrel shifter is used at different levels of designs to reduce the delay when compared to conventional multipliers. The hardware implementation of Vedic multiplier is using barrel shifter contributes to adequate improvement of the speed.
In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is great importance in DSP as well as in general processor. In past multiplication was implemented with a sequence of addition, subtraction and shift operations. There have been many

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algorithms proposals to perform the multiplication, and each offering different advantages and having in terms of speed, circuit complexity, area and power consumption.
The multiplier is a fairly large block of a computing system. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time multiplier is not only a high delay block but also a major source of power dissipation. That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

II. RIPPLE CARRY ADDER

Ripple carry is a combinational circuit for adding more than two bit information. It is also called parallel adder. Ripple carry adder can be designed by using full adder in cascading form. Carry output of first full adder is connected with input of the next full adder, so carry is rippled from one adder to another adder. That is by it is called ripple carry adder.

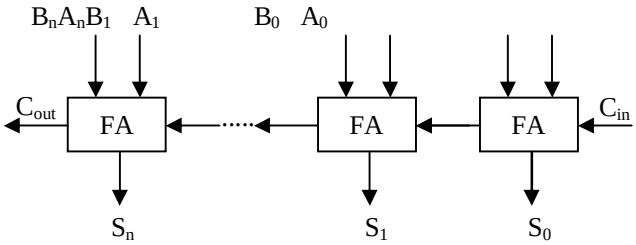

Figure 2:N-bit Ripple Carry Adder

$$S_0 = A_0 \oplus B_0 \oplus C_{in} \quad (1)$$

$$C_0 = (A_0 * B_0) + (B_0 * C_{in}) + (C_{in} * A_0) \quad (2)$$

$$S_1 = A_1 \oplus B_1 \oplus C_0 \quad (3)$$

$$C_1 = (A_1 * B_1) + (B_1 * C_0) + (C_0 * A_1) \quad (4)$$

$$S_2 = A_2 \oplus B_2 \oplus C_1 \quad (5)$$

$$C_2 = (A_2 * B_2) + (B_2 * C_1) + (C_1 * A_2) \quad (6)$$

$$S_n = A_n \oplus B_n \oplus C_{n-1} \quad (7)$$

$$C_n = (A_n * B_n) + (B_n * C_{n-1}) + (C_{n-1} * A_n) \quad (8)$$

III. KOGGE STONE ADDER

Kogge Stone Adder was proposed by Peter M. Kogge and Harold S. Stone. Kogge Stone Adder is an advanced technology of Look a- head Carry Adder. That is also called parallel prefix adder. It has more area than to Brent Kung Adder but less Fan-out. This adder provides the carry signal $O(\log n)$ time and become fastest adder for industrial level.

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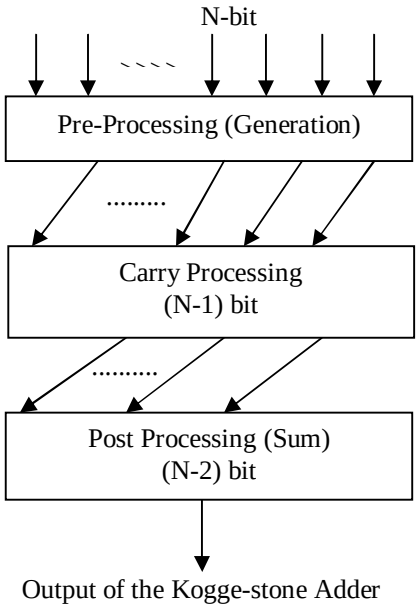

Figure 3: Block Diagram of Kogge-stone Adder

First block of KSA (Kogge Stone Adder) is Pre- Processing that will generate and propagate the carry. Processing of carry will be done over the carry processing area and all the carry signal go through the post processing block. In the pre preprocessing stage we find the, generate and propagate signals from each inputs. Propagating and generating equation can be shown in equation 9&10.

$$P_n = A_n \oplus B_n \quad (9)$$

$$G_n = A_n * B_n \quad (10)$$

Carry processing stage provides the carries corresponding to each bit. Execution of these bit operation is carried out from parallel. After finding the carries in parallel they are segmented in to smaller pieces. Carry equations can be shown in equations 11&12.

$$CP_{n-1} = P_{n-1} * P_n \quad (11)$$

$$CG_{n-1} = (P_n * G_{n-1}) + G_n \quad (12)$$

Below diagram is a functional diagram of kogge stone adder for 4 bit addition. Here elliptically symbol defined as a carry processing stage. The output of the preprocessing stage is fed to next carry stage and post processing as well.

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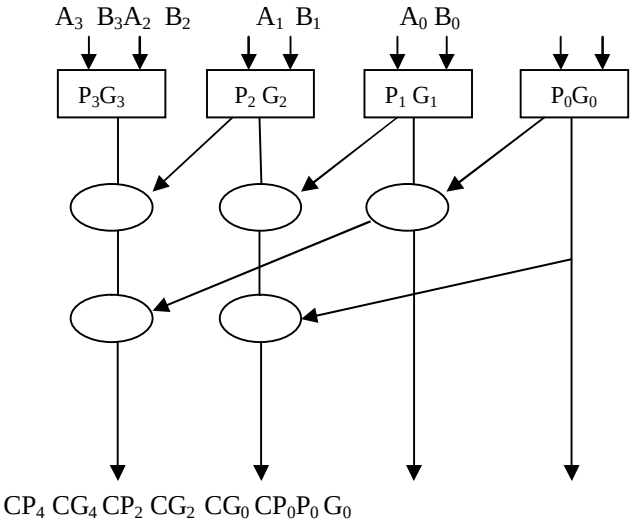

Figure 4: Function Diagram of 4-bit Kogge-stone Adder

IV. HYBRID KOGGE STONE ADDER

The complete functioning of KSA can be easily comprehended by analyzing it in terms of three distinct parts:

(a) Preprocessing: - This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

$$P_i = A_i \; xor \; B_i \qquad (13)$$

$$G_i = A_i \; and \; B_i \qquad (14)$$

(b) Carry look ahead network: - This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit.

$$C_i = G_i \; or \; (P_i \; and \; C_{i-1}) \qquad (15)$$

(c) Post processing: - This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

$$S_i = P_i \; xor \; C_{i-1} \qquad (16)$$

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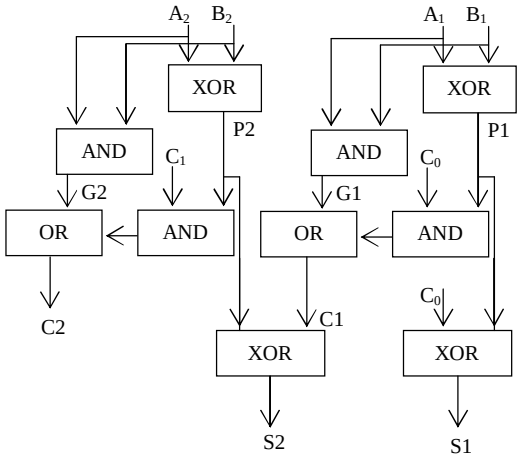

Figure 5: 2-bit Hybrid Square Kogge Stone Adder

V. VEDIC MULTIPLIER

As specified prior, Vedic Mathematics can be isolated into 16 unique sutras to perform scientific counts. Among these the UrdhwaTiryakbhyam Sutra is one of themost exceedingly favored calculations for performing increase. The calculation is sufficiently able to beemployed for the duplication of whole numbers and also binarynumbers. The expression "UrdhwaTiryakbhyam" started from 2Sanskrit words Urdhwa and Tiryakbhyam which mean"vertically" and "transversely" respectively.It depends on a novel idea through which the era of every single fractional item should be possible with the simultaneous expansion of these halfway items. The calculation can be summed up for n x n bit number. Since the incomplete items and their totals are figured in parallel, the multiplier is free of the clock recurrence of the processor. In this way the multiplier will require the same measure of time to figure the item and henceforth is free of the clock recurrence.

The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient.

To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (14×12).

Example- 14×12

- The right hand most digit of the multiplicand, the first number (14) i.e., 4 is multiplied by the right hand most digit of the multiplier, the second number (12) i.e., 2. The product 4 X 2 = 8 forms the right hand most part of the answer.

```
  1   4
    1   2
  -------
      8
```

- Now, diagonally multiply the first digit of the multiplicand (14) i.e., 4 and second digit of the multiplier (12)i.e., 1 (answer 4 X 1=4); then multiply the second digit of the multiplicand i.e., 1 and first digit of the multiplier i.e., 2 (answer 1 X 2 = 2); add these two i.e.,4 + 2 = 6. It gives the next, i.e., second digit of the answer. Hence second digit of the answer is 6.

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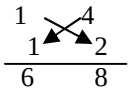
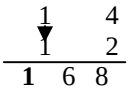


- Now, multiply the second digit of the multiplicand i.e., 1 and second digit of the multiplier i.e., 1 vertically, i.e., 1 X 1 = 1. It gives the left hand most part of the answer. Thus the answer is 16 8.



- Thus the ans

The multiplication of two numbers is done by using UrdhwaTriyakbhyam. Here first the least significant bits of the two digits are multiplied. Then the intermediate digits are cross multi-plied and added together. After this the most significant digits are multiplied.

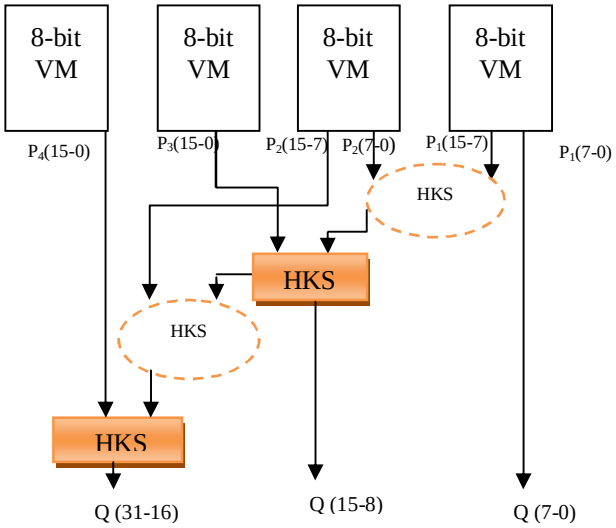


Figure 6: Proposed 16×16 Vedic Multiplier

For the 16X16 bit multiplication small block of 2X2 or 4X4 or 8X8 multiplier were used in parallel to make the process easy and efficient.

In our proposed method the high speed carry select adder is replaced by the carry select adder along with Common Boolean logic which claims to provide a better speed and less propagation delay. Here we have used four multiplier of 8 bit to perform 16 bit multiplication. The method used is the addition of all partial product formed by the cross multiplication of one bit with another. The LSB bits of first multiplier P_1 (7-0) gives the LSB bits Q (7-0) of the final output. Another bits of first multiplier P_1 (15-8) are added in series with LSB 8 bits of second multiplier to form the 16 bits, which in turn get added with 16 bits of third multiplier by using HKS Adder. The LSB bits of the output of HKS adder forms the Q (15-8) bits of the final output. The remaining 8 bit P_2(15-8) is then added with the left 8 bits of HKS output to from 16 bits, which is then added with 16 bits of the fourth multiplier by using HKS adder. The output from HKS adder forms the Q (31-16) bits. This is how the 32bit output is achieved in the less possible time.

V. CONCLUSION

Eventually, all the digital processors are dependent on the adder structure and its properties, so here i am studied a modified and high speed adder that is hybrid KS adder which has less propagation delay. With the help of this adder we can design a fast multiplier which is main component for any processor.

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REFRENCES

[1] G. Challa Ram and D Sudha Rani, "Area Efficient Modified Vedic Multiplier", International Conference on Circuit, Power and Computing Technologies (ICCPCT), 2016.

[2] S. P. Pohokar, R. S. Sisal, K. M. Gaikwad, M. M. Patil and RushikeshBorse, "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics", International Conference on Industrial Instrumentation and Control (ICIC) College of Engineering Pune, India, PP. No. 01-06, 2015.

[3] Gokhale and P. D. Bahirgonde, "Design of Vedic Multiplier using Area-Efficient Carry Select Adder", 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2015), Kochi, pp. 10-13, August 2015, India.

[4] G. Gokhale and Mr. S. R. Gokhale, "Design of Area and Delay Efficient Vedic Multiplier Using Carry Select Adder", 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2015), Kochi, pp. 10-13, August 2015, India.

[5] S. S. Kerur, Prakash Narchi, Jayashree C N, Harish M Kittur and Girish V A, "Implementation of Vedic multiplier for Digital Signal Processing", International Conference on VLSI, Communication & Instrumentation (ICVCI), pp. 01-06, 2011.

[6] HimanshuThapaliyal and M.B Srinivas, "VLSI Implementation of RSA Encryption System Using Ancient Indian Vedic Mathematics", Center for VLSI and Embedded System Technologies, International Institute of Information Technology Hyderabad, pp. 01-05, 2010 India.

[7] SumitVaidya and DepakDandekar. "Delay-power performance comparison of multipliers in VLSI circuit design", International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, pp. 21-28, July 2010.

[8] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global Journal of Engineering Education, Vol.8, No.2, pp. 204-207, Australia 2009.

[9] Shuli Gao, Dhamin Al-Khalili and NoureddineChabini, "Implementation of Large Size Multipliers Using Ternary Adders and Higher Order Compressors", International Conference on Microelectronics 978-1-4244-5816-5/09/$26.00, 2009 IEEE.

[10] S. Bouguezel, M. O. Ahmad, and M. N. S. Swamy, "New parametric discrete Fourier and Hartley transforms, and algorithms for fast computation," IEEE Transaction Circuits System I, Regular Papers, Vol. 58, No. 3, pp. 562– 575, March 2011.

[11] J. S. Wu, H. Z. Shu, L. Senhadji, and L. M. Luo, "Radix 3 × 3 algorithm for the 2-D discrete Hartley transform," IEEE Transaction Circuits System II, Exp. Briefs, Vol. 55, No. 6, pp. 566–570, June 2008.

[12] S. Bouguezel, M. O. Ahmad, and M. N. S. Swamy, "A split vector-radix algorithm for the 3-D discrete Hartley transform," IEEE Transaction Circuits System I, Regular Papers, Vol. 53, No. 9, pp. 1966–1976, Sep. 2006.

[13] D. F. Chiper, "Radix-2 fast algorithm for computing discrete Hartley transform of type III," IEEE Transaction Circuits System II, Exp. Briefs, Vol. 59, No. 5, pp. 297–301, May 2012.

[14] H. Z. Shu, J. S. Wu, C. F. Yang, and L. Senhadji, "Fast radix-3 algorithm for the generalized discrete Hartley transform of type II," IEEE Signal Processing Letter, Vol. 19, No. 6, pp. 348–351, June 2012.

[15] H. V. Sorensen, D. L. Jones, C. S. Burrus, and M. T. Heideman, "On computing the discrete Hartley transform," IEEE Transaction Accusation, Speech, Signal Processing, Vol.33, No. 5, pp. 1231–1238, October 1985.