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Design and Analysis of Multiple-Input OTA Circuit for VLSI Implementation of Neural Networks

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ABSTRACT: An Operational Transconductance Amplifier (OTA) is suitable for the VLSI implementations of artificial neural networks. This paper is mainly concentrating on design of MIOTA circuit modelling for one neuron. Keeping this as a main aspect, Op-amp specifications are taken into account, i.e., Gain, phase margin, slew rate, power dissipation and others. This work presents a design and implementation of MIOTA circuit. It generates an output voltage which is sigmoidal like function of the linear sum of a number of weighted inputs.Weight of each input controlled by the bias voltage. Simulation process is carried out by using an EDA tool cadence virtuoso with 90nm technology.

KEYWORDS: Op-amp,Cadence 90nm technology, Gain.

I. INTRODUCTION

TheOperational Transconductance Amplifier (OTA) is still a fundamental building block in modern microelectronics. In order to achieve high performance ,OTAs with high DC gain, GBW and large output swing is required.The challenge faced in CMOS technology is mainly about scaling these devices to decrease their size and power consumption. However increase in the gain improves the performance and keeps up the stability of device.

Recently there has been an increase in interest in artificial neural networks for use in artificial intelligence applications. This will especially useful in the pattern recognition or optimization with many simultaneous constraints.

Theself-programming properties of these networks allow them to learn from exampledatasetseven in the presence of noisy and conflicting dataandtheirmassive parallelism gives them a degree of faulttolerance [1].

Work in this area is still developing much is still unknown about how biological networks work. In order to simplify the analyses ,most work uses the simplest possible model of a neuron. Many different models with varying numbers of units, connection patterns and learning rules are still being explored [1] [2]. The output function is mostly a nonlinear monotonic increasing function ,typically a sigmoid.

Working models of artificial neural networks have been demonstrated through ,so far, they have been limited in the size[3]-[7]. These circuits are much faster than software simulations running on conventional computers.

The circuit presented in the following paragraphs may be useful for the VLSI implementations of neural networks.It generates an output voltage which is sigmoidal like function of the linear sum of a number of weighted input voltages. The weight of the each input which is controlled by the bias voltage which can be varied dynamically. The inputs have a wide linear range and the number of inputs for each circuit can be large.

II . BASIC CIRCUIT DIAGRAM AND ITS SPECIFICATIONS.

Fig. 1 shows the basic building block which representsone weighted input to the neuron. It sinks an outputcurrentI, which is a linear function of theinput voltage$_{vgs1}$ and has transconductance which is controlledbythebias voltage $_{vb.}$

The transconductance is defined as*dI/dV,* and is the gain of the module.When the outputs ofa number of these blocks are connected to a common node, the currents sum according to Kirchoff's current law and an op-amp can then be used to convert the current to an output voltage which is the weighted sum of the input voltages,

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In Fig. 1, when MOSFET Ml is biased in its active region, $V_{gs1} - V_{T1} > V_{ds1}$, the current I can be writtenas

$$I = \beta[(Vgs-Vt1)- Vds1/2]Vds1 \text{ ---------- (1)}$$

where $\beta=(\mu Cox)W/L$ is determined by the fabrication process and the size of the transistor. V_{t1} is the threshold voltage of M1. When $W2/L_2 >> W1/L_1$ and M2 is biased in its saturation region. Then $V_{ds1}= Vb-VT2.$

If V_b is a constant voltage, and it is assumed that $V_T= V_{T1}=V_{T2}$ then I can be written

$$I = \beta (Vb-VT) [Vi- Vb/2+VT/2] \text{ ----------(2)}$$

Or

$$I = G (Vi- Voffset) \text{ ----------(3)}$$

when M1 biased in its active (ohmic) region, *I* is a linear function of the input voltage Vi= Vgs1 and has a transconductance, *G* controlled by the bias voltage Vb.

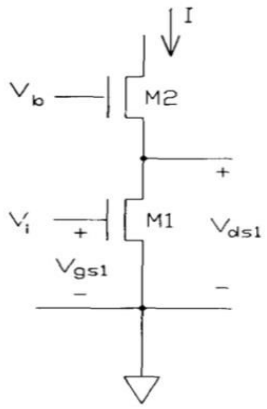

Fig 1. Mosfet structure representing one weighted input

From the Fig 1 shows a graph of the response I versus Vi as a function of $V_b=V_B$ for a test chip which was fabricated in the CMOS process. When $V_{gs1} < V_b$, the response is nonlinear and I approaches 0. The linearity of the response is most strongly dependent on the ratio of the W/L with larger ratios giving a more linear response but generally requiring more circuit area.

These are much larger than the minimum size devices because the original circuit was designed for linearity and frequency response rather than the area efficiency. When the number of these blocks are connected to a common node ,the currents sum according to kirchoffs current law. When these two modules are combined with unity gain current mirror the output current will be

$$Iout = \sum \pm Gi(Vi - Voffset) \text{ ----------(4)}$$

III. DESIGN AND IMPLEMENTATION OF MIOTA CIRCUIT USING TECHNOLOGY.

The circuit of the Fig 2 recognized as a four input OTA.The voltages V_i and V_{bi} has been reffered to a low supply voltage. Typically analog supply voltage of + or – 5V and V_{bi} = - 3.5V.The circuit in fig.2 was originally designed for use in conventional adaptive signal processing applications with special emphasis placed on obtaining a wide linear range and multiple inputs.The transconductance is controlled by the bias voltage in a continuous fashion and is used to tune the circuit .In order to remove the offset voltage which is undesirable in most applications, the groups of modules on either side of the current mirror are made symmetrical in size and bias voltage.

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Certain optimizations of this circuit can be made for use in neural networks. First, the number of inputs can be greatly increased. Second, symmetrical excitory and inhibitory inputs are not required.This will give the circuit an overall offset but typically, one or more inputs would be dedicated to setting the node threshold and these would be adjusted to account for the offset.Finally, since neural networks do not require a very linear response,the relative sizes of the input transistors can be reduced to save circuit area. If the linearity requirement is removed altogether and M1 is operated in the subthreshold region v_b will still control the transconductance and the structure becomes similar to the links used in [4] . This will minimize current consumption but places a restriction on the allowable inputvoltages.The analysis above ignores a number of second order error sources such as device size mismatches and differences in $V_T$due to process variation and sourcesubstrate bias.

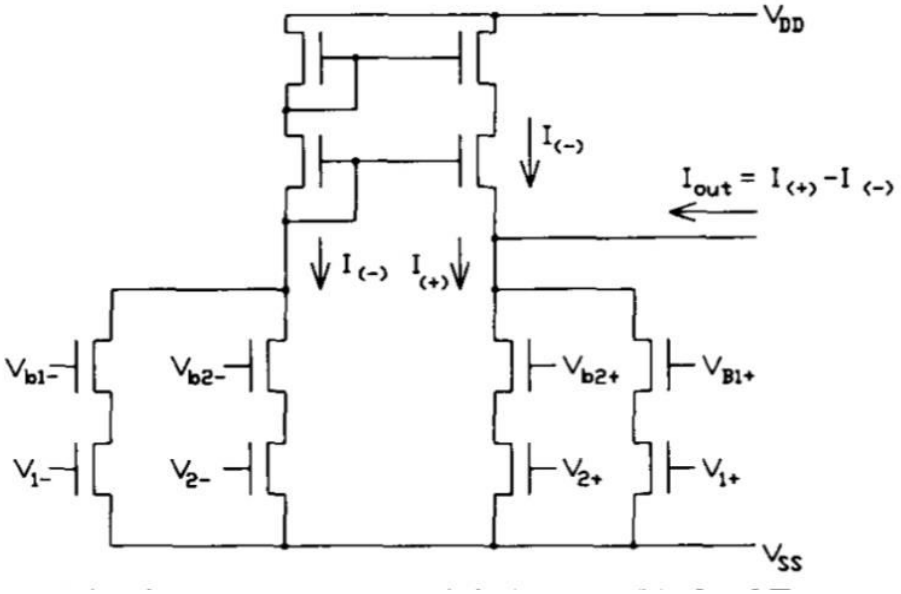

Fig 2 : Four-input multiple-input OTA (MIOTA)

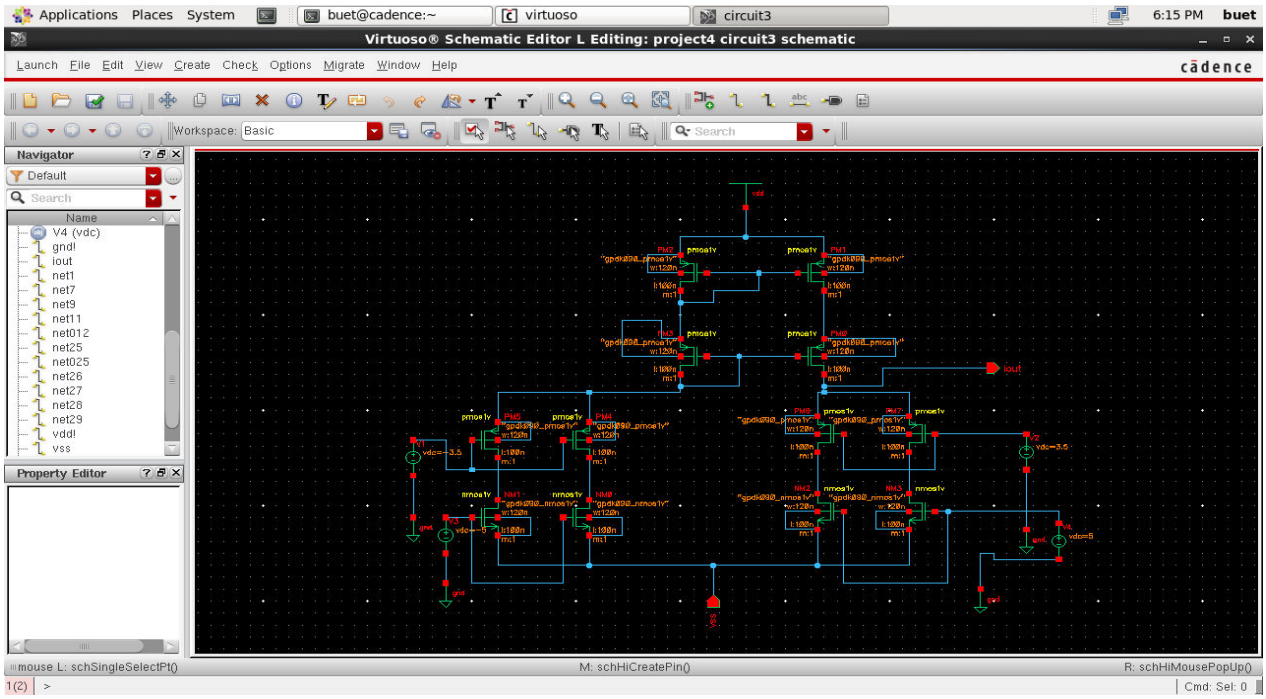

Fig 2. Implementation using 90nm technology.

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IV. CIRCUIT FOR MODELLING ONE NEURON AND ITS IMPLEMENTATION

Fig 3 shows how the circuit can be used to implement an artificial neuron. The operational amplifier and resistor convert the output current to a voltage which, for equally sized devices, is givenby

$$I_{out} = \sum i \pm \beta(V_{bi} - V_T)(V_i - V_{offset}) \quad (5)$$

and

$$V_o = RF(I_{out}) \quad (6)$$

where $F_{(Iout)}$is a nonlinear function describing the saturation behaviour.(6) holds when each input $V_i > V_{bi}$. When$V_i < V_{bi}$, the response becomes nonlinear and dI_x / dV_i, approaches 0.When the magnitude of I_{out}, is greater than some value, the output voltage Vowill saturate atthe supply voltage .These natural limiting effects give the circuit response a sigmoidal shape. ("Sigmoidal" is used here in the sense of any smooth "S" shaped curve; it does not refer to a specificfunction).

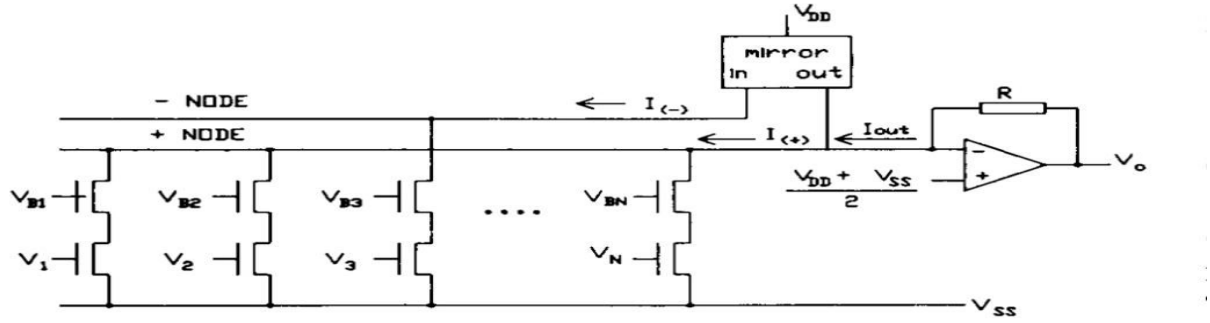
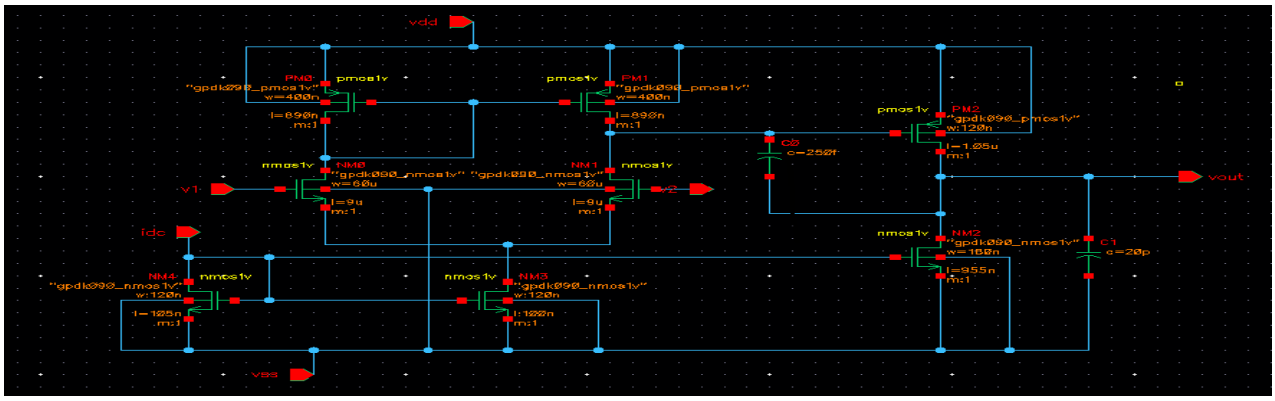


Fig 3. MIOTA circuit modeling one neuron.

This circuit appears to be useful for the VLSI implementations of neural networks because each weighted input or link can be realized with just two MOSFET transistors and all inputs are high impedances which respond to voltages rather than current.The advantage over typical op-amp voltage summing circuits because the weight of each input is continuously controlled by the bias voltage rather than the being determined by a fixed resistor or being switched in discrete steps. The limited input impedance of each resistor in the typical op-amp summing circuit means that a node driving a large number of these inputs would be required to source a relatively large current . Regular arrays of these circuits can be laid out in a crossbar arrangement to create large VLSI networks. The crossbar arrangement is a common one and has been used by Hopfield and Tanka [9] , among others, to connect every input to every summing node.This paper does not address the problem of how the *N X* M bias voltages needed to control the weights of a circuit with *N* inputs M outputs would be generated and stored. One method would be to store the voltage on a capacitor which is periodically refreshed by another system addressing the capacitors in a row/column fashion.



From Fig 3.Op-amp circuit diagram using 90nm technology

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Fig 4. Op-amp circuit output using 90nm technology.

This synaptic circuit might also be used if , as in biological networks, pulses with a firing rate proportional to the signal are used rather than dc voltages. The circuit produces a current proportional to the weighted sum of the input signals which could be integrated on a capacitance.The output pulses could then be generated by a simple op-amp circuit of the type described in [10].

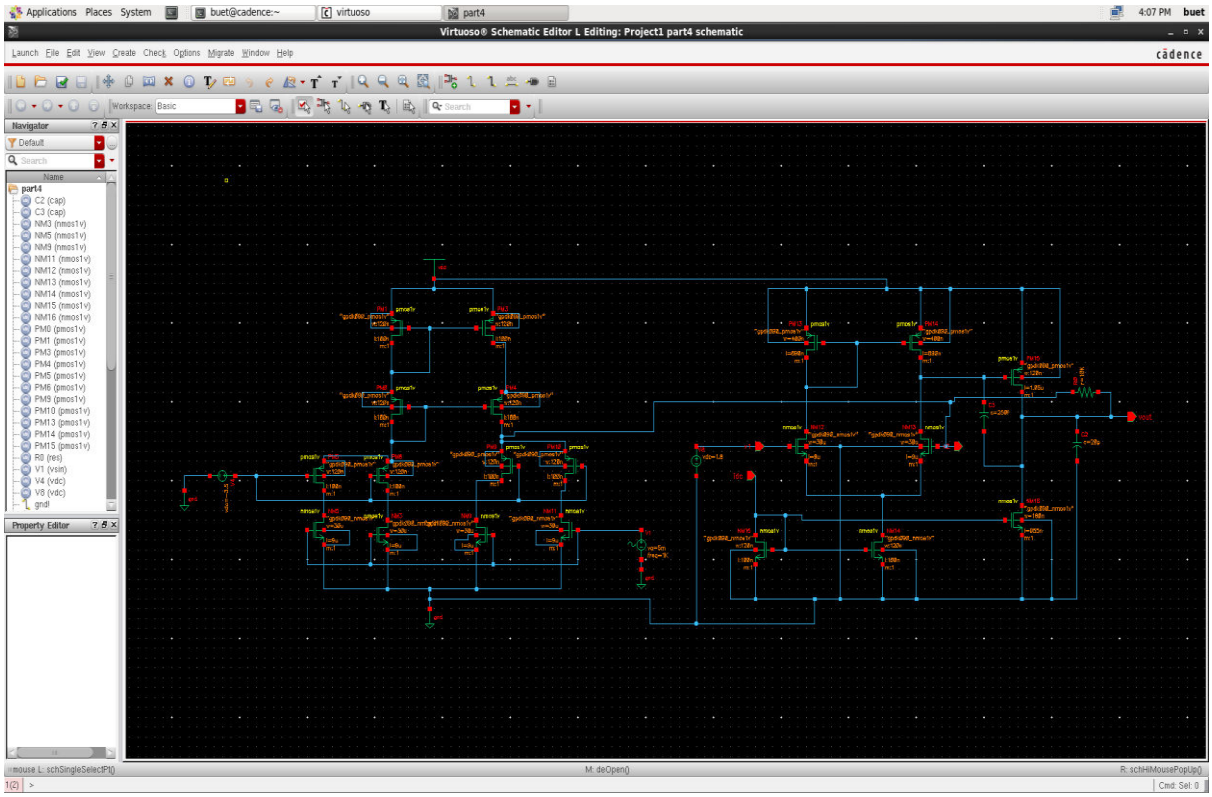

Fig 4 : MIOTA circuit modeling one neuron

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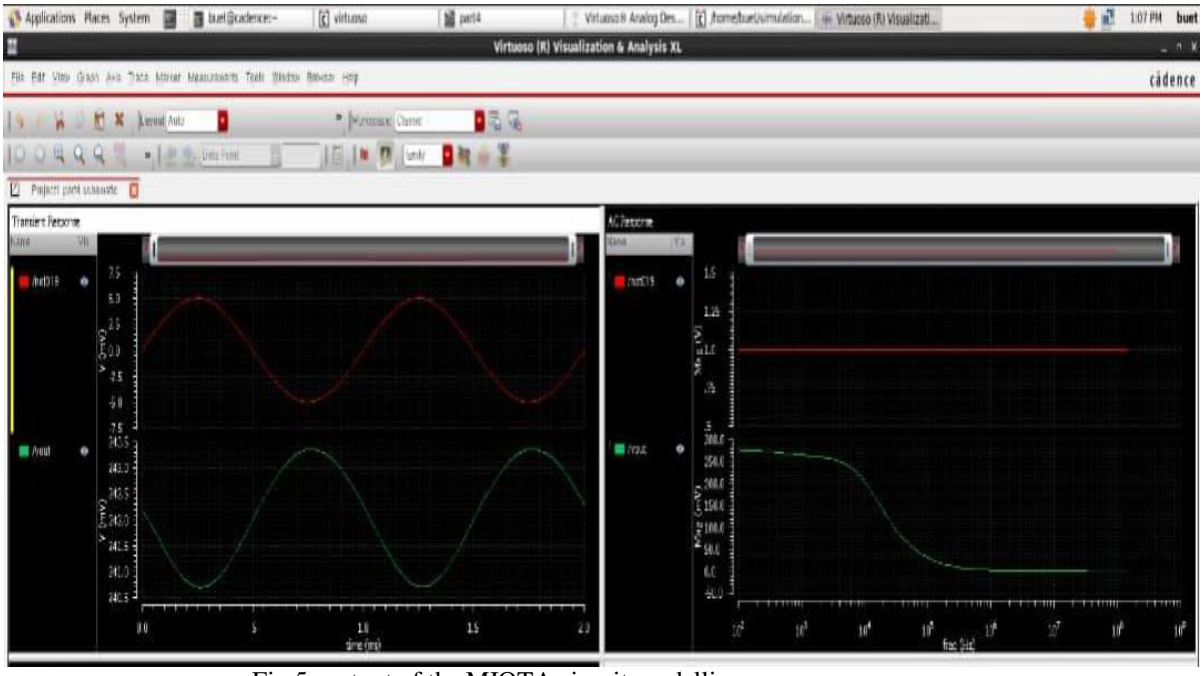

Fig 5: output of the MIOTA circuit modelling one neuron

V. CONCLUSION

A Multiple-Input OTA circuit has been presented which may be useful in VLSI implementations of neural networks. It generates an output voltage which is a sigmoidal function of the linear sum of a large number of input voltages, each input having a weight which is set by an externally controllable bias voltage. Large numbers of these cells can be fashioned in regular arrays.It appears to be efficient because each weighted connection is implemented with only two MOSFETtransistors.

REFERENCES

[1] Parallel Distributed Processing : Explorations in the Microstructures of Cognition . James L. McClelland and David E.Rumelhart , Eds,, Cambridge : MIT Press , 1986.

[2] Proc.IEEE FIRST INT.conf neural networks ,SAN Diego ,ca, June 21-24,1987.

[3] Hans P graf ,Lawrence D.Jackle, and Wayne E Hubbard, "VLSI implementation of a neural network model," Computer ,march 1988,

[4] James Hutchinson,Christof Koch, JinLuo, and carver mead, "Computing motion using analog and binary resistive networks,"computer,mar.1988.

[5] M.A. Sivilotti,m.r.Emerling,and c.A.mead,"VLSI architectures for implementation of neural networks," in proc.Amer.inst.of physics conf .on Neural Networks for computing,pp.408-413,Snowbird,UT,1987.

[6] A moopen,H.langenbacher,A.P. Takoor ,and S.K.Khanna,'Programmable synaptic chip for electronic neural networks,"in proc.Amer.inst.of physics conf .on Neural Information processing systems,pp.564-572,Denver, CO ,1987.

[7] H,P.Graf,L.D.Jackel,R.E.Howard,B.Straughn,J.S.Denker,W,Hubbard,D.M Tennant,and D.Schwartz,"VLSI implementation of a neural networks memory with several hundreds of neutrons,"proc.amer.inst.of physics conf.on neural information processing systems ,pp.182-187,Denver,CO,1987.

[8] Russell D.Reed,"A multiple-input operational transconductance amplifier with a wide linear range."Masters theses,Texas A and M univ,Aug.1986.

[9] David W.Tank and john J.Hopfield ,"Simple 'neural'optimization networks;An A/D converter,signal decision circuit, and a linear programming circuit,"IEEE Trans Circuits Syst., vol.CAS-33,May 1986.

[10] R.W.Nwtworks,"MOS neuristor Lines,'Constructive Approaches to mathematical models. Coffman/Fix, Eds. New York:Academic,pp.87-11,1970.

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