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Design and Implementation of Scalable Micro Programmed Fir Filter Using Wallace Tree and Birecoder

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ABSTRACT: Finite impulse response (FIR) filter is one of the important components in any DSP and communication systems. The output from the DSP processor is depends on the FIR filter, so need an efficient FIR filter design, to achieve an efficient output. Filter architecture contains many components; one of the main components is multiplier. Different types of multipliers are available in the digital circuits, but need an efficient multiplier design to get efficient filters. In the existing Wallace tree multiplier was designed and implemented using verilog HDL. This multiplier needs many gates to implement the design. So it takes more area and delay. To reduce the drawbacks in the existing system, to propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks. Multiplier is design by verilog HDL, after the design Wallace tree multiplier is compared with Birecoder, and analyzes the performance of the multiplier. Implement the design using Modelsim 6.3c and Xilinx ISE. Finally the designed multipliers are applied into the FIR filter, and show the best filte

KEYWORDS: Wallace tree, Birecoder, Modelsim 6.3c, Xilinx ISE, FIR filter.

I. INTRODUCTION

The unstable growth in portable multimedia and mobile computing applications has enlarged the demand for low power digital signal processing (DSP) systems and Wireless Communication. One of the most extensively used functions executed in DSP is Finite Impulse Response (FIR) filtering. In several applications, in order to attain high spectral suppression and noise reduction, FIR filters with moderately huge number of taps are essential. A lot of prior efforts for decreasing power consumption of FIR filter usually focus on the miniaturization of the filter coefficients whereas maintaining a fixed filter order[1& 2] . FIR filter structures are simplified to minimizing the number of additions/subtractions and add & shift operations. Though, one of the problems encountered is that one time the filter architecture is determined, the coefficients cannot be altered consequently, those are not appropriate to FIR filter with programmable coefficients. Fairly accurate signal processing systems are also used for the design of low power digital filters. In FIR filter order vigorously varies along with the stop band energy of the input signal. But the approach affects from slow filter-order adaptation time because of energy calculations in the feedback method [3& 4].

II. DIGITAL FILTERS

A Digital filter is a filter that performs mathematical operations on sampled and discrete time signals to reduce or enhance certain aspect of the signals. It usually consists of an Analog-to-digital converter block to convert the analog form of signal to digital form signal (sampled data or discrete time signal). To perform the numerical operations on the sampled data or discrete time signal, digital signal processors are used. This processor may be a general purpose processor such as PC or a microprocessor or a DSP chip. In some high performance applications, FPGA or ASIC is used instead of general purpose processor or specialized DSP with specific parallel architecture for performing operations such as filtering. It carries the numerical calculations on sampled data. These calculations typically involve multiplying the input values by constants and adding the products together. In addition to, some peripheral components such as memories are used to store the data [5].

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III. EXISTING WALLACE TREE MULTIPLIER

A method for fast multiplication was originally proposed by Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Using this method, a three step process is employed to multiply two integer numbers. The first step is to multiply each bit of one of the arguments, by each bit of the other, yielding *n2* resulst[6]. Based on the position of the multiplied bits, the wires carry different weights. The second step is to reduce the number of partial products to two by layers of full and half adders. The third step is to group the wires in two and then add them using conventional adder . In this paper, two different architectures of Wallace tree multiplier are presented. First one is designed using only half adder and full adder, while the second one uses a more sophisticated carry skip adder (CSA)[7].

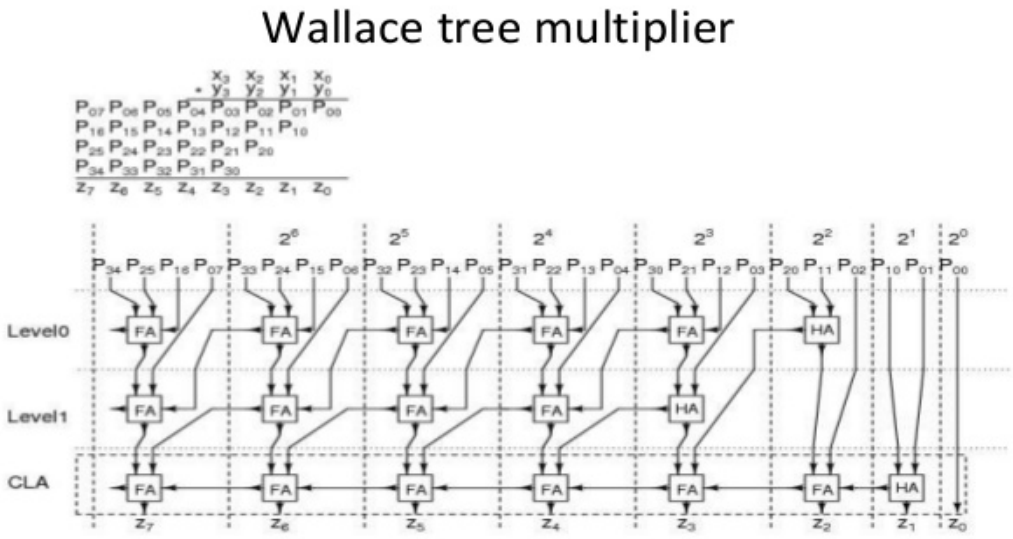

Fig 1. Wallace tree multiplier

A, STRUCTURE OF REDUCED COMPLEXITY WALLACE MULTIPLIER

A Wallace multiplier is a parallel multiplier which performs the array multiplication effectively [7]. Array multiplier has more number of gates to perform multiplication. Hence, it occupies large area for computation. In order to overcome this problem, Wallace multiplier with proposed SQRT CSLA is designed. Fig 3 shows reduced complexity Wallace multiplier structure. The reduced complexity Wallace multiplier consists of reduced number of half adders when compared to the conventional Wallace multiplier [8]. In the modified circuit, N^2 AND gates form the partial products and they are arranged in an inverted triangle order. The matrix is divided into three row groups in the reduced complexity Wallace multiplier.

1) Full adder is used for adding three bits.
2) Single bit and a group of two bits are moved to the next stage directly.

In the final stage of Wallace multiplier, proposed SQRT CSLA is used instead of conventional SQRT CSLA for addition process. It reduces area as well as power.

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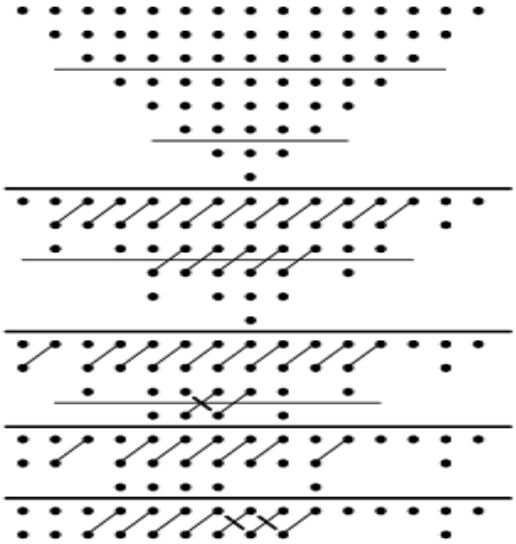

Fig 2 .Structure of reduced complexity Wallace tree multiplier

IV. PROPOSED BI-RECODER MULTIPLIER

Bi-Recoder multiplier, partial products are generated using multiplexer. Multiplexer is used to perform the partial product generation process based on multiplier bit values. In fig the value of a represents multiplicand value and the value of b is multiplier value. For each multiplexer produces 10-bit partial product value. Multiplier bits are divided into four groups and each group is having two bits. So four set of multiplexer is needed to generate the partial products.If value of b is "00" means, it passes simply 0 to the partial product generator else if it is "01" means it simply passes multiplicand value to the partial product generator else if it is "10" means it passes 1 bit left shift of multiplicand value in terms of 10 bits else it is "11" means add the results of multiplicand and 1 bit left shift of multiplicand value

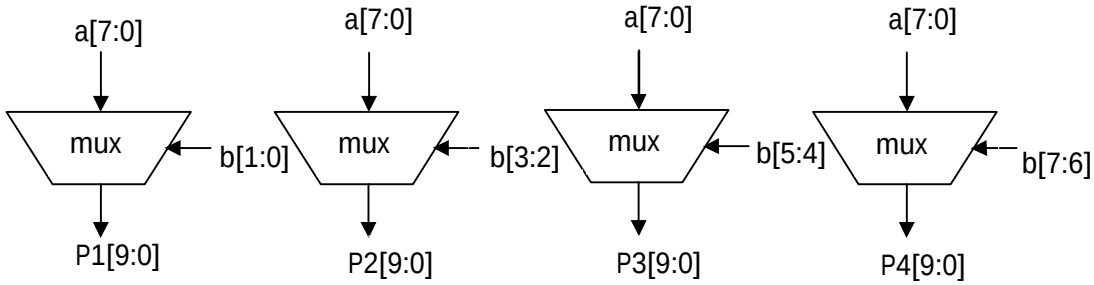

Fig. 3 Partial Product Generation stage of Bi-Recoder multiplier

A. BI-RECODER BASED FIR-FILTER

Digital Signal Processing (DSP) operations are widely used in wireless communication Technologies to control and guide the signal flows. Convolution, Correlation, Frequency Transformation and filtering are the important operations of DSP applications. In this research work, Finite Impulse Response (FIR) filter is considered for improving the performance of digital filtering process in wireless communication technology. Large endeavours have been worked on direct form digital FIR filter to improve the performance in terms of high speed and throughput. The relationship of input- output of Linear Time Invariant (LTI).

System is represented as in equation,

$yout(n) = \sum Coeff\ p\ Xin\ (n - 1)$

Where, xin(n) represents the input samples of FIR filter, yout(n) represents the output samples of FIR filter, N is the order of the filter or length of the filter and Coeffp denotes the coefficient of filters. Impulse response of FIR filter

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must be finite and therefore, filtrations also based on some finite numerical values. Square Root Carry Select Adder (SQRT CSLA) is one of the best VLSI based adders, because it utilizes less hardware complexity and high speed. Area efficient CSLA architecture is developed for binary addition process. The combination of Ripple Carry Adder (RCA) and Binary to Excess1 Conversion (BEC) unit is to reduce the propagation delay of addition process. In SQRT CSLA, N-bit data can be divided into √Ngroups for performing parallel addition process. In this, design of FIR filter is done by using Verilog Hardware Description Language (Verilog HDL). To increase the erformance of digital FIR filter, a novel BiRecoder Multiplier and reduced complexity SQRT CSLA are developed in this research work.

B. PROPOSED SQRT CARRY SELECT ADDER

carry select adder using D-Latch in the place of BEC for the purpose of speed improvement. The conventional SQRT CSLA consists of Ripple carry adder and BEC as shown in Fig.4 whereas RCA or D Latch was used in earlier architectures. The Conventional Group2, Group3 and Group4 structures are shown in Fig.5 which contain full adder, half adder, Binary to Excess1 code Converter and multiplexer units. Conventional SQRT CSLA offers lower delay and high speed than the previous architectures. Fig. 4 shows the block diagram of conventional SQRT CSLA using BEC architecture. First set of RCA is having carry input as '0' and second set is binary to excess-1 converter (BEC). Finally based on carry input, it selects sum output by using multiplexers. This adder is incorporated in the Wallace Multiplier.

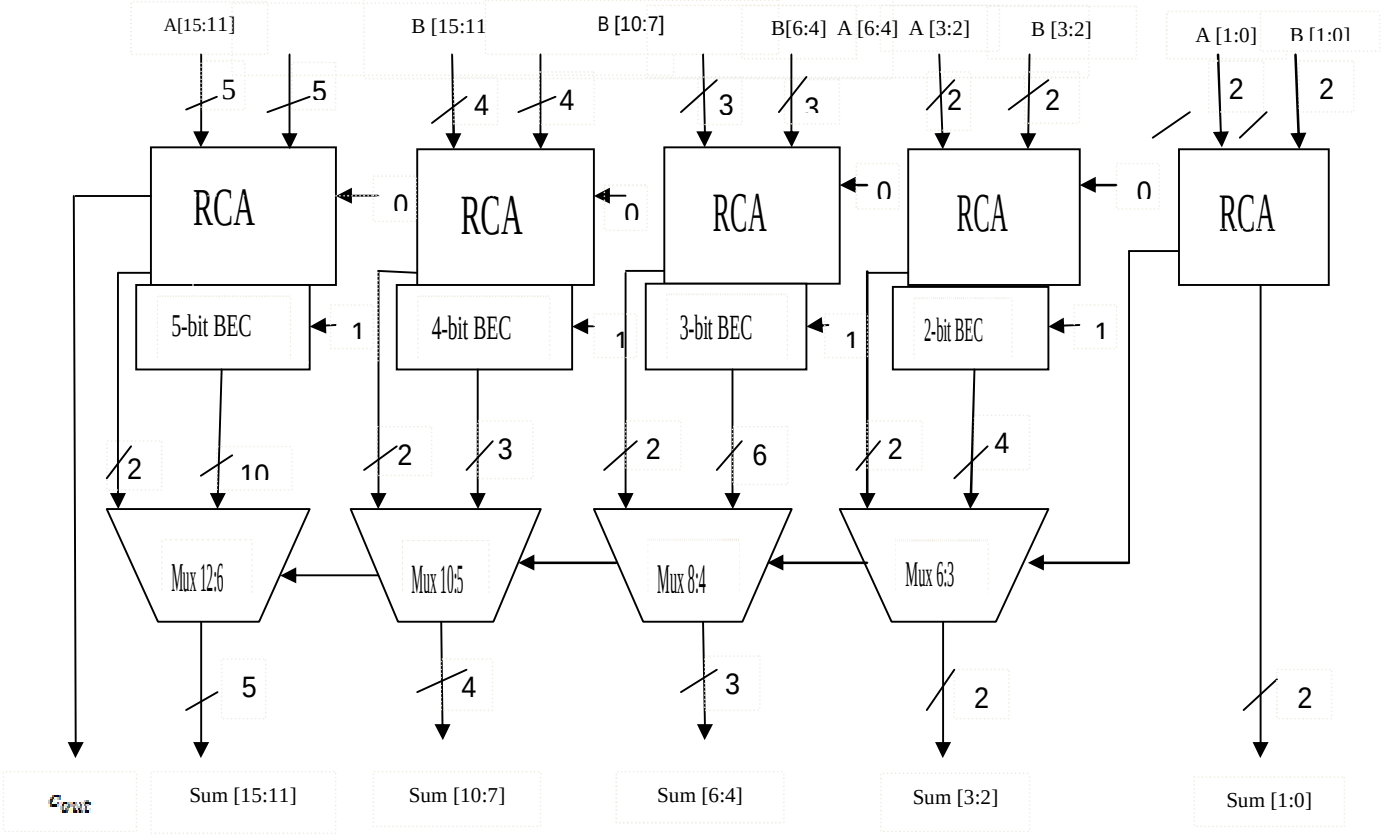

Fig 4, SQRT Carry Select Adder

proposed group-2, group-3, group-4 and group-5 structures. Group structure operation is based on only half adders. Sum output is given to an inverter which is stored in 2:1 multiplexer and sum output is given directly for same 2:1 multiplexer. If carry input is'0', it selects direct sum result or otherwise inverted output as sum. For carry output sum and carry is getting Ex-ored which is given to another 2:1 mux and another input is carry form half adder. If carry input is '0', it selects half adder carry as final carry or otherwise remaining input as final carry. Then Carry output is given to next stage as carry input. The process is continued for group-2, group-3, group-4 and group-5 structures.

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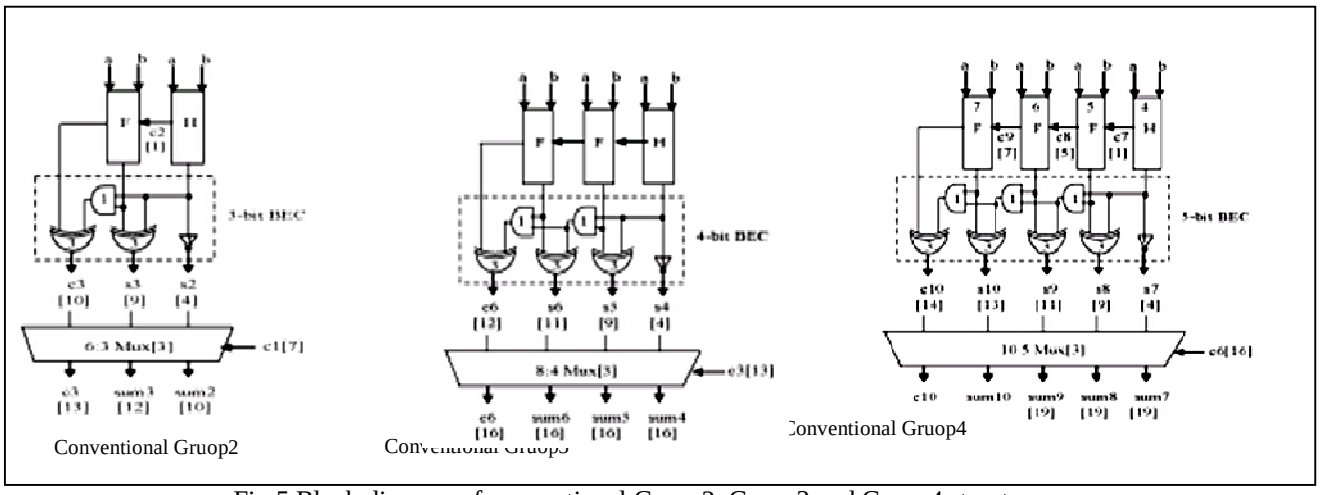

Conventional Gruop2 Conventional Gruop4

Fig 5 Block diagram of conventional Group2, Group3 and Group4 structures

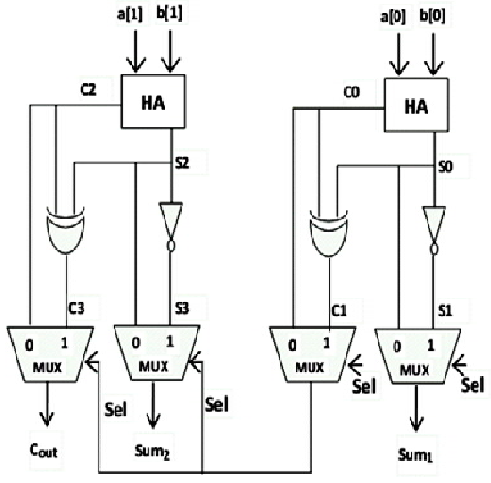

Fig.3 Block diagram of proposed Group2 structure for proposed SQRT CSLA.

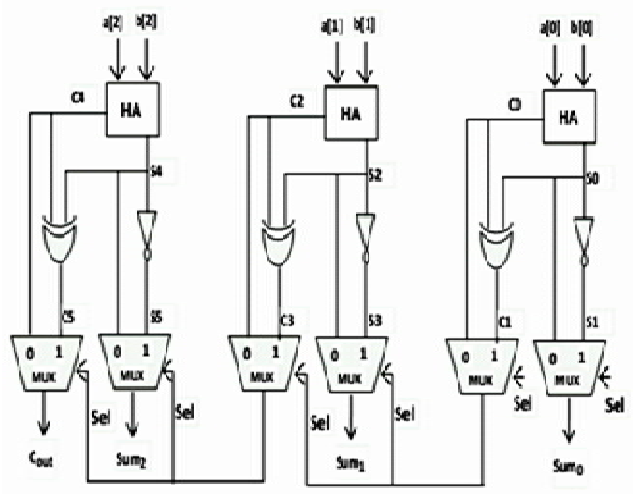

Fig.4 Block diagram of proposed Group3 structure for proposed SQRT CSLA.

Fig 6 Block diagram of proposed Group 2 & 3 structure for proposed SQRT CSLA

The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of compressors adder based Bi-Recoder due to less hardware complexity of reduced complexity SQRT CSLA.Both compressors based digital adder and reduced complexity SQRT CSLA adder is incorporated into the addition part of Bi-Recoder multiplier independently. The performance of reduced complexity SQRT CSLA based Bi-Recoder is better than the performance of compressors adder based Bi-Recoder due to less hardware complexity of reduced complexity SQRT CSLA.

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V. RESULTS AND DISCUSSION

The FIR filter designs are coded in Verilog hardware description language (HDL) and implemented in FPGA using Xilinx Virtex-5 (xc5vlx50t-1ff1136) as the target device. The Wallace tree and Bi-recoder multipliers are used in sequential and parallel architecture of microprogrammed FIR filters. Simplify pro tool is used for the synthesis, translation, mapping and place-and-route process. Different reports are generated by the CAD tools which are summarized in the tables below. The iteration of synthesis has The FPGA resource utilization table includes Virtex-5 slice look-up tables (LUTs), minimum period and maximum clock frequency. Table I and table I summarizes the implementation results of the sequential FIR filter using Wallace tree and Bi-recoder multipliers respectively.

A. COMPARSION OF WALLACE TREE MULTIPLIER AND BIRECODER MULTIPLIER

The comparsion of Wallace tree multiplier and Birecoder multiplier of power, delay, area. The power is denoted by (mw) its represented in the form of tabular column and its represented by using chart.

Parameters	Existing Wallace Tree Multiplier	Proposed Bi-recoder Multiplier
LUTs	144	130
Slices	94	72
Delay	21.440ns	20.165ns
Power(mW)	894mW	746mW

Tab 1- Comparsion of Wallace tree and Bi-recoder Multiplier

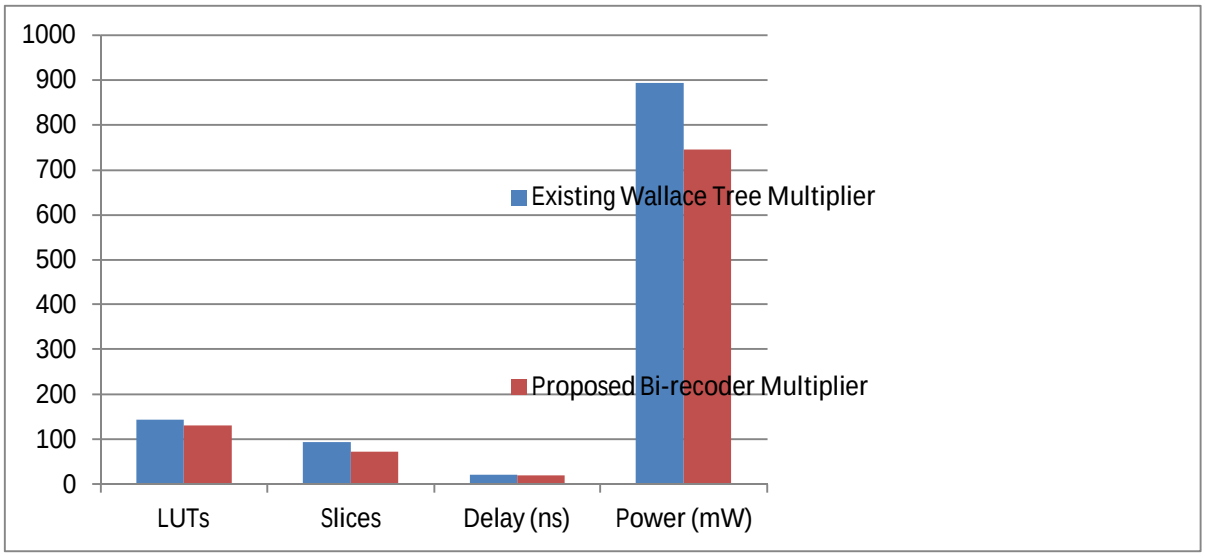

Chart - Comparison of Wallace tree and Bi-recoder Multiplier

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VI. CONCULSION

Digital filters are one of the main elements of DSP. FIR filter which mainly comprises of multiply-accumulate structure is the most commonly used digital filter. Since the performance of FIR Filter mostly depends on the multiplier used, an enhanced and improved multiplier will ameliorate the overall system performance. Wallace tree multiplier was designed and implemented using verilog HDL. This multiplier needs many gates to implement the design. So it takes more area and delay. To propose a new efficient multiplier named as Birecoder multiplier. It is one of the best multiplier in the digital circuit design. This multiplier overcomes the existing multiplier drawbacks.

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BIOGRAPHY

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