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Carbon Nano Tubes in Field Effect of Transistor

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ABSTRACT: Carbon Nanotube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance very dense and low power circuits. A Carbon Nanotube Field Effect Transistor refers to a FET that utilizes a single CNT or an array of CNT's as the channel material instead of bulk silicon in the traditional MOSFET structure. The core of a CNTFET is a carbon nanotube. The structure, operation and the characteristics of different types of CNTFET's have been discussed. The operation, *dc* characteristics of CNTFETs and analysis of the performance of various characteristics have been presented.

KEYWORDS: CNTFET, Carbon nanotubes, Field effect transistors, Nanoelectronics, characteristics

I. INTRODUCTION

The first carbon nanotube field-effect transistors were reported in 1998 These were simple devices fabricated by depositing single-wall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been prepattemed with gold or platinum electrodes. The electrodes served as source and drain, connected via the nanotube channel, and the doped Si substrate served as the gate. A schematic of such a device is shown in Fig.1. Clear p-type transistor action was observed, with gate voltage modulation of the drain current over several orders of magnitude. The devices displayed high on-state resistance of several MQ, low transconductance (-Ins) and no current saturation, and they required high gate voltages (several volts) to turn them on.

Following these initial CNTFET results advances in CNTFET device structures and processing yielded improvements in their electrical characteristics. Rather than laying the nanotube down upon the source and drain electrodes, relying on weak vander walls forces for contact, the electrodes were patterned on top of previously laid down CNs. In addition to Au, Ti and CO were used, with a thermal annealing step to improve the metal/nanotube contact. In the case of Ti, the thermal processing leads to the formation of TiC at the metal/nanotube interface, resulting in a significant reduction in the contact resistance from several MΩ to 30 kΩ. On state currents ~1μA were measured, with transconductance - 0.3 μS[1].

All early CNTFET were p-type, i.e., hole conductors. Whether this was due to contact doping or doping by the adsorption of oxygen from the atmosphere was initially unclear. N-type conduction was achieved by doping from an alkali (electron donor) gas and by thermal annealing in vacuum. Doping by exposure to an alkali gas involves charge transfer within the bulk of the nanotube, analogous to doping in conventional semiconductor materials. On the other hand, annealing a CNTFET in vacuum promotes electron conduction via a completely different mechanism: the presence of atmospheric oxygen near the metal/nanotube contacts affects the local bending of the conduction and valence bands in the nanotube by way of charge transfer, and the Fermi level is pinned close to the valence band, making it easier for injection of holes. When the oxygen is desorbed at high temperatures, the Fermi level may line up closer to the conduction band, allowing injection of electrons. Contrary to the case of bulk doping, there is no threshold voltage shift when going from p-type to n-type by thermal annealing. In addition, it is possible to achieve an intermediate state, in which both electron and hole injection are allowed, resulting in ambipolar conduction[2].

Carbon nanotube field effect transistor (CNTFETs) uses semi conducting carbon nanotube as the channel. Both p-channel and n-channel devices can be made from nanotubes. The physical structure of CNTFETs is very similar to that of

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MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics. Of course, there are some distinct properties of CNTFETs, such as:

▪ The carbon nanotube is one-dimensional, which greatly reduces the scattering probability. As a result the device may operate in ballistic regime.

▪ The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. In other words,there are no dangling bonds which form interface states. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface.

The Schottkey barrier at the metal-nanotube contact is the active switching element in an intrinsic nanotube device[3]. With these unique features CNTFET becomes a device of special interest.

II. TYPES OF CNTFET

The field effect transistors made of carbon nanotubes so far can be classified into:

a) Back gate CNTFET
b) Top gate CNTFET
c) Wrap-around gate CNTFETs
d) Suspended CNTFETs

These are explained below:

a) *Back-gated CNTFET's*

The earliest techniques for fabricating carbon nanotube (CNT) field-effect transistors involved pre-patterning parallel strips of metal across a silicon dioxide substrate, and then depositing the CNTs on top in a random pattern [1]. The semiconducting CNTs that happened to fall across two metal strips meet all the requirements necessary for a rudimentary field-effect transistor. One metal strip is the "source" contact while the other is the "drain" contact. The silicon oxide substrate can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gateable.

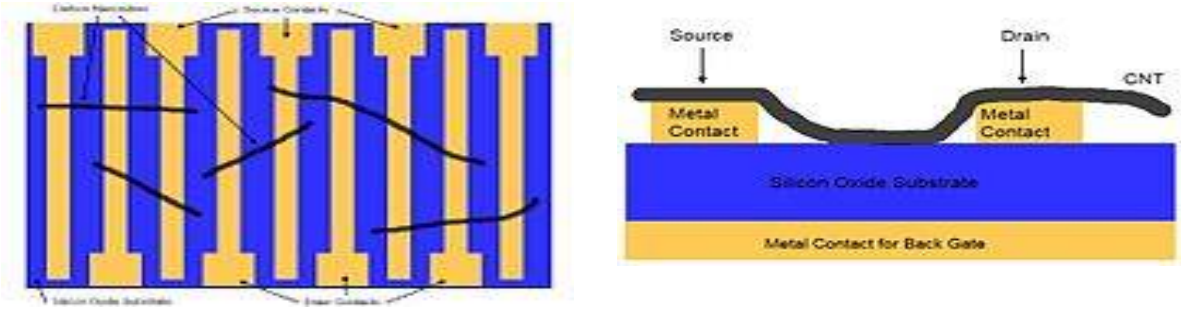

Fig 2: Top and side view of carbon nanotubes deposited on a silicon oxide substrate pre-patterned with source and drain contacts.

The types of back gate CNTFETs discussed so far have high contact resistances (≥1 MΩ), which led to a low transconductance gm (=dI/dVG) of about 10 -9A/V. This large contact resistance results from the weak van der Waals coupling of the devices to the noble metal electrodes in the 'side-bonding' configuration used. Here the SWNT is dispersed on top of the SiO2 film, and then source and drain electrodes made of transition metals compatible with silicon technology, such as Ti or Co, are fabricated on SWNT. Subsequent anneals at 400º C (Co) and, or at 820º C (Ti) in an inert ambient, form low resistance Co contacts or TiC contacts at the source and drain electrodes. Fig.1 shows I-V characteristics of p-type CNTFET employing metallic Co or TiC contacts[4].

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b) *Top-gated CNTFET's*

Eventually, researchers migrated from the back-gate approach to a more advanced top-gate fabrication process [2]. In the first step, single-walled carbon nanotubes are solution deposited onto a silicon oxide substrate. Individual nanotubes are then located via atomic force microscope or scanning electron microscope. After an individual tube is isolated, source and drain contacts are defined and patterned using high resolution electron beam lithography. A high temperature anneal step reduces the contact resistance by improving adhesion between the contacts and CNT. A thin top-gate dielectric is then deposited on top of the nanotube, either via evaporation or atomic layer deposition. Finally, the top gate contact is deposited on the gate dielectric, completing the process.

Arrays of top-gated CNTFETs can be fabricated on the same wafer, since the gate contacts are electrically isolated from each other, unlike in the back-gated case. Also, due to the thinness of the gate dielectric, a larger electric field can be generated with respect to the nanotube using a lower gate voltage. These advantages mean top-gated devices are generally preferred over back-gated CNTFETs, despite their more complex fabrication process.

c) *Wrap-around gate CNTFET's*

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs were developed in 2008 [3],and are a further improvement upon the top-gate device geometry. In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.

Fig 3: Sheathed CNT

Device fabrication begins by first wrapping CNTs in a gate dielectric and gate contact via atomic layer deposition [4]. These wrapped nanotubes are then solution-deposited on an insulating substrate, where the wrappings are partially etched off, exposing the ends of the nanotube. The source, drain, and gate contacts are then deposited onto the CNT ends and the metallic outer gate wrapping.

d*) Suspended CNTFET's*

Geometry of CNTFET devices involves suspending the nanotube over a trench to reduce contact with the substrate and gate oxide [5]. This technique has the advantage of reduced scattering at the CNT-substrate interface, improving device performance [5] [6] [7]. There are various methods used to fabricate suspended CNTFETs, ranging from growing them over trenches using catalyst particles [5], transferring them onto a substrate and then under-etching the dielectric beneath [7], and transfer-printing onto a trenched substrate [6].

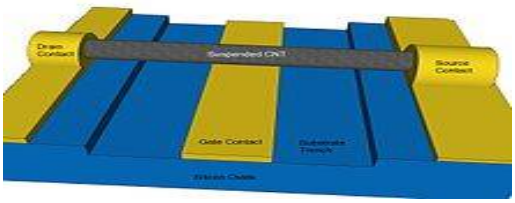

Fig 4: Suspended CNTFET device.

The main problem suffered by suspended CNTFETs is that they have very limited material options for use as a gate dielectric (generally air or vacuum), and applying a gate bias has the effect of pulling the nanotube closer to the gate,

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which places an upper limit on how much the nanotube can be gated. This technique will also only work for shorter nanotubes, as longer tubes will flex in the middle and droop towards the gate, possibly making touching the metal contact and shorting the device. In general, suspended CNTFETs are not practical for commercial applications, but they can be useful for studying the intrinsic properties of clean nanotubes[4].

III. ANOTHER FORMS OF CNTFET

The CNTFET technology is at an early stage; devices structures are still primitive and the devices physic still relatively unexplored. So, other the most popular Back Gate and Top Gate structures, some of the researcher also proposed their own structure such as N-Type, AMBIPOLAR CNTFET, Vertical Gate, and etc. to prove the performance of the transistor is better after the channel of the transistor replaced by CNT. Below are several examples of the differences structure of CNTFET.

1.2.1 N-Type and AMBIPOLAR CNTFET

The ability to produce n-type transistors is important technologically, as it allows the fabrication of CNT-based complementary logic devices and circuits. A back gated n-type nanotube transistor can be obtained by doping the nanotube with potassium vapor. The mechanism is that electron transfer from adsorbed potassium atoms to the nanotube can shift the Fermi level of the tube from the valence-band edge to the conduction band edge, thus reverting the doping from p- to n-type. [8] Fig.5 shows the schematic of setup for doping and the resulting I-V characteristics.

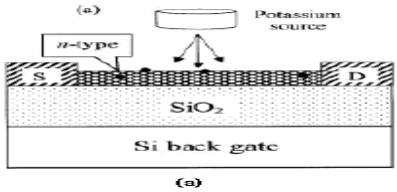

Fig 5: Schematic diagram of the potassium doping setup.

An n-type top gate device can be obtained by an in situ annealing step prior to the deposition of the gate dielectric film. Thermal treatment in an inert atmosphere drive off the adsorbed oxygen from the source and drain contact regions, shifts the Fermi level at the contacts and effectively lowers the barrier for electron injection, which results in an n-type behaviour. The oxide film protects the nanotube from the ambient gases and keeps the n-type devices stable.

If a CNTFET with SiO_2 protective film is annealed in vacuum or in inert atmosphere, the initial p-type device is gradually transformed into an ambipolar FET, i.e., the device, depending on the sign of the gate voltage VG, can operate as switches for electrons and holes. These ambipolar transistors are stable in air and show ohmic I-V_{DS} curves in both the strong hole accumulation and inversion (electron accumulation) regimes. This behaviour suggests that the effective contact barriers for both electron and hole transport are very small[5].

1.2.*2 Multi WALL CNTFET*

The complexity of structure of multi wall nanotube (MWNT) has discouraged their detailed study and use. In principle, each of its carbon shells can be metallic or semiconducting with different chilarities. Also, these shells can interact. It has been found that in MWNTs side-bonded to metal electrodes, effectively only the outer shell contributes to electrical transport. One would therefore expect that MWNTs with semiconducting outer shell can be used to fabricate CNTFETs. However, since the bandgap in semiconducting CNTs is inversely proportional to the tube diameter, only small diameters MWNTs are expected to exemplify FET characteristics at room temperature. [9]

1.2.*3 Vertical CNTFET*

This vertical Carbon Nanotube FET has been proposed by the researcher in Infineon Technology. The concept is totally difference compared to traditional MOSFET vertical gate configuration. Fig.6 showed the first draft of the Vertical CNTFET proposed by Infineon in year 2003. [10]

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IV. CHARACTERISTICS OF CNTFET'S

The drain I-V characteristics in 2D are shown in fig 7. The saturation current at V_{GS} = 0.5 V is around 6 μA, which is not inconsistent with values emerging from recent experimental work [9].

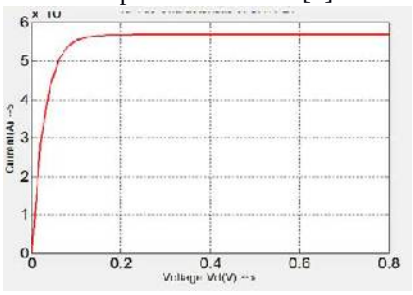

Fig 7: Drain current-voltage characteristics of planar CNTFET.

Drain I-V characteristics exhibited dependence of saturation drain current on temperature. When CNTFET is cooled, drain saturation currents were lightly decreased.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of CNTFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}]$$

Or

$$I_d = K_n\left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right] ,$$

Where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, C_{ox} is gate capacitance.

We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n(V_{gs} - V_T)^2 .$$

V. VOLTAGE CURRENT CHARACTERISTICS

As the voltage across the gate and the source of SB-CNTFET is increased from 0 volts, the Fermi level of the nanotube moves closer to the conduction band. This band lowering effect causes barriers to develop at nanotube-metal junctions. The electrons which have enough potential will cross the barrier and flow into the tube, causing leakage current. In our model, the main source of leakage is the thermionic current. When a positive voltage is applied on the drain, the barrier spike begins to progressively diminish at that end of the channel. The barrier thickness, as seen by the charge carriers, begins to reduce too. Consequently, the electrons induced on the channel can now enter the drain metal by tunnelling through the barrier while those carriers with sufficient thermal energy can jump over the barrier. The limiting value of current through the nanotube is described by the thermionic current component.

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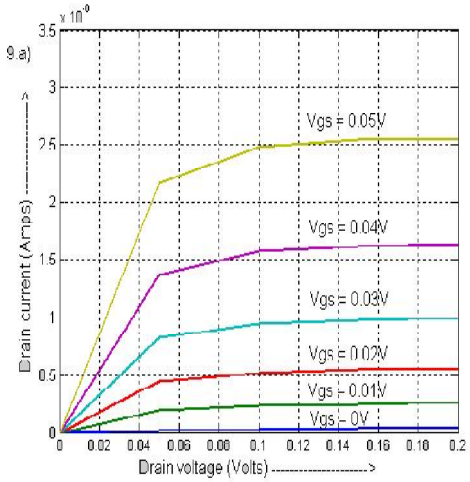

Fig 10: CNTFET sub threshold Drain characteristics

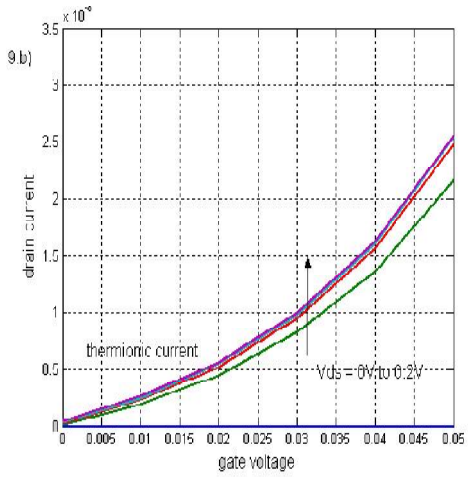

Fig 11: CNTFET sub threshold Transfer characteristics

We can see from Fig. 10 that for a given V_{gs}, the current saturates at the region, i.e., when the applied $V_{ds} \approx$ generate the transistor I-V characteristics and their dependence on the gate dielectric thickness and nature of the insulator barrier height. At this point the barrier is entirely suppressed and there is maximum current flow through the channel. Fig. 11 shows an almost linear increase in the current as a function of the gate voltage. The onset of current saturation as a function of drain voltage is expressed very clearly here. The plot consists of 5 curves for Vds ranging from 0 - 1 V. However, while there is a marked increase in the current for an increase of V_{ds} from 0.1V to 0.3V, beyond this limit, all the other curves representing the higher values of V_{ds} are almost merged. The electron current beyond this point is independent of V_{ds}.

VI. Conclusion and Future Work

The Carbon Nanotubes are considered as the most promising carbon nanostructure material is realizing the nano-electronic transistors back in year 1991. The understanding of carbon nanotube transistor is evolving and the performance of the transistor is improving very rapidly. CNTFET devices present a bright future and promise to sustain FET scaling and Moore's Law should their practical and manufacturing problems be overcome.The V-I characteristics of top gated CNTFET are also described. The main analysis is studies on the I-V characteristics of the CNTFET. These top gated CNTFET devices exhibit excellent electrical characteristics. However, as was mentioned above, the control parameter of the properties of the carbon nanotube will change the drain current directly and the channel length does not impacting the performance much. A multitude of oxide can be placed on the nanotube and thus, many high-k dielectrics can be incorporated into CNTFET to reduce the tunneling current. The large potential of CNTFET transistor to semiconductor industry and microelectronic system due the large I_{on}: I_{off} , high current drive and other special properties of carbon nanotube. However, the carbon nanotube field still in the early stage and the technology for reducing the process variation should be focused for this moment.

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BIOGRAPHY

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