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# Review of Digital Approximate Multiplier for AI-VLSI Applications

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**ABSTRACT:** The artificial intelligence techniques based VLSI applications are currently developing. The performance of FPGA-VLSI processor is depends on the digital signal processing operation speed. Digital multiplier is one of the key operations of the ALU of processor. The Xilinx seven series logic FPGA VLSI processor are using under 5G constraints. Research are continue going on various existing multipliers for enhancing in terms of performance improvement like high speed, low delay, low area, low power etc. This paper presents the reviews of architecture, performance, challenges of the approximate multiplier for VLSI-AI applications.

**KEYWORDS:** VLSI, Approximate, Multipliers, Delay, Power, Area, Speed.

## I. INTRODUCTION

Arithmetic units such as adders and multipliers are key components in a logic circuit. The speed and power consumption of arithmetic circuits significantly influence the performance of a processor. High-performance arithmetic circuits such as carry look ahead adders (CLAs) and Wallace tree multipliers have been widely utilized. However, traditional arithmetic circuits that perform exact operations are encountering difficulties in performance improvement. Approximate arithmetic that allows a loss of accuracy can reduce the critical path delay of a circuit. Since most approximate designs leverage simplified logic, they tend to have a reduced power consumption and area overhead. Thus, approximate arithmetic is advocated as an approach to improve the speed, area and power efficiency of a processor due to the error-resilience of some algorithms and applications [1]. As an important arithmetic module, the multiplier has been redesigned to many approximate versions. The often conflicting advantages and disadvantages of these designs make it difficult to select the most suitable approximate multiplier for a specific application. Thus, approximately redesigned multipliers are reviewed in this paper and a comparative evaluation is performed by considering both the error and circuit characteristics.

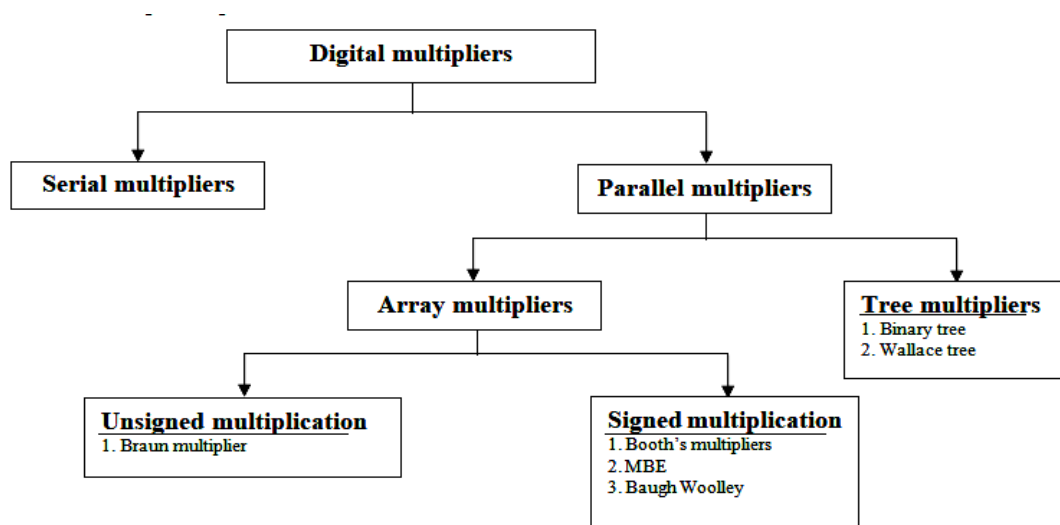


Figure 1: Types of Multiplier

Approximate computing has emerged as a potential solution for the design of energy-efficient digital systems [1]. Applications such as multimedia, recognition and data mining are inherently error-tolerant and do not require a perfect accuracy in computation. For these applications, approximate circuits may play an important role as a promising alternative for reducing area, power and delay in digital systems that can tolerate some loss of accuracy, thereby achieving better performance in energy efficiency. As one of the key components in arithmetic circuits, adders have been extensively studied for approximate implementation.

## II. LITERATURE SURVEY

**P. J. Edavoor, et al.**, presents the designs which are implemented using 45 nm CMOS technology and efficiency of the proposed designs have been extensively verified and projected on scales of area, delay, power, Power Delay Product (PDP), Error Rate (ER), Error Distance (ED), and Accurate Output Count (AOC). The proposed approximate 4:2 compressor shows 56.80% reduction in area, 57.20% reduction in power, and 73.30% reduction in delay compared to an accurate 4:2 compressor. The proposed compressors are utilised to implement  $8 \times 8$  and  $16 \times 16$  Dadda multipliers. These multipliers have comparable accuracy when compared with state-of-the-art approximate multipliers. The analysis is further extended to project the application of the proposed design in error resilient applications like image smoothing and multiplication [1].

**F. Sabetzadeh, et al.**, presents the ultra-efficient imprecise 4:2 compressor and multiplier circuits as the building blocks of the approximate computing systems are proposed. The proposed compressor uses only one majority gate which is different from the conventional design methods using AND - OR and XOR logics. Furthermore, the majority gate is the fundamental logic block in many of the emerging majority-friendly nanotechnologies such as quantum-dot cellular automata (QCA) and single-electron transistor (SET). The proposed circuits are designed using FinFET as a current industrial technology and are simulated with HSPICE at 7nm technology node. The results indicate that our imprecise compressor is superior to its previous counterparts in terms of delay, power consumption, power delay product (PDP) and area, and improves these parameters on average by 32%, 68%, 78%, and 66%, respectively [2].

**H. Saadat, et al.**, presents approximate multipliers enable the saving of area and power for implementation of many modern error-resilient compute-intensive applications. In this work, it is first propose a novel error-configurable minimally biased approximate integer multiplier MBM design. The proposed MBM design is devised by coupling a unique error-reduction mechanism with an approximate log based integer multiplier. Next, it is propose an optimization (by removing leading-one detection and barrel shifting logic) of the MBM and a class of state-of-the-art approximate integer multipliers DRUM and SSM, so that they can be efficiently used in approximate floating-point (FP) multipliers [3].

**W. Liu, et al.**, presents approximate Booth multipliers are designed based on approximate radix-4 modified Booth encoding (MBE) algorithms and a regular partial product array that employs an approximate Wallace tree. Two approximate Booth encoders are proposed and analyzed for error-tolerant computing. The error characteristics are analyzed with respect to the so-called approximation factor that is related to the inexact bit width of the Booth multipliers. Simulation results at 45 nm feature size in CMOS for delay, area and power consumption are also provided. The results show that the proposed 16-bit approximate radix-4 Booth multipliers with approximate factors of 12 and 14 are more accurate than existing approximate Booth multipliers with moderate power consumption [4].

**A. Mokhtari, et al.**, considers decentralized consensus optimization problems where nodes of a network have access to different summands of a global objective function. Nodes cooperate to minimize the global objective by exchanging information with neighbors only. A decentralized version of the alternating directions method of multipliers (DADMM) is a common method for solving this category of problems. DADMM exhibits linear convergence rate to the optimal objective for strongly convex functions but its implementation requires solving a convex optimization problem at each iteration. This can be computationally costly and may result in large overall convergence times [5].

**B. Shao et al.**, it is propose a general model for array-based approximate arithmetic computing (AAAC) to guide the minimization of processing error. As part of this model, the Error Compensation Unit (ECU) is identified as a key building block for a wide range of AAAC circuits. It is develop theoretical analysis geared towards addressing two critical design problems of the ECU, namely, determination of optimal error compensation values and identification of the optimal error compensation scheme. it is demonstrate how this general AAAC model can be leveraged to derive practical design insights that lead to optimal tradeoffs between accuracy, energy dissipation and area overhead [6].

**Z. Zhi-Qing Lü et al.**, the method formulates a reduced-order interface problem, which can be solved using an iterative algorithm. Once the resulting interface problem is solved, the unknown electric field in each subdomain can be calculated in parallel. Numerical examples are given to demonstrate the efficiency of the method [7].

**D. De Caro, et al.**, present an in-depth analysis of the maximum absolute error (MAE) of these circuits. The MAE is the main parameter to be considered in important applications, like function evaluation. It describes an efficient numerical method to compute the MAE in fixed-width multipliers and fixed-width multiplier-accumulator (MAC) circuits. Further it is present a technique to compute a compensation function that can be efficiently implemented in hardware, aimed to minimize the MAE [8].

**F. Auger et al.**, Many signal processing algorithms require the computation of the ratio of two numbers, the square root of a number, or a logarithm. These operations are difficult when using fixed point hardware that lack dedicated multipliers, such as low-cost microcontrollers, application specific integrated circuits (ASICs), and field programmable gate arrays (FPGAs). This article presents straightforward, multiplier free algorithms that implement both division and square roots, based on a technique known as dichotomous coordinate descent (DCD) [9].

**I. Park et al.**, presents square and square-root are widely used in digital signal processing and digital communication algorithms and their efficient realizations are commonly required to reduce the hardware complexity. In the implementation point of view, approximate realizations are often desired if they do not degrade performance significantly. In this paper, we propose new linear approximations for the square and square-root functions [10].

**M. Rentzsch et al.**, the converter circuit is briefly described. A model for the dynamic behaviour of the Walton Cockcroft multiplier is developed via state space modelling in the discrete time domain, which then allows it to be approximated as a low-pass filter with parameters that are a function of the converter operating point. The analytical model of the converter is based on the extended describing function and the generalised averaging technique [11].

**J. W. Hauser et al.**, this work addresses the problem of efficiently approximating a function for systems-on-a-chip and other FPGA applications, in these systems, high speed, minimal chip size, and efficient computation are necessary. The specific runtime algorithm implementation used to evaluate the set of 3rd degree polynomials is directly dependent on the hardware available and the tradeoffs are discussed. Specifically, we present an efficient multiplier-less method of evaluating the 3rd degree polynomials based on logarithms targeted for FPGA applications [12].

### III. ADVANTAGES AND CHALLENGES

#### Advantages of Approximate Multipliers

- Incorrect reading is obtained when the noise signal is occurred.
- The filter is used to reduce the noise signal which also reduces the total speed of operation.
- The accuracy of the whole system is depends on accuracy of digital to analog converter and accuracy of internal reference supply.
- The speed of operation is restricted. The speed is depends on which type of switches are used.
- The conversion time required for digital to analog converter.
- This method is very systematic.
- This method takes lesser time in solving transportation problem.
- Less computation are involved in these methods.

#### Challenges

- Iterative channel decoders such as Turbo-Code and LDPC decoders show exceptional performance and therefore they are a part of many wireless communication receivers nowadays.
- The implementation cost of traditional soft-output de mapping methods is relatively large in high order modulation systems, and therefore low complexity de mapping algorithms are indispensable in low power receivers.

- In the presence of multiple wireless communication standards where each standard defines multiple modulation schemes, there is a need to have an efficient architecture covering all the flexibility requirements of these standards.

#### IV. CONCLUSION

This paper presents review of various approximate multiplier technique of previous research. Therefore it is clear that such multiplier is designed and implemented for high speed in various applications. 16-bit and 32-bit multipliers is designed and tested. In future we implement 64-bit approximate multiplier using verilog coding on xilinx 14.7 software. Implementation will be helpful for advance digital signal applications with improved performance.

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