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Low Power Hybrid Full Adder Using Transmission Gates

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ABSTRACT: Addition is a fundamental operation for all the arithmetic operations; it is mainly used in digital signal processing architecture and microprocessor. The sum module is a core of arithmetic operation like addition, subtraction, multiplication and division. The aim of this project is to design a full adder having low power consumption and delay. Here, a new hybrid 1-bit full adder is designed using both CMOS (Complementary metal oxide semiconductor) logic and transmission gate logic for the purpose of reducing the number of transistors. This design was implemented for 1-bit and then extended for 32-bit. This circuit is implemented using Synopsis tools in 35-nm technology. In comparison with existing full adder designs, the present implementation is improved in terms of power and area.

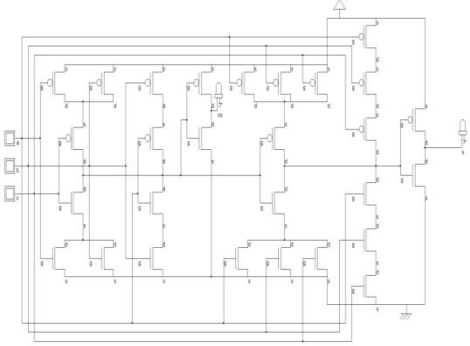
KEYWORDS: CMOS logic, high speed, hybrid design, low power, Transmission-gate.

I. INTRODUCTION

The process of creating thousands of transistors are combined to a single integrated chip is a very large scale integration. Using low power components with low power design is more valuable. Full adders Full adders, being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years [1], [2]. Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells [3]. The designs are classified into two categories static style and dynamic style. Static full adders are more reliable with less power but on chip area is large compared to dynamic style.

Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS) [3], dynamic CMOS logic [4], complementary pass-transistor logic (CPL) [5], [6], and transmission gate full adder (TGA) [7], [8] are the most important logic design styles in the conventional domain. Hybrid technologies are used for designing the full adders in more than one different style. This improvement in power, delay and layout area was obtained using this logic style.

II. LITERATURE SURVEY



Fig(1): Full Adder using CMOS transistors

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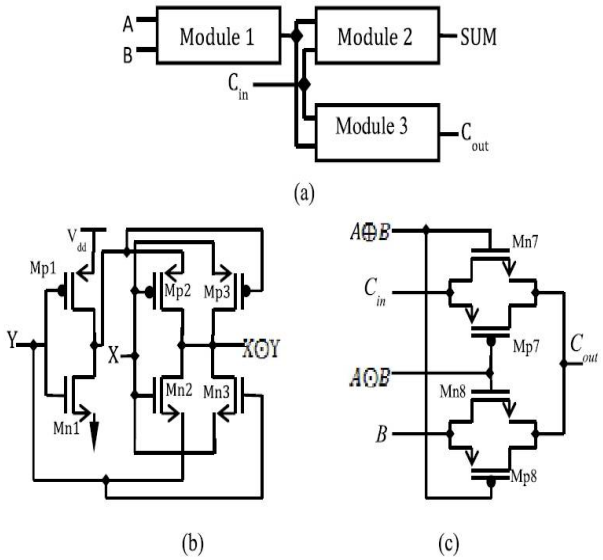
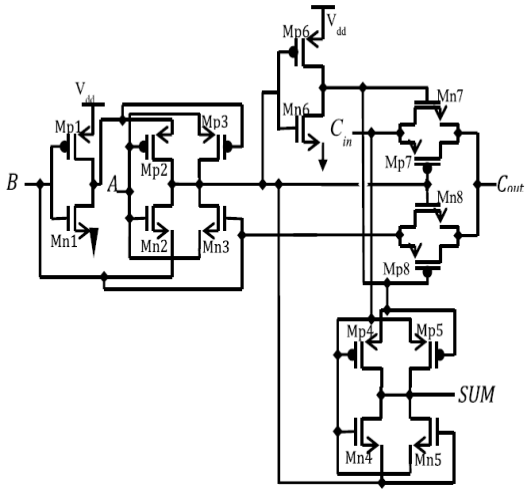
The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers [3].

III. PROPOSED FULL ADDER



Fig(2) : (a) Schematic structure of proposed full adder (b) XNOR module (c) carry generation module

The proposed full adder is represented by three modules as shown in fig(a). Module 1 and Module 2 are the XNOR modules that generates sum signal (SUM) and Module 3 generates the output carry signal (C_{out}). XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.



Fig(3): Detailed circuit diagram for proposed full adder

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The inverter is formed using transistors Mp1 and Mn1 generate signal B, which is used to implement the controlled inverter using the transistor pair Mp2 and Mn2. Output of this inverter is XNOR of A and B. It has voltage degradation problem which is eliminated using two pass transistors Mp3 and Mn3. PMOS (Mp4, Mp5, Mp6) transistors and NMOS (Mn4, Mn5, Mn6) transistors are form the second stage XNOR module to realize the complete sum function. In this circuit the output carry signal is implemented by the transistors Mp7, Mp8, Mn7 and Mn8. The input carry signal propagates through a transmission gate (Mp7 and Mn7), in order to reduce the overall carry propagation path significantly. The use of these gates are responsible for reduction in propagation delay of the carry signal.

The given hybrid adder requires only 16 transistors whereas the other hybrid adders require more than 20 transistors. By analyzing the truth table of a full adder, the condition for C_{out} is:

If A=B, then C_{out}=B else C_{out}=C_{in}

IV. PERFORMANCE OF CARRY LOOK AHEAD ADDER USING TRANSMISSION GATES

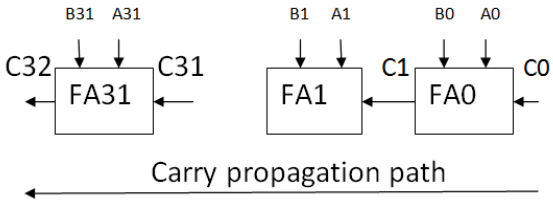
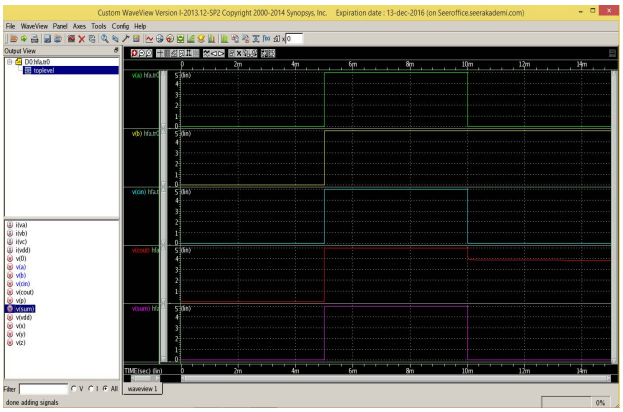


Fig (4) 32 bit carry propagation adder using hybrid adder design

A 32-bit carry propagation adder [fig(4)] is implemented as an extension of the hybrid full adder. It is a non carry look-ahead adder structure where the carry propagation takes place to all the way to the last adder block. Here both the power consumption as well as carry propagation was also improved. The power obtained for this adder is 1.06e-04

V. EXPERIMENTAL RESULT

CMOS 28T full adder, hybrid full adder have been successfully implanted using h-spice in synopsis tool. A 35-nm technology libraries is used in this tool. The results are obtained as follows:



Fig(5) Output waveform for hybrid full adder circuit

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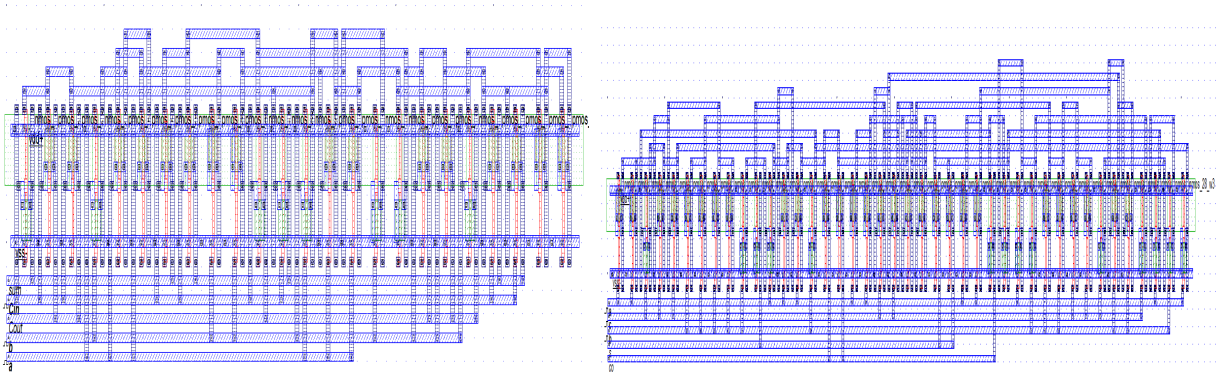

Fig(6) i. Layout for hybrid full adder circuit ii. Layout for CMOS 28T full adder

The figures fig(6), (i) and (ii) shows the layout of a proposed full adder and existing full adder respectively. The number of transistors for the proposed hybrid full adder is 16 and the existing full adder is 28. Hence, by observing the layouts of these adders area will be decreased. With an aim to optimize power of the circuit, the energy consumption has been minimized in the proposed case. It was observed that in the present design the power consumption could be minimized by mainly sizing the transistors in inverter circuits, while the carry propagation delay could be improved by mainly sizing the transistors of the transmission gates paths between C_{in} and C_{out}. The proposed hybrid adder requires 16 transistors whereas the other hybrid adder requires more than 20 transistors. The use of less number of transistors in this paper also improves speed. The power comparison for different logics has been showed in Table(1).

Designs	Power	No. of transistors
CMOS	7.5e-04	28
CPL	1.759µ	32
HPSC	1.56µ	22
TGA	1.76µ	20
FA HYBRID TGL (Proposed)	6.864e-05	16

Table (1): power comparisons for adders

VI. Conclusion and Future Work

Full adder is used in digital signal processors (DSP) and microprocessor. There is also an increasing demand for mobile electronic devices such as cellular phones, PDA's and laptop computers. In this paper, a low power hybrid full adder has been proposed the design has been extended for 32 bit carry look ahead adder also. The simulation was carried out using synopsis tools with 35-nm technology and compared with CMOS design. By using this hybrid logic

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design, power is reduced. This paper can be further implemented with pass transistor logic for better power performance.

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BIOGRAPHY

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