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A Review on VLSI based DSRC application of FM0/Manchester encoder-decoder

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ABSTRACT: In the communication system the secure data transmission is very important. Numbers of encoding techniques are used for the communication of data. Several types of applications such as FM0, miller and Manchester encoding are used for the communication which provides the security to the data. These techniques have their own importance that depends on its application and their needs. These techniques are very strong as they provide the result without losing their parameters. Generally these encoding techniques provide the output using FSM (finite state machine) at high speed. Architecture of FM0, Manchester and miller encoding are used to balance the DC output. This is the main advantage of using these techniques. There architecture requires reduced number of the transistors in the design implementation. In this paper a brief review on is presented on VLSI based DSRC (dedicated short-range communication) application of FM0/Manchester encoder-decoder.

KEYWORDS: DSRC, FM0 encoder, FPGA, VLSI, Manchester encoder, SOLS.

I. INTRODUCTION

Encoding technique is used in the communication system to convert the information of data into the suitable form of transmission. Encoding techniques are used for the purpose of security. Different encoding techniques used for the serial communication application. The several types of applications such as FM0, Manchester encoding, Miller encoding, NRZ, FM1, RZ, etc. are used for encoding the data. These encoding techniques can also be used in the optical communication; it minimizes the critical area and path-delay by adding buffers in the path of the signals. A baseband processor consists of a PIE reader, UHF/RFID Reader and a decoder (FM0 or Miller or other) for encoding and decoding purpose application at a high frequency clock. The architecture system of DSRC transceiver is as shown in Fig 1.

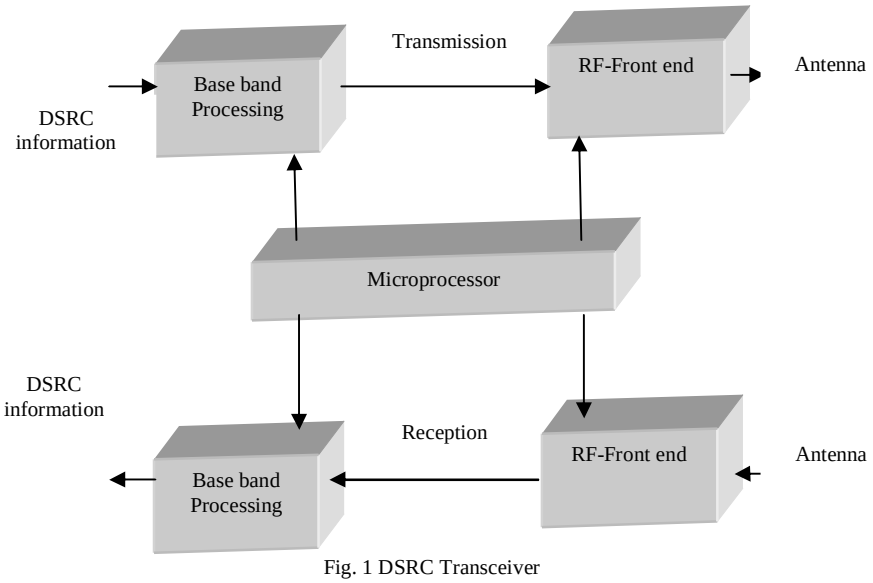

Fig. 1 DSRC Transceiver

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The architecture system of dedicated short range communication (DSRC) transceiver is shown in Figure 1. The upper part dedicated for transmission and bottom parts are dedicated for receiving the information. The transceiver is classified into three modules: baseband processing, microprocessor, and RF front-end. The instructions of microprocessor interpret to schedule the tasks of baseband processing and RF front-end from media access control. The baseband processing is dependable for the error correction, modulation, and encoding and clock synchronization. The RF frontend transmits and receives the wireless signal through the antenna.

II. RELATED WORK

In [1], [5] author proposed fully reused VLSI (Very Large Scale Integration) architecture by using SOLS technique for both the FM0 and Manchester encoding. The SOLS technique eliminates the limitations of hardware utilization by using two core techniques- (1) Area compact retiming and (2) Balance logic-operation sharing techniques. The Area-compact retiming is used to reduce the hardware problem like number of transistors and the balance logic operation sharing the help identical logic components can be efficiently combines with the FM0 and Manchester encoding. In this paper the proposed method works on parameters like low power consumption, high operating frequency etc. This paper develops a fully reused VLSI architecture and also exhibits a competitive performance compared with the existing works.

In [2], it is shown that an unbalance computation time results in the glitch at the input of MUX that causes the logic-fault on coding. This paper overcomes the problem of glitches by using XNOR with the inverter by replacing the XOR and this becomes the input of the MUX. This is done to balance the computational time. The adoption of FM0 or Manchester code depends on Mode and CLR signal. In this design both modes are separately allocated to system controller. Whether FM0 or Manchester code is adopted, all the logic component of the proposed VLSI architecture is utilized and provides better results. The work in [3] presents a review on Manchester, Miller and FM0 encoding techniques. This paper presents the circuit design strategies of Manchester, Miller and FM0 using a finite state machine. A comparative study of all these techniques is also presented in this work.

A review on theoretical background of FM0 and Manchester [4] is presented describing the utility of FM0 and Manchester encoding and how it can be used for DSRC. In DSRC DC-Stability and signal reliability are fulfilled by FM0 and Manchester. These works presents a system of VLSI architecture of FMO/ Manchester encoding using SOLC technique and also compare this technique with other techniques. The SOLS consists of two core methods such as area-compact retiming and balance logic-operation sharing. The area-compact retiming technique relocates the hardware resource to reduce transistors. The balance logic operation sharing technique of SOLC efficiently combines FM0 and Manchester encodings with the fully reused hardware architecture. This paper not only implements a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing techniques. In [6] presents a review on evaluation of various forms of DSRC system. DSRC is the only short-range wireless alternative today that provides Fast Network Acquisition, Low Latency, High Reliability when Required, Priority for Safety Applications, Interoperability, Security and Privacy which is one of the challenging task faced by all in the worldwide. This article deals with active Dedicated Short Range Communications (DSRC) application for Intelligent Transport Systems (ITS) and its economic evaluation focused on many wireless systems like vehicle communication, mobile Communication etc.

In [7] proposed a fully reused VLSI architecture using the SOLS technique for both FM0 and Manchester encoding. The SOLS technique eliminates the limitation of hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98×30.43 μm2. This paper not only develops a fully reused VLSI architecture and also exhibits an efficient performance compared with the existing works.

In [8] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings. The coding diversity between FM0, Manchester and Miller encodings causes the limitation on hardware utilization of VLSI architecture design. The area compact retiming and balance logic operation sharing techniques eliminates the limitation of hardware utilization. Area compact retiming concept relocates the hardware resource and reduced the

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number of transistors effectively. The Balance Logic operation sharing technique combines FM0 and Manchester encodings with the identical logic components to produce balanced computation time. Every component is active in both FM0 and Manchester encodings and it will greatly improve the hardware utilization rate to 100% and reduce the power consumption. The FM0 and Manchester encoders are designed with these techniques to achieve high speed and fully reconfigured VLSI architecture for application system. In future the design can be implemented using high performance FPGA devices.

In [9] proposed a system to minimize the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistor and by combining the resources of FM0 and Manchester encodings. This paper is realized in 180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for Manchester encoding and FM0 encoding.

In [10] proposed the SOLS technique to overcome the problem on hardware utilization of VLSI design used for the DSRC dedicated short-range communication. The DSRC standards typically adopt FM0 and Manchester codes to succeed in dc-balance, enhancing the signal irresponsibleness. Still, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to style a completely reused VLSI design for each. The SOLS technique improves the hardware utilization rate from fifty seven.14% to 100% for each FM0 and Manchester encodings. In [11] proposed a method for power reduction in VLSI architecture using FM0 and Manchester encoding. Power is reduced by reducing the number of components used and improves the performance of the FM0 and Manchester encoding. These results are observed by using spice. The power consumed is 0.72 mw for Manchester encoding. The power consumption is 0.14 mw for FM0 encoding. The FM0 and Manchester encoding is widely used in dedicated short range communication. Signal reliability could be achieved in dedicated short range communications by adopting FM0 and Manchester encoding.

In [12] author present the shows the encoding technique of FMO and Manchester with SOLS technique eliminates the limitation of hardware utilization by two core techniques (a) Area Compact of Retiming (b)Sharing of Logic Operation. Using compact of area retiming, the number of transistor is reduce to 22 transistors. The sharing of logic operation combines FMO and Manchester encodings. The maximum operating frequency of Manchester, FMO encodings are 2 GHz, 900MHz and consumption of power is 1.58mW, 1.14mW respectively..

In [13] the paper presents coding diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. The fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings are proposed. Which can eliminates the limitation on hardware utilization. The ACR technique relocates the hardware resource to reduce the transistor count.

BLOS efficiently combines the FM0 and Manchester encodings with the identical logic components. The SOLS technique improves the Hardware Utilization Rate (HUR) from 57.14% to 100% for both FM0 and Manchester encodings. The balanced hardware architecture is realized in different CMOS technology this paper not alone develops a fully reused VLSI architecture and also exhibits an efficient performance compared with the existing works.

In [14] the limitation on hardware utilization of VLSI architecture design can be caused due to coding-diversity between FM0 and Manchester encodings. A limitation on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, SOLS technique is used fully reused VLSI architecture for both FM0 and Manchester encodings. The limitation on hardware utilization can be eliminating by using SOLS technique by two core techniques: area-compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the number of transistors. The balance logic operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components.

In [15] proposed SOLS technique to prevent wide code diversity that limits the hardware utilization rate of such a reusable encoder. To implement a system that has its own advantages like smooth traffic control, vehicular safety etc DSRC communication protocol is used this system encode the message and transmit it to other DSRC. The data is encoded using FM0 and Manchester encoding that causes the problem and it can be overcome by using SOLS technique. The SOLS encoder is of better advantage than the normal reusable encoder in terms of device utilization. Besides the logic delay and memory usage of the system also get reduced.

In [16] presents Miller encoding which is integrated with FM0 and Manchester encoding architecture for the application of Dedicated Short Range Communication (DSRC). These encodings have same similarities and clock rate embedded within the transmitted data. Using the similarities in the FM0, Manchester and Miller techniques, hardware

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architecture is developed by using SOLS technique. This paper develops a fully reused VLSI architecture and also exhibits a competitive performance compared with the existing works.

In [17] SOLS technique is introduced to solve the hardware utilization problem caused at the time when both the FM0 and Manchester encoding is used to encode the message in DSRC by considering two parameters area compact retiming and balance logic-operation sharing. This reduces the hardware setup problem by reducing transistor and combines FM0 and Manchester encodings with the identical logic components respectively.

In [18] in this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in 180nm technology with outstanding device efficiency. The power consumption is 29392.843nW for Manchester encoding and FM0 encoding.

III. CONCLUSION

The presented work exploits the design strategies of number of scholars and presents a brief of it. This review paper presents the common work that explain the entire circuits of FM0 encoder, Miller, Manchester and a FSM (finite state machine) for all three encoders which are designed by using VHDL (Verilog Hardware Description Languages). The concept of encoding will be used in various applications as future work.

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