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Optimization Techniques for Efficient FPGA Hardware Implementation on IRNSS User Receiver

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ABSTRACT: The Indian Regional Navigational Satellite System (IRNSS) is an autonomous regional satellite navigation system developed by Indian Space Research Organization (ISRO). This paper deals with different optimization techniques used for generation of SPS gold codes in IRNSS user receiver. We have used Xilinx ISE 14.7 for achieving design, code and tool optimisation goals. This paper also discusses the most efficient FPGA hardware to be implemented on IRNSS user receivers for faster processing of data for user interfacing.

KEYWORDS : Indian Space Research Organization (ISRO),Indian Regional Navigational Satellite System (IRNSS), Xilinx ISE, SPS Gold codes, Optimization.

I. INTRODUCTION

Indian Space Research Organization (ISRO) has developed a satellite based navigation system, known as Indian Regional Navigation Satellite System (IRNSS), with a constellation of 7 satellites. It is a regional system being developed by India for positioning servicesover India and the region extending to 1,500 kilometres around India. The IRNSS consists of 3 segments: Space segment, ground segment and user segment. The satellites will be placed in two different orbital planes; 3 satellites in the Geostationary orbit (GEO) and 4 satellites in the Geo-synchronous orbit (GSO). The satellites transmit navigation signals in both the L5 band and the lower S-band, used to provide accurate real-time positioning and timing services over India. IRNSS will provide two levels of service, the standard positioning service(SPS) will be open for civilian use, and a restricted service(RS) for restricted/authorized users.

IRNSS system performances expected are: Position accuracy around 20 m over the Indian Ocean Region (1500 km around India) and less than 10 m accuracy over India and GSO adjacent countries. The navigation signals which are transmitted are in the S-band frequency of 2–4 GHz and is broadcasted through a phased array antenna for better coverage and signal strength. 24 hours navigational support provided by IRNSS satellite for all land, sea and air users over Indian and Asia-Pacific regions. IRNSS has high accuracy in position, time and velocity information in real time applications for different types of vehicles. The communication by the IRNSS trans-receiver has the frequency bands of L5 (1176.45 MHz) and S (2492.08 MHz).

In this paper, an overview is presented on the status of current investigations relating to the optimization of methods with respect to the code optimization, the design models, and tool optimization techniques applicable to IRNSS and its combination with other measuring systems. Reference to practical results is made to illustrate how the continuous refinement of such methodologies can lead to the continuous improvement in the accuracy of baseline determinations and satellite orbits, achievable under most observing conditions.Undoubtedly, as contemporary IRNSS receiver technology improves and the number of available satellites increases, IRNSS-based systems will be used for a wide variety of surveying and geodetic activities ranging from efforts to support uniform topography mapping and the growing need for better geodetic control for multipurpose cadaster systems (Ethridge, 1988) to precise geodynamic measurements and precise low-Earth satellite tracking.

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II. PROPOSED IRNSS USER RECEIVER

The main objective of the IRNSS user receiver is to simultaneously acquire signals from all the IRNSS satellites using best satellites geometry of configured constellations with respect to GDOP & Signal strength to provide the PNT(position, navigation and time) solution to display the outputs. The User Receivers has capability to receive IRNSS frequency accurately. Radio frequency (RF) signals are received IRNSS satellite from the antennas the input signal is amplified to the required amplitude, the signals are then down converted to two-level of intermediate frequencies and the frequency is converted to a desired output frequency. An analog-to-digital converter (ADC) is used at the output signal end to digitize the signal. Further processing of signals is done using a baseband processor. SPS uses the bi-phase shift keying BPSK [1] modulation, whereas the RS service will employ binary offset carrier modulation. The transmission is done using the L-band and S-band in right-hand circularly polarized (RHCP) helix array antenna to provide global coverage signals. Thus, user receivers can operate in both single-and/or dual frequency mode.

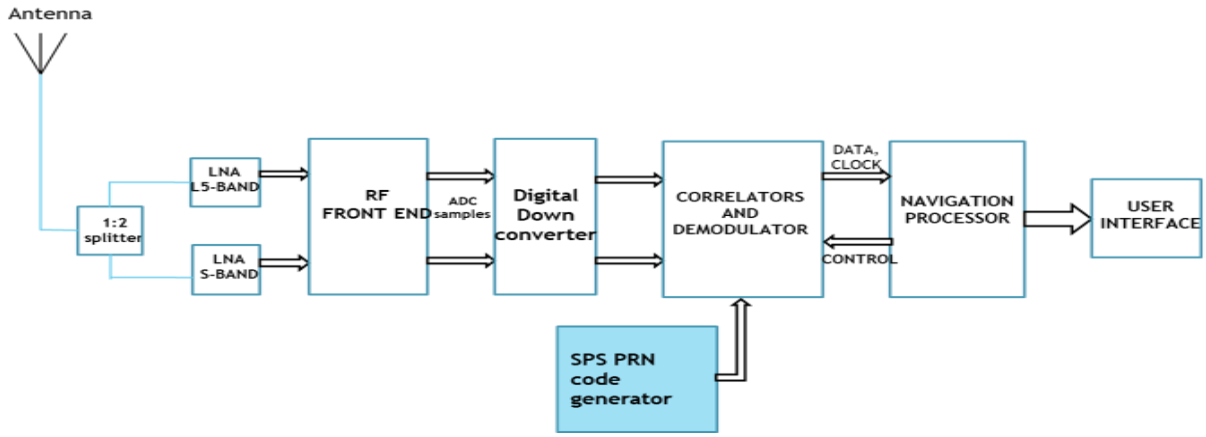

Fig.1 IRNSS proposed block diagram

Figure 1 shows the block diagram of IRNSS user receiver which consists of antenna, L5 and S band splitter, RF front end, digital down converter, correlators and de-modulator, navigation processor, user interface and SPS code generator.

III. OPTIMIZATION TECHNIQUES

Optimization is performed to achieve the best possible result under given boundaries. Software running in an FPGA must be often examined and should respond to a large number of input stimuli from many different sources because a processor is a time multiplexed resource, hence it cannot process these input signals in parallel form as done by hardware-based design processor. So, for computing a significant percentage of time is spent in traversing control structures and determining how to respond to a given set of inputs. In a high-level heavy control FPGA, it is possible that an application might end up spending more time in figuring out what to do than actually doing it.
There are mainly two types of optimization techniques. They are broadly divided into machine independent and machine dependent optimization.

3.1 Machine-independent Optimization

In this type of optimization, the compiler complies the code which is intermediate, it then changes the code in which CPU registers or absolute memory locations are not involved . Substantial run-time is overhead in a High-level language if we translate each construct independently into the machine code.

3.2 Machine-dependent Optimization

After the target code has been generated the code is transformed according to the target machine architecture and optimization is performed. The CPU registers may have absolute memory references rather than relative references. Machine-dependent optimizers puts efforts to take maximum advantage of the memory hierarchy.

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This paper discusses various ways in which techniques from the realm of hardware design can be applied to the optimization of control structures in software. First, two local optimization techniques, the design and tool optimization are presented. These allow for a more efficient evaluation for choosing the best hardware for implementation of SPS code for better functioning of IRNSS user receiver. Then, a general method for restructuring a software routine using design optimization discussed.

IV. CODE OPTIMIZATION

Optimum solution is found by using the classical optimization techniques. Optimization is a program transformation technique, which tries to improve the code by making it consume less resources such as CPU, Memory,etc and deliver high speed to the user.

We can covert a high-level general programming code into a low-level programming codes. While performing code optimizing process we must follow the underlying rules given:

- Meaning of the program should not be changed when the final output code is optimized.
- Speed of the program should increase and if possible, the program should also use lesser number of resources.
- There should not be any delay the overall compiling process and the processing speed should be fast.

The replacement and elimination of unnecessary instructions in object code by a faster sequence of instructions which does gets the same output is usually called "code optimization."

4.1 Optimization by Logic Network Simplification

We have optimized the SPS code using XILINX 14.7 by elimination of adding inputs manually as shown in Figure 2. Here we have used two initial value inputs for L5 band satellite hence which increased the memory consumed by the code which intron consumed more time to compute the PRN SPS codes.

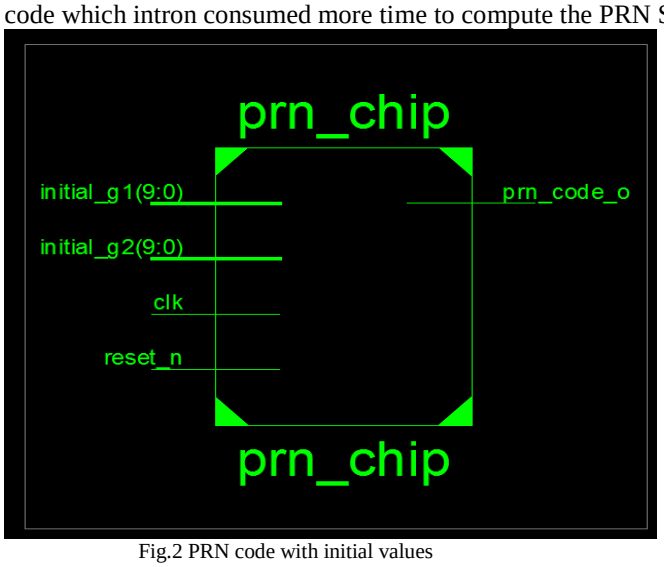

Fig.2 PRN code with initial values

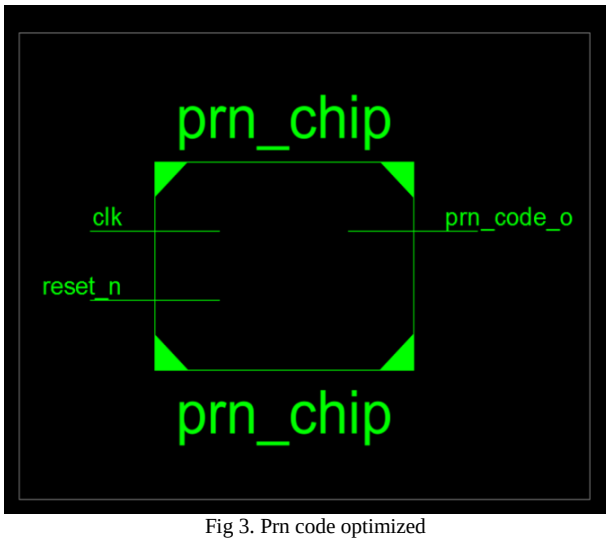

Fig 3. Prn code optimized

We can optimize this code by completely eliminating the initialization by taking it automatically by parallel programming.Figure 3 shows optimized prn code which used lesser memory and faster processing time.

V. TOOL OPTIMIZATION

There has been increasing need for high bandwidth, so system designers increased the resource utilization when designing with Virtex®-6 devices. With their in-built flexibility, Xilinx FPGAs are used mainly for high-performance or multi-channel digital signal processing (DSP) applications which takes advantage of hardware parallelism. Xilinx FPGAs gives comprehensive solutions for processing bandwidth, with easy-to-use design tools for software developers, hardware designers and system architects.

ISE software releases and up-to-date information on additional design techniques, Xilinx continues to enhance algorithms place and route to help users to optimize routing in their Virtex-6 FPGA designs hence making it easier to reach performance, power design goals and achieving the next-generation bandwidth requirements.

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TABLE I. COMPARISON OF DIFFERENT HARDWARE FPGAS

FAMILY	SPEED GRADE	CLOCK PERIOD (ns)	FREQUENCY (MHz)
Zynq	-3	1.006	993.641
	-2	1.141	876.271
	-1	1.361	734.754
Artix7	-3	1.313	761.55
	-2	1.420	704.325
	-1	1.585	630.915
	-2L	1.420	704.325
Automotive Zynq	-1I	1.250	800.000
	-1Q	1.250	800.000
Defence-Grade Zynq	-2I	1.128	886.368
	-1I	1.250	800.000
	-1Q	1.250	800.000
Kintex7	-3	1.006	993.641
	-2	1.141	876.271
	-1	1.361	734.754
	-2L	1.141	876.271
Spartan3E	-5	2.810	355.866
	-4	3.263	306.466
Virtex7	-3	1.006	993.641
	-2	1.141	876.271
	-1	1.361	734.754
	-2L	1.141	876.271
Space-Grade Virtex-4QV	-10	1.992	502.084

In this paper we have done software implementation of different FPGAs on XILINX 14.7 and made a comparison of their clock period and frequency. By comparing their speeds we can conclude the best hardware to implement the SPS codes of IRNSS user receiver. This optimized hardware receiver can compute all the processes and acquire data and position faster.

As we can see from the table 1 that the best hardware to implement the SPS code is ZYNQ as the Zynq-7000 has all Programmable SoC (AP SoC) family which integrates the software programmability of an ARM-based processor with the hardware programmability of an FPGA which enables the key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device. Consisting of single-core Zynq-7000S and dual-core Zynq-7000 devices, the Zynq-7000 family is the best price to performance-per-watt, fully scalable SoC platform for unique application requirements.

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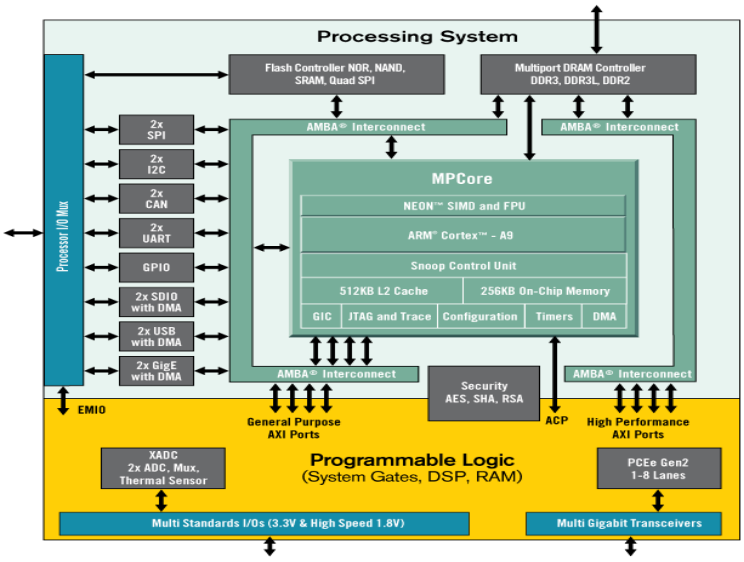

Fig 4. Block Diagram ZYNQ 7000

VI. DESIGN OPTIMIZATION

The purpose design objective can be to either minimize the cost of production or maximize the efficiency of the production. An optimization algorithm is a procedure in which we achieve efficiency by comparing various solutions till an optimum or a satisfactory solution is found.

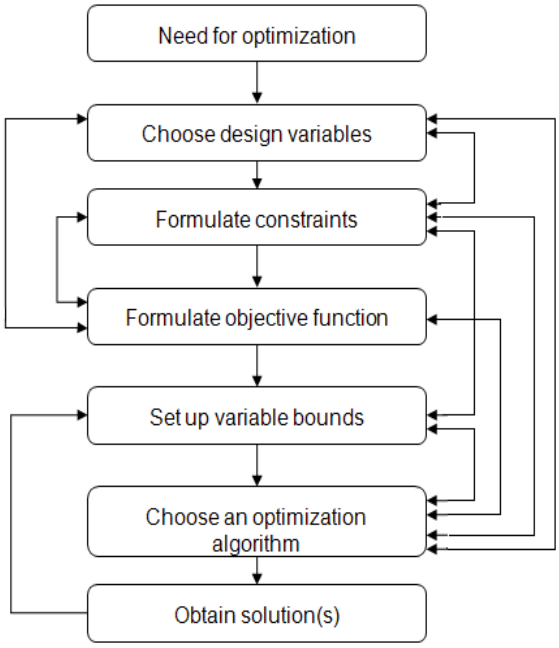

Fig. 2 Flow Chart For Optimum Design Procedure

The main reason we use formulation is to create a mathematical model of the optimal design problem, which then can be solved easily using an optimization algorithm. Figure 2 shows an outline of the steps usually involved in an optimal design formulation.

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5.1 System architecture

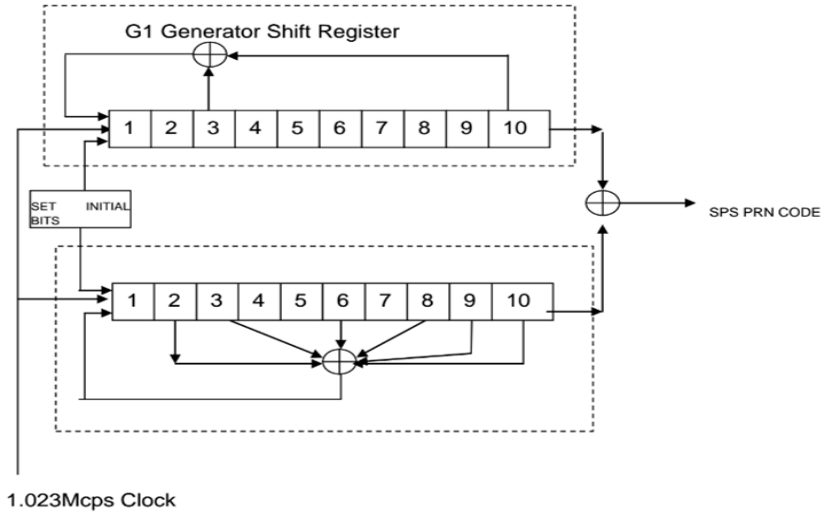

Fig.3 SPS code generator

IRNSS utilizes Gold codes for the SPS signal. The codes are selected based on the auto-correlation and cross-correlation properties. In figure 3 the codes are generated using Linear Feedback Shift Registers.[2]

For SPS code generation, the two polynomials G1 and G2 are as defined below:

$$G1: X10 + X3 + 1 \quad (5)$$

$$G2: X10 + X9 + X8 + X6 + X3 + X2 + 1 \quad (6)$$

Polynomial G1 and G2 are similar to the ones used by GPS C/A signal. The G1 and G2 generators are realized by using 10 bits Maximum Length Feedback Shift Registers (MLFSR). The initial state of G2 provides the chip delay. G1 and G2 are XOR'ed for the generation of the final 1023 chip long PRN sequence. The time period of the PRN sequence is 1 millisecond.

5.2 Principle of the Proposed Method

In this paper we propose a much faster and efficient Gold codes generator, which can be easily initialized to any desired code, with a minimum delay. This is different from the classical Linear Feedback Shift Register(LFSR) based Gold codes generator that requires, in addition to the shift process, a significant number of logic XOR gates. The presence of all these logic XOR gates in classical LFSR based Gold codes generator causes more consumption time in the generation and acquisition processes. In addition to its simplicity and its speed, in the proposed architecture, we use only two XOR gates, has fewer resources than the conventional Gold generator and can thus be produced at lower cost.

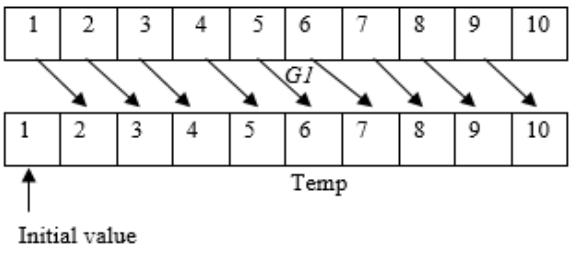

Fig 4. Proposed design optimization method

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In figure 4 we can see that the new optimized design uses only one XOR gate for initialization of values of all values are shifted parallel at the same tome and the output of the complete output is XOR'ed with G2 and we derive the final SPS PRN codes of IRNSS satellite.

VII. SIMULATION RESULTS

We have implemented the SPSs PRN code on SPARTAN 2 FPGA kit and simulated it on Model simulator for verification of the PRN codes with the ISRO setup.

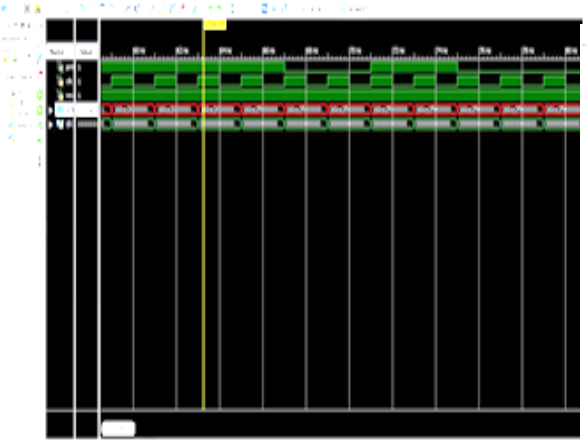

Fig.7b Xilinx simulation for Satellite 1 in S band

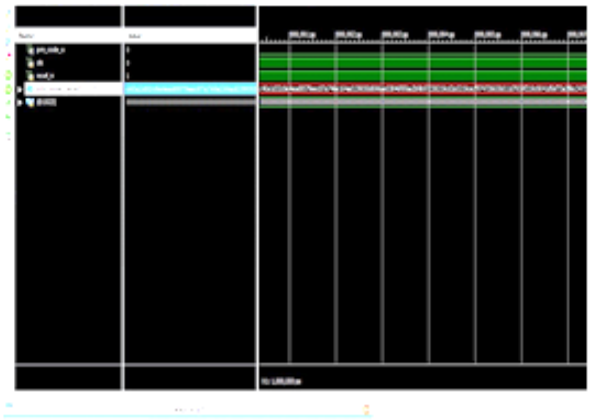

Fig.7a Xilinx simulation for Satellite 1 in L5 band

Fig. 7a demonstrates the generation of PRN code for Satellite-1 in L5 band. The output signal is used for validating the generated data bits carried out in Xilinx ISE 14.7 utilizing Verilog HDL. The output is obtained only when the respective count input is provided along with the reset input and clock input. Reset input is used as active high.Figure 7b shows the output signal for satellite 1 in S band using Xilinx 14.7 and is validated.

VII.CONCLUSION

Various techniques from the area of hardware synthesis can be used to optimize control flow in software. ZYNQ is the best hardware to implement the PRN code as it integrates the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration.

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REFERENCES

[1] Ganeshan A. S., Rathnakara S. C., Gupta R., Ja in A.K. (2005) ―Indian Regional Navigation Satellite System(IRNSS) Conceptǁ, ISRO Satellite Centre Journal of Spacecraft Technology, 15(2):19 23.
[2] Ganeshan A.S. (2012) ― Overview of GNSS and Indian Navigation Programǁ, GNSS User Meeting, 23 Feb.2012, ISRO Satellite Centre, Bangalore.
[3] Saikiran B, Vikram V (2013) IRNSS Architecture and Applications, KIET Institute of Comm. & Electronics.
[4] E. M. Sentovich, et al., "SIS: A System for Sequential Circuit Synthesis". Technical Report of the UC Berkeley Electronics Research Lab, May 1992.
[5] Rao Sasibhusan G., Global Navigation Satellite Systems with essentials of satellite communications, McGraw Hill, New Delhi, 2010.
[6] Logsdon, T., TheNavstar Global Positioning Syatem. New York, NY: Van Norstrand Reinhold, 1992.
[7] Dashora, N. and R. Pandey, GPS data post-processing methods for undifferenced receivers located near the crest of EIA, Proc. Int. Beacon Satellite Symp., Boston, USA, 2007.
[8]K.L.Duand, Wireless Communication Systems: From RF Subsystems to 4G Enabling Technologies, Cambridge University Press, Cambridge,UK,1stedition,2010.
[9] M. J. E. Golay, "Multi-slit spectrometry,"Journal of the Optical SocietyofAmerica,vol.39,no.6,pp.437–444,1949.
[10]R. Turyn, "Ambiguity function of complementary sequences," IEEE Transactions on In formation Theory, vol.9,no.1,pp.46– 47,1963.
[11] Y. Taki, H. Miyakawa, M. Hatori, and S. Namba, "Even shift orthogonal sequences,"IEEE Transactions on Information Theory, vol.15,no.2,pp.295–300,1969.

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[12] C.C.Tsengand, C.L.Liu,"Complementary sets of sequences, "IEEE Transactions on Information Theory,vol.18,pp.644–652, 1972.
[13]R.C.Dixon, Spread Spectrum Systems with Commercial Applications, John Wiley & Sons, New York, NY, USA, 3rd edition, 1976.
[14] L.T.Wangand,E.J.McCluskey,"Linear feed back shift register design using cyclic codes, "IEEE Transactions on Computers, vol. 37,no.10,pp.1302–1306,1988.