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High Speed Energy Efficient Clock-Less Approach for Designing Asynchronous Architectures

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ABSTRACT: NULL convention logic is an appealing approach in designing self-timed asynchronous architectures that avoids many problems in standard digital circuits. This technique integrates control and data transformation into a single logical function, yielding a self-timed delay insensitive circuit. This paper presents a novel NCL+ approach supporting Return-to-one protocol (RTO) for designing clock-less digital circuits i.e., delay insensitive asynchronous logic. Comparative analysis have been done among traditional digital CMOS, NCL and NCL+ paradigms to measure the performance and to verify the functionality of each gate using Tanner EDA with 250nm technology in terms of power, propagation delay, power delay product and noise. Simulation results suggest that the proposed NCL+ design consumes less power, offers high speed and more robust to noise.

KEYWORDS: VLSI; CMOS; NCL; NCL+; RTZ; RTO; Threshold Gates.

I. INTRODUCTION

Delay-insensitive self-timed asynchronous circuit design has been the main objective of renewed research for the advantages they provide over traditional synchronous circuit template. Some benefits of these circuits include reduced propagation delay, power consumption, easy design reuse, and less noise [1]. For designing delay insensitive asynchronous design paradigms NULL Convention Logic (NCL) have been proved to be a promising method among various asynchronous design templates. To maintain delay insensitivity NCL circuits employs threshold gates with hysteresis [1, 2]. Several CMOS implementation have been developed for designing NCL gates that includes dynamic, semi-static and static schemes [3-4].

NULL Convention Logic exploits Return-to-Zero (RTZ) handshake protocols, means that all the rails are assigned to zero when there is absence of data in the channel [5, 6]. In this paper, we present a novel approach NCL+ to hold Return-to-One (RTO) [13] protocol, where in the absence of valid data a spacer is provided by assigning all wires to one in the data channel [5-8]. We show that the NCL+ gates offers low power than the NCL and CMOS gates and we also show that the gates produce less noise compared to NCL and CMOS. This paper addresses as, section II describes the overview of NCL. Section III presents the NCL+ design methodology. In Section IV the NCL+ gates are compared with NCL and conventional CMOS gates in terms of average power, propagation delay, power-delay product and noise using Tanner EDA v.15.0 with 250nm technology and conclude in section V.

II. LITERATURE SURVEY

A. *NULL Convention Logic:*

Delay-Insensitivity, input completeness and hysteresis state holding behavior are the discrete advantages of NCL paradigms [1]. Delay insensitivity signifies that the circuit functions or works correctly despite of when the inputs are obtainable and can be achieved through dual/ quad rail logic [5, 6].

Dual wire logic consists of two rails, whose values are taken from the set {DATA0, DATA1, NULL} as in Table 1, where the DATA0 and DATA1 corresponds to Boolean logic levels 0 and 1, respectively. NULL corresponds to an

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empty set, i.e. no DATA is available. The two rails cannot be asserted simultaneously when they are mutually exclusive, called an illegal state [1, 7, 8].

Table 1: Dual-rail Signal

State	D0	D1
NULL	0	0
DATA0	1	0
DATA1	0	1
ILLEGAL	1	1

B. *NCL Threshold Gates:*

NCL threshold gates with hysteresis ability are constructed to realize the NCL architectures [1, 3]. A fundamental threshold NCL gate, THmn gate is shown in fig. 1, has n inputs and one output. Hysteresis property is imposed by the fact that, after the output is asserted; all the inputs must be de-asserted prior to the output becomes de-asserted [7, 9].

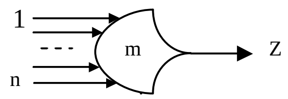

Fig. 1. Fundamental THmn threshold NCL gate

Another type of NCL threshold gate, shown in fig. 2, is the weighted threshold gate, THmnWw1w2…wR, where, m is threshold value and n is number of inputs respectively. The weighted gates have an integer value, $m \geq wR > 1$, given to input R. Here $1 \leq R < n$; where w1, w2 ... wR, are the weights of integer input 1, input 2 ... input R [1, 7].

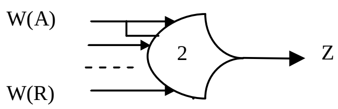

Fig. 2. Weighted THmnWw1w2…wR NCL gate

To design DI asynchronous architectures, NCL exploits 27 [18-20] fundamental threshold gates. Several CMOS paradigms have been implemented to design NCL architectures, which include dynamic, semi-static and static [3, 9, 10, 11, 12]. Among these the Static implementation of NCL gates, shown in fig. 3, are widely used because of its state holding capacity and are faster than the other two implementations [14-20].

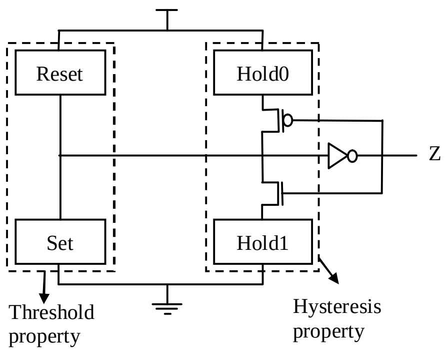

Fig. 3. Static implementation of NCL

III. PROPOSED NCL+ METHODOLOGY

A. *Return-to-One Protocol:*

The RTO [5, 13] protocol hand shaking protocol is similar to RTZ with the only difference is that, all the wires are inverted. Logical switching of data starts with all inputs 1's in the channel, shown in fig 4. When the valid data is

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passed, the receiver acknowledges data by lowering acknowledged signal and to end the logical transition all data wires must return to 1, denoting a spacer [6]. When the spacer is detected the ack signal is raised high, such that a new data transition can begin. These two handshaking protocols from Table 2 supports m-of-n DI codes [6, 8] and can interface with only n inverter stages [13].

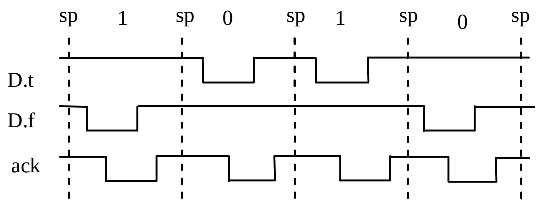

Fig. 4. RTO 1-of-2 data transmission

For m-of-n DI codes simplification, RTO (D.x) logical wire can be obtained from RTZ code:

$\{x \in N \mid 0 \leq x \leq m-1\}$,

$RTO(D.x) = \neg RTZ(D.x)$ eq .(1)

where RTZ (D.x) and RTO (D.x) refers to logical wire values in the RTZ and RTO protocols , respectively. [13].

Table 2: RTO Wire Encoding

Wire Name	Spacer	Bit '0'	Bit '1'
D.t	1	1	0
D.f	1	0	1

NCL+ is an adaptation of NCL that supports RTO protocol [5]. NCL+ gates can exploit a threshold function with a basic set of 14 NCL+ gates, shown in fig 5. The RTO protocol assigns the logical function of an NCL+ threshold gate to be the reverse of its NCL counterparts [11, 13].

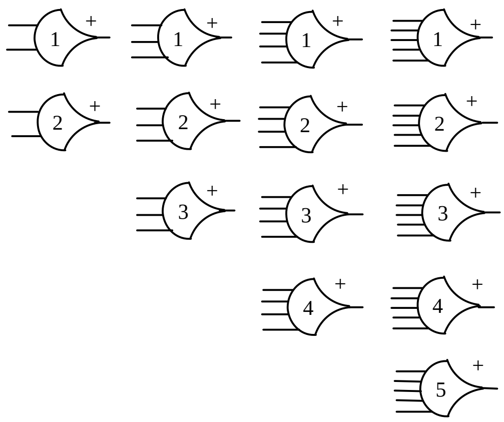

Fig. 5. Basic set of 14 NCL+ gates

The static CMOS implementation of NCL+ threshold gate is shown in fig. 6 that exploits set and reset networks to hold the state information. The basic fundamental difference is that only the wires are inverted/reversed, means that the NCL+ gates assign the switching function to be the inverse of NCL gates.

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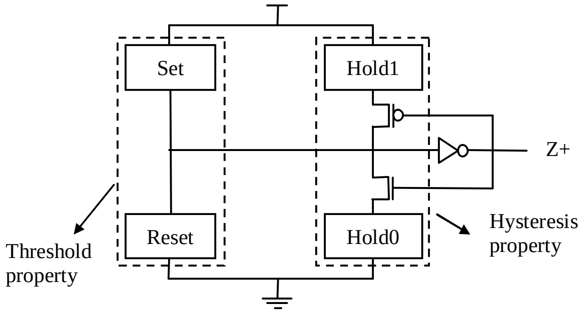

Fig. 6. Static implementation of NCL+

B. *NCL+ frame work:*

The output will be switched to logic 1, only when all the inputs are encoded to 1. When at least m of its inputs is at logic 0 the output switches to logic0 and keeps the previous value for other combinations of inputs. Both NCL and NCL+ necessitate same number of transistors and are typically equal in terms of cell- topology and area considerations [13].

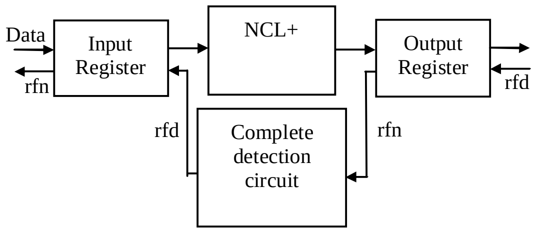

Fig. 7. NCL+ frame work

The NCL+ architecture, shown in fig. 7 consists of two DI registers where the inputs and outputs are configured in mutually exclusive assertion groups. To the input registers, inputs are organized from alternating NULL and DATA wave-fronts. The NCL+ circuit propagates a valid DATA until all the inputs have been received and propagated from the DATA wave-front. Therefore a DATA wave front cannot pass through the NCL+ circuit until all the inputs are DATA or the subsequent register has requested to pass the DATA. After the valid DATA is acknowledged, the output register sends a request for NULL wave front, rfn to the completion circuitry in order detect the completion of DATA wave front. Because of the hysteresis behavior, the gates will not pass NULL until all the inputs have been received and propagated from the NULL wave-front. So when a NULL wave front arrives at the input register, the NULL values will be passed through the output when all the inputs becomes NULL. After the NULL wave front is passed, the completion circuitry detects the NULL and sends a request for DATA; rfd signal to the previous register indicating that it has acknowledged and stored the NULL wave front and the previous register can pass a DATA wave front. Due to completion of NULL and DATA wave-fronts unwanted switching transitions are reduced there by reducing glitching effect.

IV. Comparative Analysis Between CMOS, NCL, And NCL+ Paradigms

A. *Power Consumption:*

Power management is a mounting issue in today's scenario. Due to switching activity of the active devices the dynamic power is consumed, which is given by the following equation.

$$P_{dynamic} = P_{transient} + P_{capacitance} = \frac{1}{2}\alpha C V_{DD}^2 f \qquad \text{eq. (2)}$$

Where Ptransient is the transient power due to change in logic states and the capacitive power Pcapacitance occurs due to charging and discharging of the circuit. Here α represents the switching coefficient, C is the load capacitance, V_{DD} is the reference voltage and f represents the clock frequency.

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Table 3: Simulation results for average power of CMOS, NCL, NCL+ threshold logic gates (μW)

GATES	CMOS	NCL	NCL+
TH12	4.97×10^{-5}	6.52×10^{-5}	7.17×10^{-5}
TH22	6.01×10^{-5}	7.60×10^{-5}	6.36×10^{-5}
TH13	2.00×10^{-5}	2.99×10^{-5}	2.96×10^{-5}
TH23	5.16×10^{-5}	3.18×10^{-5}	5.86×10^{-5}
TH33	2.93×10^{-5}	3.23×10^{-5}	2.80×10^{-5}
TH23W2	3.36×10^{-5}	3.11×10^{-5}	3.33×10^{-5}
TH33W2	3.08×10^{-5}	3.56×10^{-5}	2.98×10^{-5}
TH14	9.07×10^{-5}	1.42×10^{-5}	1.38×10^{-5}
TH24	3.64×10^{-5}	2.03×10^{-5}	1.69×10^{-5}
TH34	3.72×10^{-5}	1.70×10^{-5}	1.66×10^{-5}
TH44	1.50×10^{-5}	1.85×10^{-5}	1.39×10^{-5}
TH24W2	2.45×10^{-5}	1.73×10^{-5}	1.45×10^{-5}
TH34W2	3.03×10^{-5}	1.03×10^{-5}	1.69×10^{-5}
TH44W2	2.97×10^{-5}	1.11×10^{-5}	1.62×10^{-5}
TH34W3	1.68×10^{-5}	1.77×10^{-5}	1.52×10^{-5}
TH44W3	1.51×10^{-5}	1.81×10^{-5}	1.41×10^{-5}
TH24W22	1.70×10^{-5}	1.63×10^{-5}	1.39×10^{-5}
TH34W22	2.78×10^{-5}	2.10×10^{-5}	1.64×10^{-5}
TH44W22	2.64×10^{-5}	1.59×10^{-5}	1.53×10^{-5}
TH54W22	1.85×10^{-5}	2.05×10^{-5}	1.28×10^{-5}
TH34W32	1.71×10^{-5}	1.68×10^{-5}	1.29×10^{-5}
TH54W32	1.85×10^{-5}	1.88×10^{-5}	1.43×10^{-5}
TH44W322	2.26×10^{-5}	1.70×10^{-5}	1.51×10^{-5}
TH54W322	2.73×10^{-5}	1.92×10^{-5}	1.57×10^{-5}
THxor0	4.14×10^{-5}	1.58×10^{-5}	1.48×10^{-5}
THand0	2.83×10^{-5}	1.44×10^{-5}	1.45×10^{-5}
TH24comp	3.30×10^{-5}	1.74×10^{-5}	1.43×10^{-5}

From the simulation results as shown in table 3, our proposed NCL+ design consumes low power when compared to other conventional CMOS and NCL design models. Therefore the proposed method has an advantage in terms of power consumption.

B. *Noise Susceptibility:*

In the aspect of noise, our proposed NCL+ design generates less noise when compared to static CMOS and NCL design models. Therefore from the evaluation results shown in table 4, the proposed method has an added advantage in terms noise when compared to CMOS and NCL design styles.

Table 4: Simulation results for noise of CMOS, NCL, NCL+ logic gates

GATES	CMOS	NCL	NCL+
TH12	1.70K	73.26	9.70
TH22	1.27X	73.11	73.11
TH13	1.13K	165.43	80.25
TH23	823.49K	165.28	28.46
TH33	3.50X	165.30	165.28

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TH23W2	393.83K	165.51	11.04
TH33W2	196.99K	165.31	31.49
TH14	852.23	524.58	147.20
TH24	31.81K	263.10	37.15
TH34	959.17K	263.01	56.20
TH44	8.10530X	263.05	263.01
TH24W2	51.53K	262.58	27.96
TH34W2	115.81K	263.10	15.17
TH44W2	440.36K	263.08	48.25
TH34W3	715.20K	262.47	8.71
TH44W3	177.12K	263.10	20.51
TH24W22	232.86K	261.62	49.82
TH34W22	46.68K	263.10	12.04
TH44W22	1.23X	263.01	25.08
TH54W22	4.12X	263.04	119.44
TH34W32	78.76K	262.23	14.22
TH54W32	883.64K	263.07	44.08
TH44W322	106.57K	263.10	19.16
TH54W322	970.22K	263.08	61.38
THxor0	597.12K	263.03	32.37
THand0	507.28K	262.97	27.47
TH24comp	597.12K	263.03	32.37

C. *Propagation Delay:*

To increase the system performance of a digital circuit the propagation delay should be low, which is given by

$$t_{delay} = \frac{C_L V_{DD}}{I} \propto \frac{V_{DD}}{(V_{DD} - V_t)^2} \quad \text{eq. (3)}$$

The traditional NCL design consumes more delay than the conventional static CMOS design. In order to reduce the propagation delay of the static NCL gates and improve the performance of the circuit, NCL+ design methodology is used that provides less propagation delay to transmit the valid data and to generates a spacer in the data channel. The simulation values for the three design styles are tabulated in table 5. Based on these simulation results, our proposed NCL+ design show the lowest propagation delay than NCL but the downside is that it produces more delay than the conventional CMOS design.

Table 5: Simulation results of propagation delay for CMOS, NCL, NCL+ gates (s)

GATES	CMOS	NCL	NCL+
TH12	20.60n	20.79n	19.95n
TH22	19.50n	20.71n	20.70n
TH13	46.62n	40.81n	40.31n
TH23	623.93p	40.81n	10.42n
TH33	40.15n	40.45n	40.67n
TH23W2	40.44n	40.78n	40.35n
TH33W2	39.95n	40.83n	4057n
TH14	80.80n	80.90n	80.26n
TH24	776.44p	80.93n	80.41n
TH34	380.41p	80.91n	80.63n
TH44	80.13n	80.87n	80.87n

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TH24W2	786.59p	80.93n	80.37n
TH34W2	40.37n	80.91n	80.54n
TH44W2	40.53n	80.90n	80.65n
TH34W3	80.61n	80.92n	80.40n
TH44W3	80.41n	80.88n	80.63n
TH24W22	80.68n	80.93n	80.34n
TH34W22	754.54p	80.92n	80.40n
TH44W22	419.87p	80.91n	80.59n
TH54W22	80.22n	80.86n	80.45n
TH34W32	80.64n	80.92n	80.42n
TH54W32	79.95n	80.90n	80.65n
TH44W322	767.11p	80.92n	80.41n
TH54W322	437.29p	80.91n	80.56n
THxor0	245.37p	80.91n	80.56n
THand0	541.27p	80.92n	80.41n
TH24comp	454.20p	80.91n	80.56n

D. *Power-Delay Product (PDP):*

The Power-Delay Product is the product of the total dynamic power and propagation delay, which is given by

$PDP = P_{dynamic} \times T_{delay}$ eq. (4)

The proposed NCL+ design has finest PDP than the conventional NCL design. The power-delay product for CMOS, NCL and NCL+ gates is tabulated in table 6.

Table 6: Simulation results of power-delay product for CMOS, NCL, NCL+ threshold logic gates (W-s)

GATES	CMOS	NCL	NCL+
TH12	1.02×10^{-12}	1.35×10^{-12}	1.43×10^{-12}
TH22	1.19×10^{-12}	1.57×10^{-12}	1.31×10^{-12}
TH13	9.32×10^{-13}	1.22×10^{-12}	1.19×10^{-12}
TH23	3.23×10^{-14}	1.29×10^{-12}	6.10×10^{-13}
TH33	1.17×10^{-12}	1.30×10^{-12}	1.13×10^{-12}
TH23W2	1.35×10^{-12}	1.26×10^{-12}	1.34×10^{-12}
TH33W2	1.23×10^{-12}	1.31×10^{-12}	1.20×10^{-12}
TH14	7.32×10^{-13}	1.14×10^{-12}	1.10×10^{-12}
TH24	2.60×10^{-14}	1.64×10^{-12}	1.35×10^{-12}
TH34	1.41×10^{-14}	1.37×10^{-12}	1.33×10^{-12}
TH44	1.20×10^{-12}	1.49×10^{-12}	1.12×10^{-12}
TH24W2	1.92×10^{-14}	1.40×10^{-12}	1.16×10^{-12}
TH34W2	1.22×10^{-12}	8.33×10^{-12}	1.36×10^{-12}
TH44W2	1.20×10^{-12}	8.97×10^{-12}	1.30×10^{-12}
TH34W3	1.35×10^{-12}	1.43×10^{-12}	1.22×10^{-12}
TH44W3	1.21×10^{-12}	1.46×10^{-12}	1.13×10^{-12}
TH24W22	1.37×10^{-12}	1.31×10^{-12}	1.11×10^{-12}
TH34W22	2.09×10^{-14}	1.69×10^{-12}	1.31×10^{-12}
TH44W22	1.10×10^{-14}	1.23×10^{-12}	1.23×10^{-12}
TH54W22	1.48×10^{-12}	1.65×10^{-12}	1.02×10^{-12}
TH34W32	1.37×10^{-12}	1.35×10^{-12}	1.15×10^{-12}
TH54W32	1.47×10^{-12}	1.52×10^{-12}	1.15×10^{-12}

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TH44W322	1.73×10^{-14}	1.37×10^{-12}	1.21×10^{-12}
TH54W322	1.19×10^{-16}	1.55×10^{-12}	1.26×10^{-12}
THxor0	1.01×10^{-15}	1.26×10^{-12}	1.19×10^{-12}
THand0	1.53×10^{-14}	1.16×10^{-12}	1.16×10^{-12}
TH24comp	1.49×10^{-14}	1.40×10^{-12}	1.15×10^{-12}

V. Conclusion and Future Work

In this work, we have designed and implemented delay-insensitive asynchronous static NCL+ library. All the static NCL+ gates were configured, successfully simulated and verified to be functionally correct. Furthermore power, propagation delay, power-delay product and noise of each gate is simulated and calculated. From the simulation results it is observed that power consumed and by each gate is less when compared with static NCL and CMOS topologies and the proposed design is more robust to noise, which is an added advantage. NCL+ provides less delay and power-delay product compared to NCL but the drawback is that it provides more delay when compared to static CMOS design. Future work includes optimizing the propagation delay for higher performance and better speed of operation.

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