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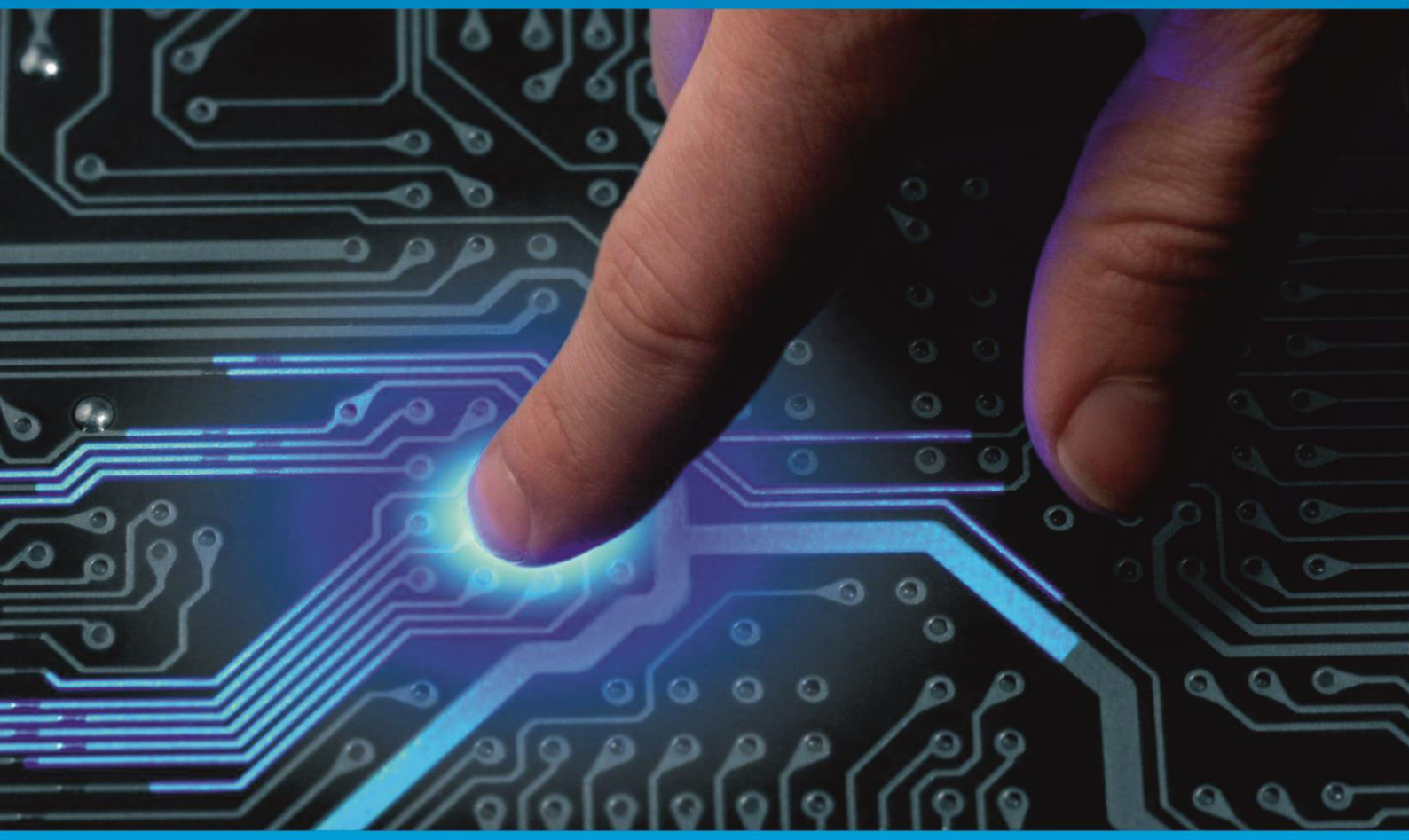

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Lector Technique Based Performance Analysis of Current Mirrored Footed Domino Comparator

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ABSTRACT: A paper presents, how to reduce the power consumption and evaluation delay in diode footed domino comparator using lector based current mirrored footed domino comparator. In many applications, domino logic is widely used with less area and high performance overhead. As technology is scaled down, the supply voltage is reduced for low power and the threshold voltage is also scaled down to achieve high performance. Here, the reduction of problem leakage in CMOS circuit is done by lector technique. That take in p-type and n-type LCTs (Leakage Controlled Transistors) are placed between ground from supply. Lector is a one of technique in domino logic, which are self-controlled and offers the extra resistance, which will reduce the problem of leakage current in the CMOS circuits. A method using lector based current mirrored footed domino comparator is proposed to reduce the power dissipation and evaluation delay. To improve the speed and noise immunity of circuit performances. The proposed leakage resistant domino uses a current mirror and PMOS as well as NMOS transistors to conquer the leakage produced by the circuit. Current mirror is a cost-efficient resistor that refuses leakage and can be shared among all gates.

KEYWORDS: Current mirrored footed domino, Diode footed domino, Keeper transistor, Lector, Domino logic, CMOS, Comparator, Power consumption, Evaluation delay, Power delay product and Leakage controlled transistors.

I. INTRODUCTION

Power consumption is a critical factor while designing of VLSI circuits, due to the technology scaling the supply voltage and threshold voltage has been scaled down in order to upgrade the performance of circuit this leads to introducing more leakage current in the CMOS logic circuit. For effective leakage tolerant such as lector technique have been introduced in both diodes Footed domino and diode footless domino logic [1, 2] where lector has a two type of transistor one is p type leakage controlled transistor and other hand is n type leakage controlled transistor. However size of the keeper transistor is very small due to high propagation delay and charge sharing problem were arise is the major concern of designing CMOS circuit. For effective noise tolerant current mirrored footed domino logic has low power consumption and good unity noise gain as compared with conventional logic[3] where keeper transistor is used to compensate the leaky current and also reducing the contention current arise from VDD to GND but increasing sub threshold leakage current as the technology scaled down. Length of the Gate and thickness of the gate oxide are responsible for leakage power and it differs exponentially along threshold voltage. In high-performance designs technology generations especially for wide fan-in dynamic gates [4] employed in register, flip-flop, processing unit, memories and all. Then the proposed High speed domino, reduce the leakage current and the parasitic capacitance occurs at the dynamic node. Parasitic capacitance means unwanted delay occurs during circuit in ON condition then the delay has been removed with help of current comparison based domino but it has less noise immunity. In diode footed domino logic [5] gate and drain terminal of NMOS transistor are connected together and make a diode configuration. Hence leakages reduced by stacking effect of transistor. Performance have been analyzed with various domino [6] proposed domino having a better leakage tolerance and increased noise immunity.

This is employed with two keeper transistor in order to improve the noise immunity and reducing delay without increment chip area. Then major drawback of proposed method Extra NMOS transistor was added to compensate the keeper leakage current. For high – speed and low power integrated chip Performance domino logic [7] based circuits are extensively used and can be broadly classified as footed and footer less domino logic [8]. The footer transistor used to isolates the pull down network (PDN) from ground avoiding the change of state of dynamic node by PDN during the

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pre-charge making it better with respect to timing characteristics. On the other hand, if the footer transistor is absent from circuit, the footless domino reduces the power dissipation along with the circuit evaluation delay. Due to distinct characteristics, the footed as well as footless domino logic based circuits both are extensively employed in case of leakage tolerant. In high speed processor design the current mirrored based footed domino [9] widely used to enhance the speed of the device and it has better noise immunity. In the conventional domino [10] more evaluation delay has been introduced during the evaluation phase, and then the delay has been reduced by placing the mirrored transistor parallel with the evaluation network. For high performance application leakage resistant domino logic [11, 12] is widely used to improving noise immunity without degradation of circuit performance but consuming large chip area.

II. LITERATURE REVIEW

Now we good graces sometime years, major part re the cardinal boundary deep-laid is done using impetuous reasonability resulting among other things well-rounded probing work in this field. Discussion with respect to accomplished refer to the domino techniques are give details inside of this section.

Domino circuits are broadly used in high-speed uses for the putting into practice of high fan-in circuits. However, domino circuits are vulnerable to noise. The noise consideration of domino circuits is due to their short switching threshold voltage, which is the similar to threshold voltage of NMOS devices in the evaluation process. The substantial rise in deep-submicron noise through technology scaling severely effects the worth of domino circuits. By technology scaling, the supply voltage is topped down to drop the power consumption. In order to increase performance, the transistor threshold voltage has to be commensurately surmounted to keep a high drive current. On the other hand, the Vth (threshold voltage) mounting results in the considerable and increase of the sub-threshold leakage current.

I .Diode Footed Domino Logic

Figure I shows that diode footed domino logic scheme. In this domino consisting of diode configuration here the diode footer is placed series with the evaluation network. Then there are two phase of performance. One is precharge phase and another one is evaluation phase .Hence the sub threshold leakage current has been minimized with the use of stacking effect. Then diode footer based on gate and source terminals are connect together to form a diode configuration. Then the diode footer promotes the gate switching threshold voltage from Vth to 2Vth.which leads to enhance the remediate the noise immunity.

Then there are two phase of operation performed such as,

1. Precharge phase
2. Evaluation phase

Precharge Phase

When the applied input of clock pulse is LOW, here by precharge transistor goes to active state, and then remaining part of the evaluation transistor goes to inactive state. During the precharge phase the dynamic node get pre charged through the VDD.

Evaluation phase

When applied input of clock pulse is HIGH, cause evaluation transistor goes to active state, and then remaining part of the precharge transistor will be in off state. During the evaluation phase the dynamic node is discharged through the GND.

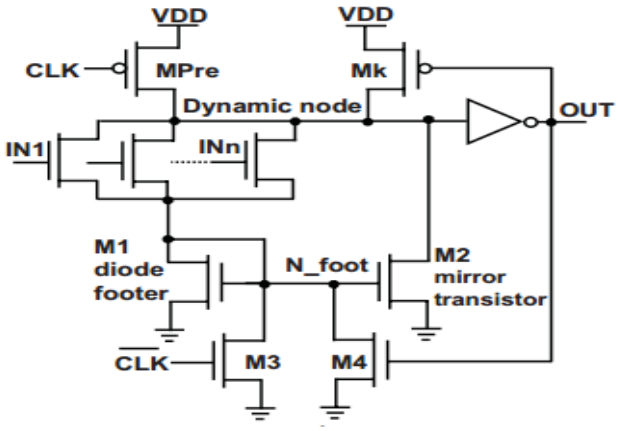

Figure I: Diode Footed Domino Logic

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II. Diode Footed Domino logic Comparator

The circuit design of diode footed comparator illustrated in Figure II. It consists of keeper transistor, mirror transistor, precharge transistor and the evaluation transistor then footer transistor. In normally a comparator circuit that compares two binary words and indicates whether they are equal or not. In recharges phase, active clock input is asserted to low, and all the input goes to low. Therefore the dynamic node is pre charged through VDD and the output of the comparator is low. In the Evaluation phase, active clock input is asserted to high then the dynamic node is discharged to conduct the leakage path between the dynamic node and GND. In case all the applied input bits are equal (when matches are found) there is no discharge path exists between dynamic node and GND. In case of applied input bits are not equal (when mismatches are found) hence the leakage path is exists between the dynamic node and GND cause the output of the comparator is go high. Finally the keeper transistor is used to compensate the leakage current then the size of the keeper is very small due to that will dissipates the large amount of leakages while matching or mismatching of input occurs. That is major concern of the diode footed domino comparator.

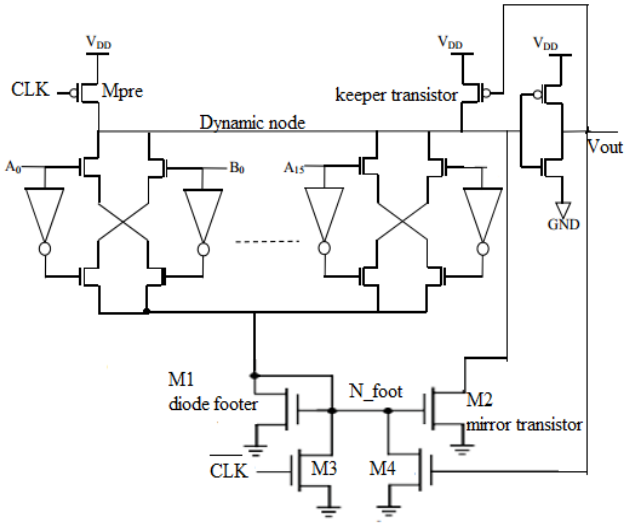

Figure II: Diode Footed Domino Logic Comparator

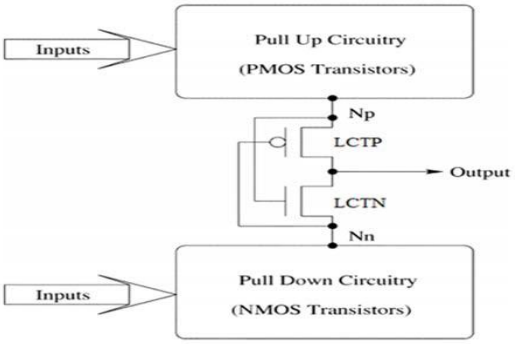

Figure III: Constructive Analysis of Lector Technique

III. TECHNIQUE USED

LECTOR is a technique that describes the leakage reduction without affecting dynamic power dissipation for designing comparator circuit. LECTOR expands as **Le**akage **C**ontrolled **T**ransistor. Figure III shows that Constructive Analysis of Lector Technique, it consisting of N-type leakage controlled transistor and P-type leakage controlled transistor. Where gate terminal of the both (N-type and P -type transistor) controlled by source of other .then it has two pull up (PMOS) network and two pull down (NMOS) network are connected serially. When applying input to the transistor either high or low but one of the leakage controlled transistor should be in near cutoff region for any combination input.

In this method, dual leakage control transistors are LCTP (PMOS) and LCTN (NMOS). That introduced in the middle of the pull-up and pull-down network. These two gate transistors are controlled by the source terminal of each other here, transistor LCTP and LCTN's switching depends on the potential difference at node NP and NN, respectively.

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Hence, for any combination of applied input one of the lector transistors will operate near cut-off region, increasing the resistance between supply and ground rails leading to shrinking of the leakage current.

Non idle mode

During non-ideal mode (pre-charge mode), when the clock is low the dynamic node is debited to VDD through transistors, MPre and LCTP. The pre-charging of dynamic node is virtually autonomous of the input states.

If all the inputs act low ahead the clock is set to low then the node NN will hold at low voltage along with transistor LCTP bid the less resistance rail for charging dynamic nodule. If all the inputs applied act high, then the potential difference at node NN is insufficient for turning OFF LCTP completely i.e., LCTP is conducting adjacent its cut- off region. Therefore, resistance due to LCTP will act much lower than the completely OFF state resistance leading to high charging of the dynamic node. In this case, the leakage current be determined by, going on the applied inputs while; the comparator output is liberated of these feedbacks (i/p's).

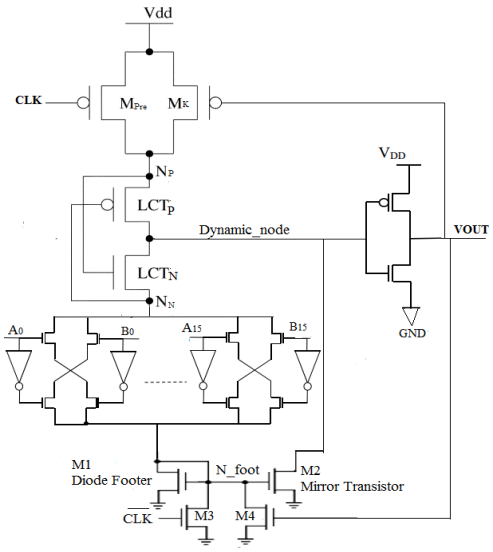

Figure IV: Lector based diode footed domino logic comparator

Idle mode

During ideal mode (evaluation mode), just as the clock is high, dynamic node gets discharged or charged depending upon the applied input vectors. If valid inputs are applied pull-down network transistors leakage current establishes some potential across diode footer, M1, which forms the OFF evaluation transistors gate-source-voltage negative. This results in exponential contraction in sub leakage current. Therefore, if sequences of inputs are equal and matching, the dynamic node will no longer be discharged by the pull-down network and the output concerning the comparator is low and it directs keeper transistor, MK, ON.

The potential at node NP will direct the transistor LCTN, ON, but potential at node NN will no longer allow the transistor LCTP to completely cut-off making it conduct adjacent cut-off-region leading to high resistance path amidst supply and ground shrinking the sub-threshold and gate leakage current. Here, if all the inputs are low, the LCTP will operate near cut-off-region and if all the applied inputs are high, the LCTN will conduct near cut-off-region. Hence, by employing LCTs, the resistance along the supply and GND is enlarged which in turn reduces leakage current and concurrently increases the domino comparator circuits propagation delay. Controlling the propagation delay of the circuit is done by LCTN and LCTP are the proper sizing of the lector transistors.

IV. PROPOSED METHOD

The proposed design of the current mirrored footed domino logic is illustrated in Figure IV. A current mirror is a circuit considered to replica a current over one active device by monitoring the current in alternative active device of a circuit, charge the output current constant regardless of loading .The main objective of a current mirror circuit is to reducing the evaluation delay introduced from the evaluation network when clock input is high. Then the proposed current mirror circuit is added in parallel to the evaluation network of the current mirrored footed. Where m1 is the precharge transistor it gets the input from clock. M2 is the keeper transistor which is used to compensate the sub threshold leakage current while charging and discharging of dynamic node. Then the transistor m3 and m4 make a stacking effect to the circuit in order to reducing the problem of leakage current in evaluation phase.

Then keeper ratio explained as,

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$$k = \frac{\mu_p (W|L) keeper - transistor}{\mu_n (W|L) evaluation - transistor}$$

Where,

W, L are length and width of the transistors.

μ_p, μ_n are the motilities holes and electrons.

When the size of the stack gets increased then the size of the evaluation network also increased. Gate of the keeper is controlled by m5 transistor. This is used to regulate the leakages in CMOS circuit.

PROPOSED CURRENT MIRRORED FOOTED DOMINO COMPARATOR

The proposed design of current mirrored footed domino comparator shown in Figure V. Then the proposed comparator used to founds the matches and mismatches of the binary input. Basically in domino logic two phase of operation were performed. When applying clock input is goes to low, the precharge transistor M1 (PMOS) goes to active state and the evaluation transistor (NMOS) will be on stable state.

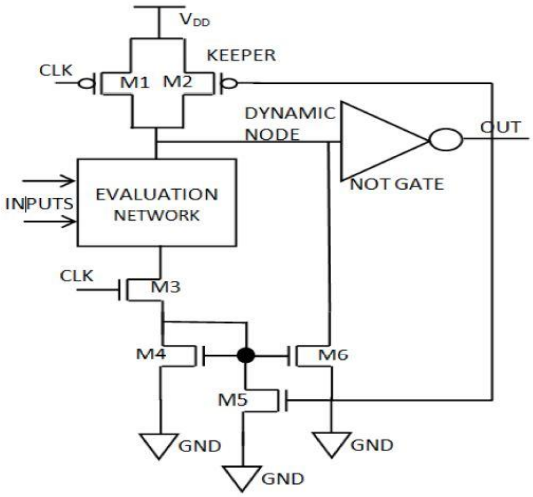

Figure V: Current Mirrored Footed Domino

During this mode dynamic node will be pre charged through the VDD. Results that output of the comparator pull down to low. Where keeper transistor used to compensate the charge loss, contention current arising from VDD to GND .When the applying input is goes to high, then the evaluation transistor (NMOS) goes to active state and the precharge transistor M1 (PMOS) goes stable state. During this mode dynamic node will be charged or Discharged based on the applying input. If the applying binary inputs are equal therefore no discharge will be occurs from pre charge node to ground. Hence the outputs of the comparator still at low .In case of applying inputs are not equal, and then the discharge path will occur from pre charge node to GND. Due to that output of the comparator goes to high. Schematic view of current mirrored footed domino comparator is shown in Figure VI.

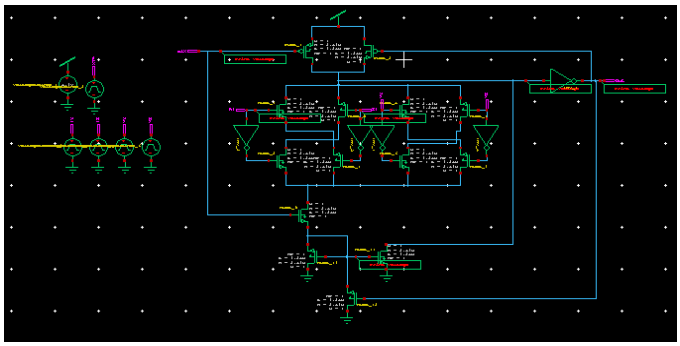

Figure VI: Current Mirrored Footed Domino comparator

LECTOR BASED CURRENT MIRRORED FOOTED DOMINO COMPARATOR

The design of schematic view of the lector based diode footed domino logic comparator shown in Figure VII. In this paper lector based diode footed domino comparator is one of the efficient reductions of leakages Where LECTOR is a leakage controlled transistor it consists of two type of leakage controlled transistor. One is p type leakage

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controlled transistor (LCTP) and other hand is n type leakage controlled transistor. In this method a leakage controlled transistor is placed between the pull up network and pull down network. Hence these method based on the stacking of transistor (i.e.) sub threshold leakage current that is flowing through a stack of series connected transistor decrease when more than one transistor in the stack is turned off. This effect is known as stacking effect (or) self-bias effect. Switching speed of the LCTP and LCTN Transistors are based on the potential difference occurring at point on NP and NN. Where NP and NN denotes the dynamic nodes of n type and p type transistor. One of the transistor will be operates on cutoff region and should not both on active region then only it will offers excess resistance to resist the flow of leakage current.

There are two phase of operation are performed, such as

1. Precharge phase
2. Evaluation phase

Precharge phase

When applied input of the clock pulse is LOW, precharge transistor will turn ON, then remaining part of the evaluation transistor remains OFF. During these precharge phases the dynamic node is reduced to VDD through the precharge transistor $M_{pre,}$ (PMOS Leakage Controlled Transistor) LCTP. In case of applied logic input is low for any combination of input is low then dynamic node of NN holds the low charges where as the operation of the LCTP is controlled by NN. Hence LCTP will operate on cut off region. In case of applied logic input is low for any combination of input is high then dynamic node of NN holds the charges as high. Hence LCTN will operate on cut off region. In that such case only leakage current responsible to the applied level of logic inputs but comparator output is irresponsible of these inputs.

Evaluation phase

When applied input of the clock pulse is HIGH, caused by evaluation transistor will be turn ON, then remaining part of the precharge transistor remains turn OFF. During the evaluation phase the dynamic node gets discharged or charged based on the level of applying input binary words through the evaluation transistor M_{eva}, (NMOS leakage controlled transistor) LCTN. If applied binary input to A and B are equal there is no any leaky path for precharge node .suppose if A and B inputs are not equal even in any single bit position changed it will make leaky path from precharge node to GND.

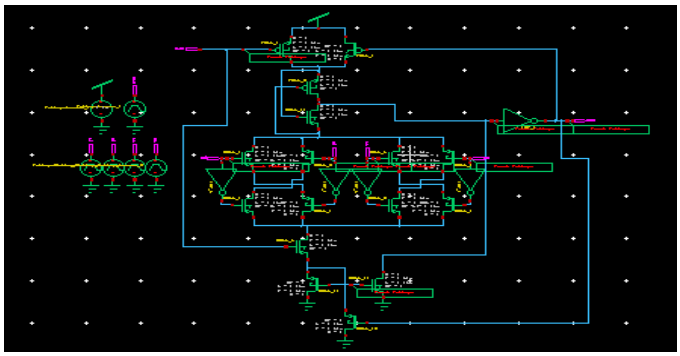

Figure VII: Lector Based Current Mirrored Footed Domino Comparator

Due to that dynamic node is discharged to low then static inverter placed at the output of comparator so the output go to high. Where the footer transistor m1 is connected in serious with evaluation network in order to reduce the leakages occur in CMOS circuit. Gate terminal of the transistor m4 is used to control the operation the keeper transistor. This keeper used to compensate the problem of charge sharing and contention current arises during the evaluation phase. The Potential difference occurs at node NP will control the operation of LCTN and potential difference occurs at node NN will control the operation of LCTP.

ADVANTAGE

The proposed paper has low power consumption and simple design circuit when it's compared with the conventional comparator. The evaluation delay has been reduced with current mirrored footed domino. Lector is a self-controlled device

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V. SIMULATION RESULTS

Tanner EDA tool is a SPICE computer analysis programmed for analogue integrated circuits. With these engine tools, spice program provides ability to proposal and simulate new ideas in analog IC (Integrated Circuits) before going to the time overwhelming and costly process of chip fabrication. Simulation setup of S-Edit window is shown in Figure VIII. Description of S-Edit is given below,

- Start S-Edit
- Start a New Design
- Create a new Cell
- Enter the symbol libraries:
- Setup the SPICE Models for the Generic_025 kit.

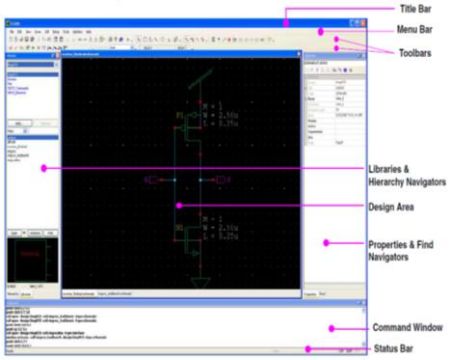

Figure VIII: Simulation setup of S-Edit window

S-Edit is a schematic entry tool that is conditioned manuscript circuits that can be ambitious frontward into a layout of an integrated circuit (IC). It as well be responsible for the capability to achieve SPICE virtual reality of the circuits via a simulation engine that is called T-SPICE. T-SPICE can be outfit and entreated from within S-edit. SPICE models for the Generic_025 kit of figure is shown in Figure IX.

Tanner T-Spice virtual reality delivers fast and accurate simulation for analog and mixed-signal system (AMS) integrated circuit designs. T-Spice not only act out circuits rapidly with a high degree of accuracy, nevertheless as well is well-suited with industry most important standards and mixes easily with the Tanner S-Edit schematic capture tool and Tanner W-Edit.

T-Spice consist of better accuracy with forward-looking modelling, multi-threading livelihood, device state scheming, real-time waveform broadcasting and exploration, and a thorough knowledge wizard for simple SPICE syntax conception.

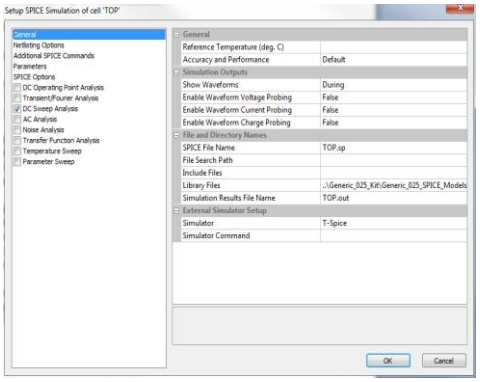

Figure IX: SPICE models for the Generic_025 kit

T-Spice implements fast and perfect simulation of analog and mixed analog/digital circuits. The simulator contains the most recent and best device models offered, as well as combined line models and livelihood for user defined device models via tables or C functions. Net-list View of T-SPICE window is shown in Figure X.

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T-Spice procedures an extended description of the SPICE input language that is companionable with all industry standard SPICE simulation programs. Totally SPICE's device models are integrated, as well as resistors(R), capacitors(C), inductors(L), mutual inductors, single and coupled transmission lines, current sources(I), voltage sources(V), controlled sources, and a full complement of the latest advanced semiconductor device simulations from Berkeley and Philips Labs. Figure XI shows the programmers editor window.

In W-Edit charts can automatically configure for the type of data being presented. Chart views can be panned back and forth and zoomed in and out, specifying the exact X-Y coordinate ranges. W-Edit shows T-Spice simulation yield waveforms as they are presence of created during simulation. Figure XII shows the Simulated waveform of current mirrored footed domino comparator.

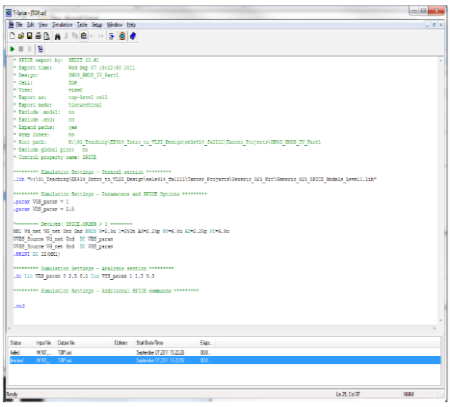

Figure X: Net-list view of T-SPICE

Imagining the intricate numerical data resultant from VLSI circuit simulation is dangerous to test, understand, and improve those circuits. W-Edit is a waveform observer that offers simplicity of use, power, and speed in a supple environment intended for graphical data exhibition.
It provides the facility of,

- Design simulation
- Device statement
- Simulation commands
- User designed external models
- Small signal and noise models

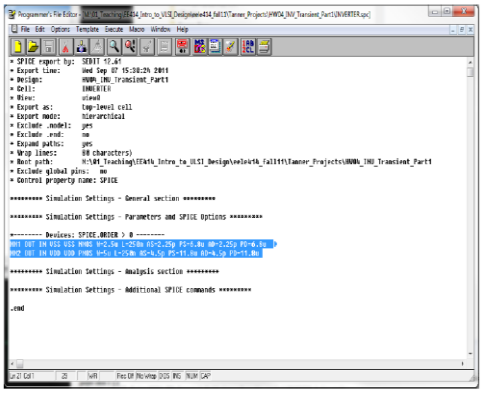

Figure XI: Programmer's editer window

The benefits of W-Edit includes:

- Constricted integration with T-Spice, Tanner EDA's circuit-level simulator. W-Edit can graphic representation data created by T-Spice straight, without alteration of the output data files. W-Edit graphic representation data enthusiastically as it is created during the simulation.

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- Graphic representation are robotically constructed for the type of data actuality offered.
- An information set is preserved by W-Edit as a unit called a trace. Several traces commencing different output files can be observed instantaneously, in solitary or manifold windows. You can copy and move traces among graphic representation and frames. You can achieve trace arithmetic or spectral analysis on in effect traces to generate new ones.
- You can sauce pan back and forth and zoom in and out of chart views, as well as requiring the particular *x-y* coordinate range W-Edit displays. You can portion positions and distances flanked by points simply and exactly with the mouse.

You can make especially material goods of axes, traces, grids, charts, text, and colours.W-Edit is a waveform observer that provides ease of use, power speed in a stretchy environment intended for graphical chart.
L-edit is an IC physical design tool from Tanner EDA. This apparatus tolerates you to draw the layout of an integrated circuit, look at cross-sections, perform design rule check (DRC), and create a Net list of your layout so that you can achieve layout versus schematic (LVS) using a altered tool.

Description of L-Edit is given below,

- Log onto a computer and launch L-edit
- Create a new layout design
- Verify the technology rule options & setup grid Save design

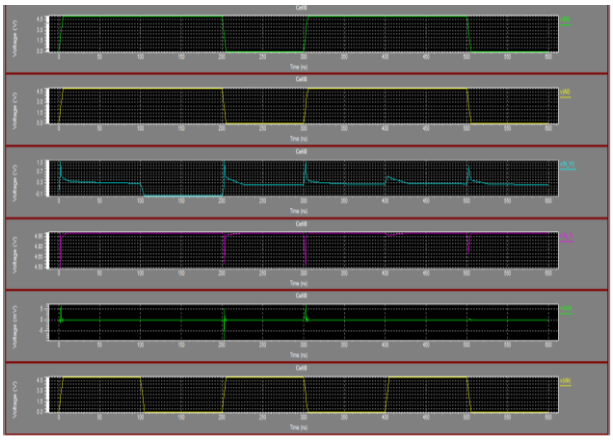

Figure XII: Simulated waveform of current mirrored footed domino comparator

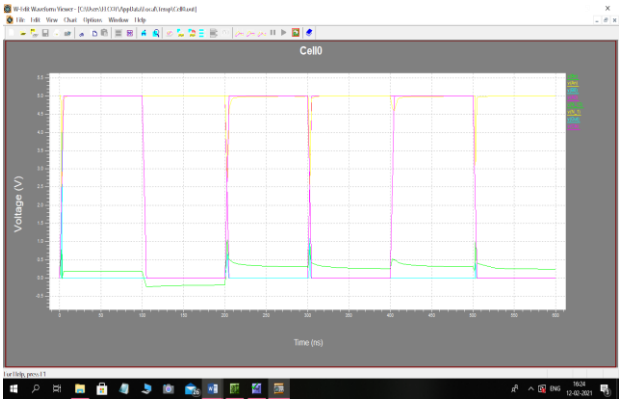

Figure XIII: Simulated waveform of lector based current mirrored footed domino comparator

Figure XIII shows the Simulated waveform of lector based current mirrored footed domino comparator. We continuously want to certify that the layout we have formed is what we proposed in the schematic. LVS will compare the Net list exported from S-edit and the Net list exported from L-edit. Here, not using L-Edit for implementing process. Only use S-Edit, T-Edit and W-Edit. W-Edit is vigorously connected to T-Spice and S-Edit by a run-time apprise feature that shows simulation results for instance they are animation created and permits waveform cross-probing unswervingly in the schematic managing editor for earlier design cycles.

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VI. CONCLUSION

In this paper, the current mirrored footed domino comparator and the lector based current mirrored footed domino comparator were designed and simulated. Then the performances have been analyzed with respect to power, delay and power delay product. In this paper current mirror footed domino has less power consumption i.e. 10 to 20 % then the conventional comparator such as diode footed domino. Then the Evaluation delay has been reduced by connecting the current mirrored domino parallel with the evaluation network .power delay product also be efficient when it's compared with the conventional domino. The power, delay and power delay product of the various domino logic has been analyzed and this is listed out in the Table I.

Table I: Comparison table of power, delay and PDP results with different domino methods

Parameter Analysis	Existing comparator		Proposed comparator	
	Diode footed domino comparator	Lector based Diode footed domino comparator	Current mirrored footed domino comparator	Lector based Current mirrored footed domino comparator
Power	26.23µw	10.06µw	22.7µw	9.755µw
Delay	30.58ps	52.56ps	30.12ps	51.23ps
PDP	0.80fs	0.59fs	0.689fs	0.528fs

Figure XIV, Figure XV, and Figure XVI shows that power, delay and PDP analysis of different domino logic respectively.

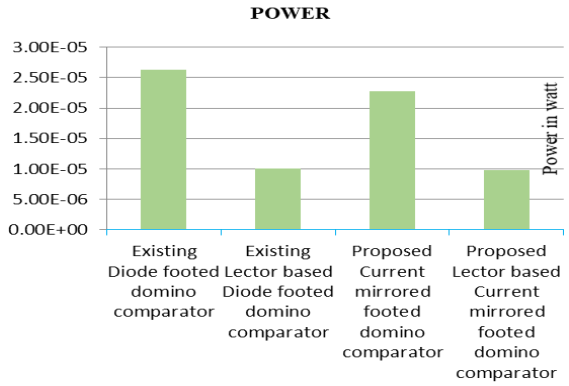

Figure XIV: Power analysis of different domino logic.

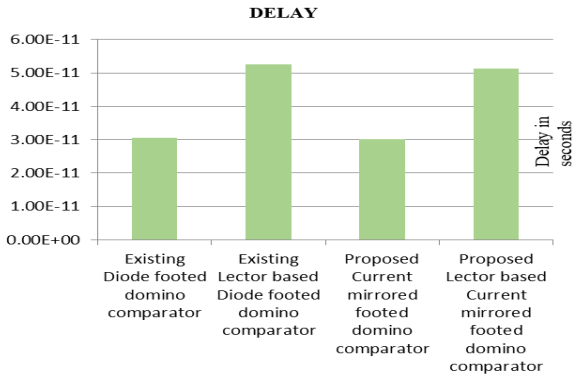

Figure XV: Delay analysis of different domino logic

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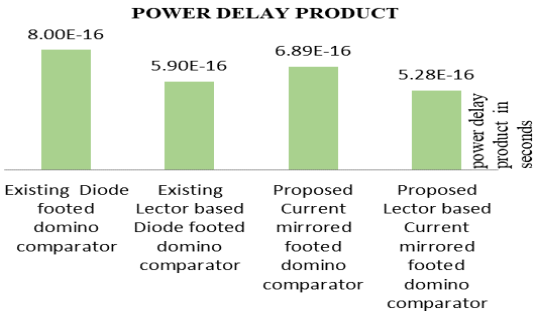

Figure XVI: Power delay product analysis of different domino logic

REFERENCES

[1] Hamid Mahmoodi-Meimand[1] and K.Roy[2], "Diode-Footed Domino: a leakage tolerant high fan-in dynamic circuit design style," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 3, pp. 495-503, March 2019.

[2] Sapna Rani Ghimiray and Manish Kumar "A leakage-tolerant 16-bit Diode Footed Domino Comparator using Lector technique",2017 Devices for Integrated Circuit (DevIC), 23-24 March 2017, 978-1-5090-4724-6/17/$31.00 ©2017 IEEE.

[3] Nagendra Sah, Eesh Mittal An Improved Domino Logic ,International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS-2017).

[4] Sapna Rani Ghimiray, Preetisudha Meher, Manish Kumar, A Leakage-Tolerant 16 – Bit Comparator using Lector Technique Based Footless Domino Logic Circuit, IOP Conf. Series: Materials Science and Engineering 225 (2017) 012139 doi:10.1088/1757-899X/225/1/012139 ICMAEM-2017.

[5] Anil Kumar, Bhavna P. Shrivastava and Ajay Kumar Dadoria ,A new leakage-tolerant domino circuit for wide fan-in gates with CNTFET,IEEE,(ICICIC– 2017)

[6] C. Arun Prasath[1], B. Manjula[2] Design and simulation of low power wide fan-in gates," International-Journal of science and innovative engineering & technology, Vol.1, ISBN 978-81-904760-6-5, May 2016.

[7] A.Dutta1, S.R.Ghimiray2, M.Kumar3, "Performance comparison of 3bit ECRL ADC with conventional logic style," International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT'2016), pp. 444-448, 2016.

[8] A. Manikandan , J. Ajayan , C. Kavin Arasan , S. Karthick K. Vivek High Speed Low Power 64-Bit Comparator Designed Using Current Comparison Based Domino Logic 978-1-4788-7225-8/15/$31.00 ©2015 IEEE

[9] Mansi Gangele, K. Pitambar Patra Comparative Analysis Of Lector And Stack Technique To Reduce The Leakage Current In CMOS Circuits, International Journal of Research in Engineering and Technology Volume: 04 Issue: 07 July-2015

[10] Jeeja Jaculine Let R B, Bharath P and Varatharaj M Power Efficient High Speed Domino Circuit Using Adiabatic Logic, International Journal of Computer Sciences and Engineering Vol.-2(4), pp (126-130) April 2014, E-ISSN: 2347-2693

[11] Preetisudha Meher[1] and K. K. Mahapatra[2], "Modifications in CMOS dynamic logic style: a review paper", Journal of the institution of engineers – springer "Series-B", Vol. 96, pp:391–399, 2013.

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