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A Comparator Circuit Design Using Cyclic Combinational Gate Diffusion Input (CCGDI) - For Low Power, Low Area and High Speed Applications in VLSI Design

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ABSTRACT: Cyclic Combinational Gate diffusion input (CCGDI) - This technique reduces power consumption, area and propagation delay of digital combinational circuits while it maintains low complexity of logic design. Performance comparison with traditional CMOS logic design technique is presented with the help of few examples and comparator

KEYWORDS: Cyclic Combinational Gate diffusion input (CCGDI), *Double Pass Transistor (DPL), CMOS, Gate Diffusion Input (GDI), low power design, comparator.*

I. INTRODUCTION

Integrated circuit technology is anticipated to scale down through a few more technology nodes, enabling several billion transistors on a single chip. Designs need to trade off among performance and power. The power consumption must be reduced for either of the two different reasons: firstly, to reduce the heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. The other reason is to save energy in battery operated instruments like mobile phones, laptops, palmtops, tablets etc. where average power is in milli watts. In CMOS circuits, the power consumption is proportional to switching activity, capacitive loading and the square of the supply voltage. In order to reduce the power consumption several methodologies have been applied. Several techniques have been introduced to deal with the complexities of low power design like Pass Transistor Logic (PTL), Complementary Pass Logic (CPL), Domino logic, Differential Cascade Voltage Switch (DCVS), MOS Current Mode Logic (MCML), Complementary CMOS (C2MOS), and Double Pass Transistor Logic (DPL) etc. Result shows future CMOS technologies will give an advantage for conventional CMOS circuits in terms of power and speed. Morgenstern, Fish and Wagner introduced a new technique of low-power digital combinatorial circuit design- Gate Diffusion Input (GDI).

As different kinds of logic styles are being introduced, researchers are also involved in developing different algorithms to minimize the logic circuits. Binary Decision Diagrams (BDD) has come to the front as possibly the most successful data formation for representing Boolean functions. After several work researchers rewrite the definition of combinational circuits with cyclic loops, giving noticeable performance improvement.

This paper investigates more on that and explores a new technique for designing of power efficient digital combinational circuit by introducing Gate Diffusion Input (GDI) devices in Cyclic Combinational circuits to overcome the challenges in VLSI design. This new approach Cyclic Combinational Gate diffusion input (CCGDI) has been discussed briefly in section II.

II. BRIEF OVERVIEW OF CCGDI TECHNIQUE

To design a digital combinational circuit by Cyclic Combinational Gate Diffusion Input (CCGDI) technique first we focus over two different approaches for low power design. First approach is cyclic combinational method for minimization of the Boolean functions and the second approach is Gate Diffusion Input (GDI) technique which represents Boolean functions by minimum nos. of transistor.

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A. Cyclic Combinational (CC) Circuit

Combinational circuits are generally considered as acyclic (i.e., feed-forward) structured. However, cyclic circuits can be combinational. In cyclic combinational circuit the primary outputs is combinational even when some intermediate signals are sequential.

Every digital circuit deals with 0's and 1's. But actually there is no distinct substantial existence of digital signal: each signal is a continuous real valued function of time f(t), related to a voltage level which is actually analog. This can be explained by the given example, extending the set of Boolean values B= [0,1] to the set of ternary values T= [0, 1, ±], where

Logical [f(t)]= 0 if s(t) < V_{low}
1 if s(t) > V_{high}
± Unknown

The third value '±' indicates that the signal is in doubt & the value is unknown. We can easily determine the value of circuit output when the input values are either '0' or '1' for any combinational circuit but conventionally we cannot determine the output when value of the one of the inputs is '±' unknown. The truth-tables for the common logic gates (AND, OR, NAND, NOR gates) including the '±' values are shown in table 1.

TABLE 1: TRUTH TABLE OF COMMON GATES INCLUDING UNKNOWN VALUES

X	Y	AND (X,Y)	OR (X,Y)	NAND (X,Y)	NOR (X,Y)
0	0	0	0	1	1
0	1	0	1	1	0
0	±	0	±	1	±
1	0	0	1	1	0
1	1	1	1	0	0
1	±	±	1	±	0
±	0	0	±	1	±
±	1	±	1	±	0
±	±	±	±	±	±

From table 1 it can be seen that for two input gates we can get valid output from different six nos. of combinations of inputs including '±' value. The input combinations where one of the inputs is unknown ('±') but output is either 1 or 0, can be used for making structural feedback in combinational circuit elements. In cyclic design feedback should be such that the primary outputs should be able to give the output as '0' or '1' not '±'. So there is no logical feedback that is transmitted to produce the primary outputs. Thus we can reduce the Boolean expression by introducing extra feedback input without affecting the logical behavior of the circuit. For representing the combinational functions into cyclic circuit, two popular methods are available namely: Branch-and-bound algorithm and Karnaugh map methodology.

B. Gate Diffusion Input (GDI) Technique

The GDI technique allows realization of a wide variety of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a less number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power behavior and allowing simple top-down technique by using small cell library. The basic cell of GDI is shown in fig. 1.

1) The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS).

2) Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

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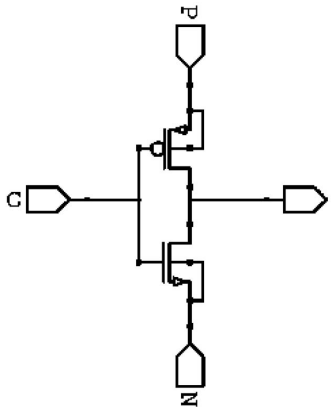

Fig 1. GDI basic cell

TABLE II: VARIOUS LOGIC FUNCTIONS OF GDI CELL FOR DIFFERENT INPUT CONFIGURATION AND CORRESPONDING TRANSISTOR COUNT

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'B	F1	2
B	1	A	A'+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4
B	B'	A	AB+A'B'	XNOR	4

Table II shows how different Boolean functions can be realized by simple change of the input configurations of the GDI cell. GDI logic technique consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be fewer and for this reason GDI gates have faster operation which presents that GDI logic style as a power efficient way of design.

Our approach of low-power digital combinational circuit design using CCGDI technique includes both the above discussed techniques. The following section describes the methodology of CCGDI technique.

III. CCGDI METHODOLOGY

CCGDI methodology includes two steps, i) General Cyclic representation and ii) GDI realization of cyclic function.

A. General Cyclic Representation

For common cyclic representation Karnaugh map methodology is taken. For making of cyclic expression first the dependency graph is drawn. From dependency graph the entity dependent output truth tables are redrawn including that controlling output value in the left hand part of the truth table as another input. Then the minimized Boolean expressions are obtained by means of K-map. The above process is repeated for each and every dependent output to obtain the ultimate cyclic expressions.

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B. GDI realization of cyclic function

Once the cyclic functions are found the next approach is to represent those cyclic Boolean functions with GDI cell. After getting the required CCGDI expressions for the combinational functions the functional and timing analysis is done using standard simulator. For comparative study between CCGDI circuit and conventional CMOS combinational circuit let us take some examples.

1) **Example 1:** A set Of three Boolean functions: Here three distinct functions f_1,f_2 & f_3 are taken randomly. The Boolean expressions and corresponding truth table are as follows:

$$f_1 = \overline{x_1}x_2\overline{x_3} + \overline{x_2}(x_1 + x_3),$$

$$f_2 = \overline{x_1}\,\overline{x_2}\,\overline{x_3} + x_1(x_2 + x_3),$$

$$f_3 = \overline{x_3}(\overline{x_1} + \overline{x_2}) + \overline{x_1}\,\overline{x_2},$$

TABLE III: TRUTH TABLE OF FUNCTIONS DESCRIBED IN EXAMPLE 1

inputs			outputs		
x_1	x_2	x_3	f_1	f_2	f_3
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	0	1	0
1	1	1	0	1	0

To bring cyclic property in the circuit we have listed a dependency between these functions. So a dependency graph can be drawn as fig. 2.

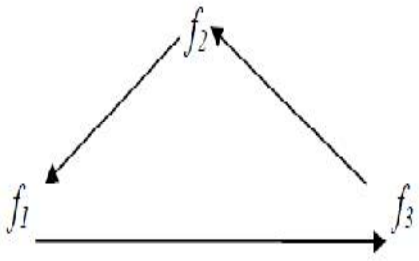

Fig 2. Dependency graph of example 1

So function f_1 will be dependent over f_2, function f_2 will be dependent on f_3 & function f_3 will be dependent on f_1 to produce a complete cycle. Now truth tables can be redrawn as follows:

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TABLE IV: TRUTH TABLE OF EXAMPLE 1 USING CYCLIC DEPENDENCY

Basic inputs			controlling value	output
x_1	x_2	x_3	f_2	f_1
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	1	0

Basic inputs			controlling value	output
x_1	x_2	x_3	f_3	f_2
0	0	0	1	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

Basic inputs			controlling value	output
x_1	x_2	x_3	f_1	f_3
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

As the no of input variable increases, it gives more flexibility in minimization of Boolean function. The Boolean functions can be derived using k-map. Now k-map representations of cyclic functions f_1,f_2 & f_3 are shown in fig. 3.

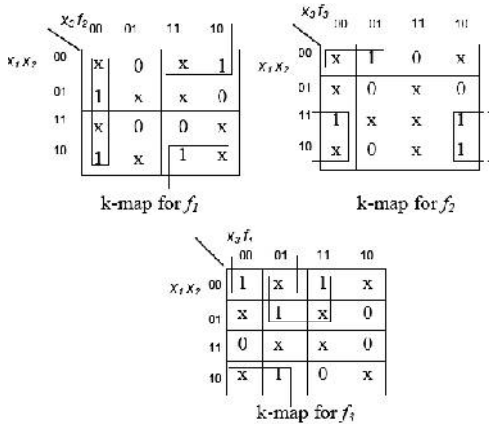

Fig 3. K-map representations of f_1, f_2, f_3.

As it can be seen that these k-maps have more nos. of don't care position which implies better flexibility in establishing Boolean functions. So the cyclic solution for the functions f_1,f_2 & f_3 can be represented as:

$$f_1 = \overline{x_3}\,\overline{f_2} + \overline{x_2}x_3$$

$$f_2 = \overline{x_1}\,\overline{x_2}\,\overline{x_3} + x_1\,\overline{f_3}$$

$$f_3 = \overline{x_1}\,f_1 + \overline{x_2}\,\overline{x_3}$$

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Now cyclic solution for the functions f_1,f_2 & f_3 can be implemented by basic GDI gates using 16 nos. of transistors as shown below in fig. 4

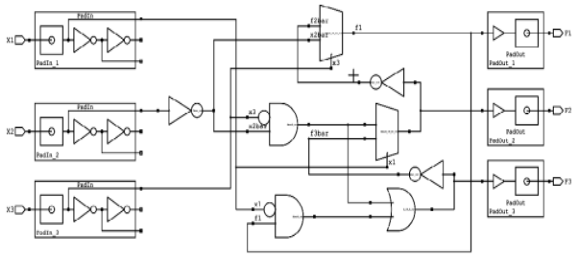

Fig. 4. CCGDl based representation of example 1.

2) **Example2:** A **two bit magnitude comparator** can be taken as another example which has four input lines namely A_1 & A_o indicating A number and B_1 & B_o representing number B. The truth table of a 2- bit comparator is shown in table V,

TABLE V: TRUTH TABLE OF A 2-BIT COMPARATOR

Inputs				Outputs		
A_1	A_0	B_1	B_0	$A>B$	$A=B$	$A<B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

With the help of k-maps the output functions can be represented as;

$$(A > B) = A_1\overline{B_1} + A_0\overline{B_0}(\overline{B_1} + A_1)$$

$$(A < B) = \overline{A_1}B_1 + \overline{A_0}B_0(\overline{A_1} + B_1)$$

$$(A = B) = (A_1 \square B_1).(A_0 \square B_0).....(1)$$

Expression (1) shows acyclic representations of 2-bit comparator. Now the similar outputs are represented in form of dependency with each other in order to create these functions cyclic. So the dependency graph of 2-bit comparator can be drawn as shown in fig. 5 below:

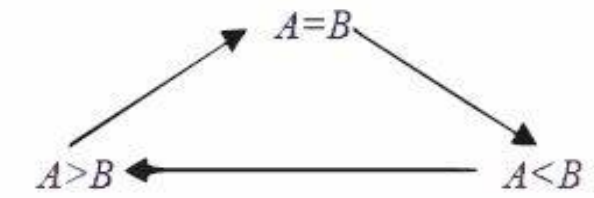

Fig 5. Dependency graph of 2-bit comparator

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From this diagram it can be determined that the output A>B is depending over A<B, whereas A=B is depending over A> B and A<B is depending over A =B. Now the truth table can be redrawn as follows;

TABLE VI: TRUTH TABLE OF CYCLIC 2-BIT COMPARATOR

Basic inputs				controlling value	output
A_1	A_0	B_1	B_0	$A<B$	$A>B$
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	0	0

Basic inputs				controlling value	output
A_1	A_0	B_1	B_0	$A>B$	$A=B$
0	0	0	0	0	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

Basic inputs				controlling value	output
A_1	A_0	B_1	B_0	$A=B$	$A<B$
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	0
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	1	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	1	0

With the help of k-maps the output cyclic functions can be represented as;

$(A > B) = \overline{L}(A_1\overline{B_1} + A_0\overline{B_0})$, Where L=A<B

$(A < B) = \overline{A_1}B_1 + \overline{E}B_0(\overline{A_1} + B_1)$, Where E=A=B

$(A = B) = \overline{A_1}\,\overline{B_1}(A_0 \square B_0) + A_1\overline{G}(A_0 + \overline{B_0})$, Where G=A>B …….. (2)

IV. IMPLEMENTATION OF CCGDI TECHNIQUE

Three examples which have been described in section III, are now being implemented using CCGDI technique and their functional and timing results are tested and compared with conventional CMOS based circuits in standard simulator. Beginning with first example, both the schematics of conventional CMOS based circuit and proposed CCGDI circuit are simulated for 80ns by providing different input combinations shown in fig. 7. Corresponding transient response of outputs are plotted in fig. 8 and fig. 9 respectively.

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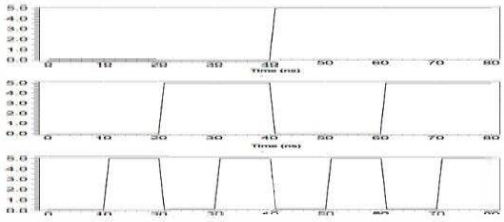

Fig. 7. Different input combinations of X_1, X_2 ,X_3 for example 1 (from top to bottom X_1, X_2 ,X_3 - respectively)

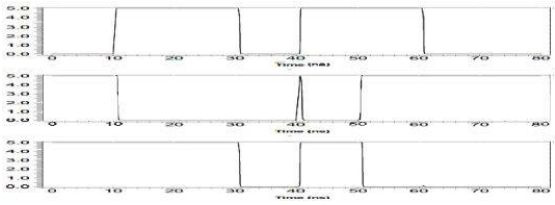

Fig. 8. Transient responses of f_1,f_2 & f_3 using static CMOS technique (from top to bottom -. f_1,f_2 & f_3 respectively)

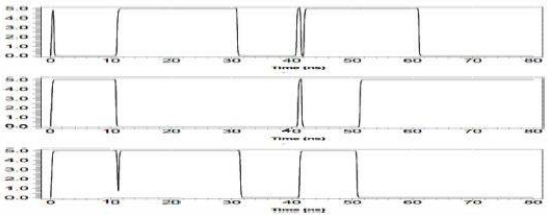

Fig. 9. Transient responses of f_1,f_2 & f_3 using CCGDl technique (from top to bottom f_1,f_2 & f_3 respectively)

The second example of comparator is simulated for 160ns by providing different input combinations shown in fig. 10. Corresponding transient response of outputs are plotted in fig. 11 and fig. 12 respectively.

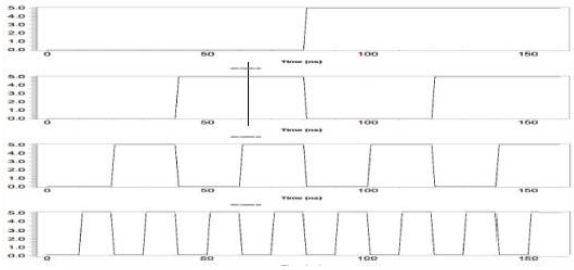

Fig. 10. Different input combinations for 2 bit comparator (from top to bottom – A_1,A_o, B_1, B_o respectively)

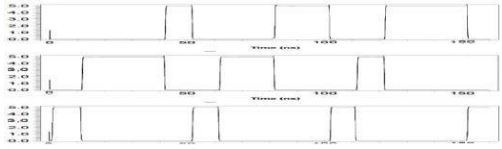

Fig. 11. Transient responses of outputs of CMOS two bit comparator (from top to bottom - A>B, A<B & A=B respectively)

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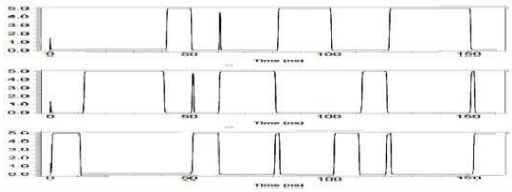

Fig. 12. Transient responses of Outputs of two bit comparator using CCGDT technique (from top to bottom - A>B, A<B & A=B respectively)

The third example of seven segment display decoder is also implemented using conventional CMOS technology and proposed CCGDI technique. Both the schematics are simulated for lOOns by providing different inputs Corresponding transient responses of outputs

From the simulation results it can be easily understood that the proposed CCGm based circuits have the same logical behaviour as like the conventional CMOS based circuits where as the power & timing behaviours are improved as tabulated in the table VII & VIII,

TABLE VII: POWER COMPARISON BETWEEN CMOS AND CCGOT CIRCUITS

		Power Analysis(mw)		
		Avg. Power	Max Power	Min Power
Example 1	CMOS	12.985	39.607	2.4243
	CCGDI	7.0861	43.088	0.86921
Two bit comparator	CMOS	50.44385	546.7599	17.95799
	CCGDI	35.2578	330.6739	11.98812

TABLE VIII: DELAY COMPARISON BETWEEN CMOS AND CCGOT CIRCUITS

		Transistor count (core)	Transient Delay Analysis(ns)		
			Rise time delay	Fall time delay:	Avg. tr. delay
Example 1	CMOS	42 nos.	0.2993	0.2945	0.2962
	CCGDI	16 nos.	0.1263	0.1201	0.1231
Two bit comparator	CMOS	88 nos.	1.3472	1.7112	1.5292
	CCGDI	30 nos.	0.4903	0.3864	0.4384

Fig. 13 shows the power delay product comparison of CMOS logic technique and proposed CCGm technique.

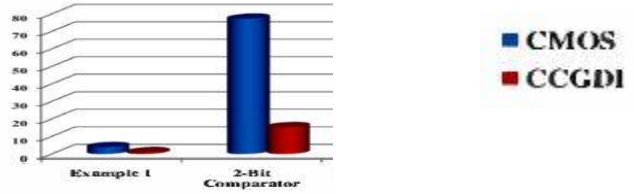

Fig. 13. Power-Delay Product Comparison of different examples described in sec. III

V. CONCLUSION

From the above results it can be concluded that our proposed CCGm technique has got better performance in terms of speed, power and area consideration in comparison with the conventional CMOS combinational circuits. The power delay product has been improved upto 78% in case of CCGm from CMOS. The transistor count reduces 61 % in case of example 1, for 2-bit comparator reduction rate is 66% and 83% in case of seven segment decoder. This implies

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for more complex functions reduction rate is more. It turns out that in contrast to older process technologies, this approach is more suitable for industrial usage in advanced process technologies.

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