ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

Design High Performance HV Multiplexer with Sigma Delta ADC for Battery Management System

S.Gayathri [1], M.Siva Kumar [2]

M.E Student, Department of Electronics and Communication Engineering, Adhiyamaan College of Engineering, M.G.R Nagar, Hosur, India[1]

Associate Professor, Department of Electronics and Communication Engineering, Adhiyamaan College of Engineering, M.G.R Nagar, Hosur, India[2]

ABSTRACT: This paper presents a voltage monitoring IC using sigma delta based high voltage multiplexer and sigma delta ADC for battery management systems(BMSs). In our previous technology the voltage monitoring IC unable to accommodate high input volts . Semiconductor process is used to recognize a solution on silicon in the voltage monitoring IC which is controlled by the voltage drop limitation among gate and source of HV devices. To overcome the limitation, HV multiplexer is proposed in this paper in tanner EDA tool. In addition Delta sigma modulator is proposed using the 13 parallel decimators for the 13 ADCs, which is measuring individual cell voltages, cell temperature and battery current and to produce high speed in HV multiplexer.

KEYWORDS : Battery Management System ;Sigma Delta ADC;High Voltage Multiplexe ;High Voltage(HV)

I. INTRODUCTION

Generally the functions of a BMS include battery, power and energy management.Here **Battery management** Refers all functions that are required to ensure proper battery operation and **Power management** includes functions that reduce power consumption by the system parts with respect to active hardware and software design changes e.g. lowering or powering components and signals down when not in use.As well as **Energy management** includes functions that ensure energy conversions in the system are at its lowest levels e.g. zero-voltage and zero-current switching in the battery charger Problems with current commercial BMS is Size and complexity do not allow them to be installed in a small space.To overcome the energy management problem to measure all individual cell voltages in battey management with the help of tanner EDA tool.

II. LITERATURE SURVEY

High voltage batteries are used in the telecommunications, aviation and motor industries. Thesebatteries provide power or backup power to the different systems connected to them.Measurement of a low value DC voltage is easily measured using specific integrated circuits (ICs). When an individual cell voltage in a high cell count battery stack needs to be measured it cannot be done with ICs due to the high stacked common mode voltage with respect to the referenced ground of the system (Ibanez & Dixon, 2004) (Williams & Thoren, 2008).

The Battery management system operate with five blocks .There are battery Interconnect Modules(BIM) ,main Controller ,Analysis, logging and telemetry and Communication .Here the BIM used to detecting the battery status by HV multiplexer (HVMUX) .

Here the HVMUX is composed of five blocks .There are HV switches ,HV subtractors, LV multiplexer and LV multipler .several HV switches have been reported [1]-[2]. A 2 × VDD switch was designed using 0.18 μm CMOS process. It reports 7-V tolerance so it is not possible to be used in a large scale HV BMS. Several integrated HVMUX have been reported [3] this integrated HVMUX fabricated with a 0.35 μm 50-V CMOS process it gives large voltage

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

distortion in the output .A 16:1 analog MUX is drive with 15V HV analog switches [4] used SOI technology.here the SOI technology is not suitable for power device .

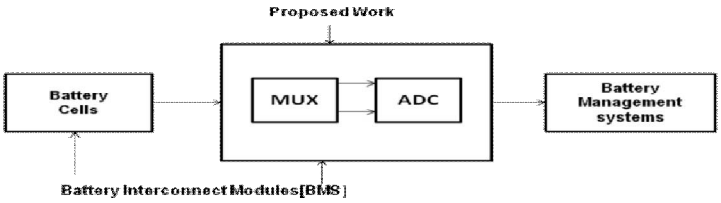

Fig.1.Block diagram of BMS with combined HVMUX and sigma delta ADC

In this paper HVMUX are composed with 13 bit parallel sigma delta ADC to resolve the power consumption problem .In section II we explain about HVMUX .In section III the HVMUX is disclosed including sigma delta ADC .In section IV describes the schematic of HVMUX with ADC .In section V we demonstrate the power measurement of proposed HVMUX .

III. HIGH VOLTAGE MULTIPLEXER

A multiplexer can use addressing bits to select one of several input bits to be the output. A selector chooses a single data input and passes it to the MUX output.It has one output selected at a time.The early CMOS switches and multiplexers were typically designed to handle signal levels up to ±10 V while operating on ±15-V suppliesToday, analog switches and multiplexers are available in a wide variety of configurations, options, etc., to suit nearly all applications. On-resistances less than 0.5 Ω, pico ampere leakage currents, signal bandwidths greater than 1 GHz, and single 1.8-V supply operation are now possible with modern CMOS technology. In BMS HVMUX including HV switches and HV subtractor and divider .combination of eight switch cell connected together to form HV switches

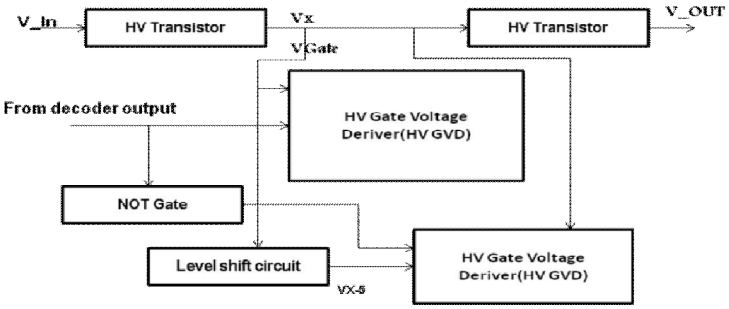

Fig.2.HV Switch Cell

Fig.2 Describes when Vx is equal to VGate ,the HV Transistor is turned off.By contrast when Vx is equal to Vx-5v ,The hv Transistor is turned on .

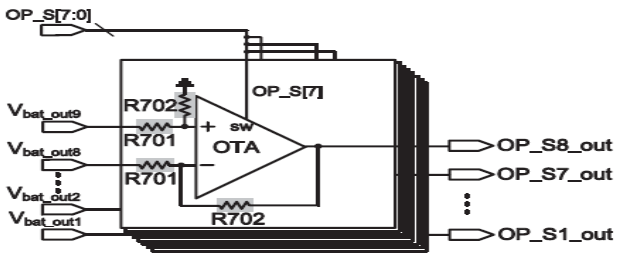

Fig .3. Block of HV subtractors and divider

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

Fig .3 shows block of HV subtractors and divider composed of operational transconductance amplifiers(OTA).Here the input of HV subtractors and divider taken from output of HV switch cell .The R701 and R702 are used to produce lower voltage to LV multiplexer . Here LV MUX composed of 8 transmission gates and selects anyone of inputs to the output .

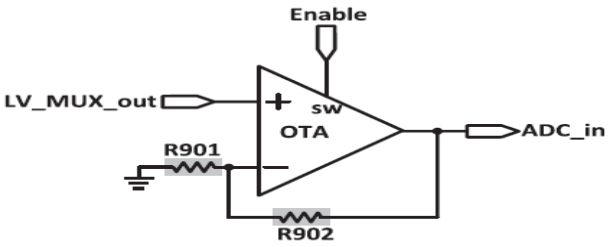

Fig .4.Schematic of LV multiplier.

Fig .4 shows schematic of LV multiplier .The final stage of HVMUX is LV multiplier .it multiplies to Voltage of LVMUX passes to sigma delta ADC

IV. SIGMA DELTA ADC

The low power Delta Sigma modulator is important to understand not only the structure and function of the device. Delta Sigma is an architecture for digital systems where, high precision analog circuitry is technologically challenging.The main advantages of sigma delta modulators are increase the functionality of BMS and reduce the BMS cost. Whether the limitations are due to the available technology or the cost, significant limits must be assumed in a practical design.

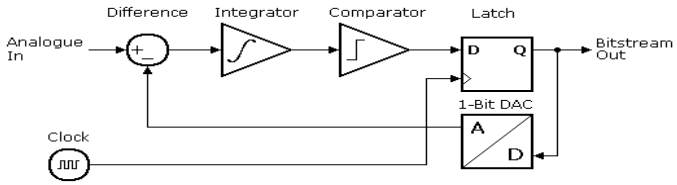

Fig .5.Schematic of sigma delta ADC

Fig 5 shown a Delta Sigma modulator can be broken down into five functional blocks there are Subtractor, Integrator,Comparator, A/D converter, feedback D/A converter, and the output register. Here the final ADC resolution determined by comparator and subtractor .The comparator is the most critical part of sigma delta ADC .Here the comparator performance related to size and structure . The integrator is the most resource hungry component, because it requires large passive components for noise attenuation. Since area is the most limiting factor, the integrator design must be considered first. The feedback D/A converter are used to reconstruct the analog signal . In one bit DAC linearity is determined by the accuracy of switching between the reference signal, for high switching accuracy the system will be very linear.

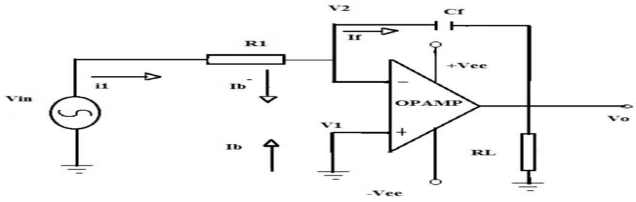

Fig .6. Schematic of integrator

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

The Op-Amp Integrator is an operational amplifier circuit which performs the mathematical operation of integration. It acts like a storage element which produces an output voltage proportional to the integral of its input voltage with respect to time.

Fig.6 shows When a voltage VIN is applied to the circuit the capacitor is little resistance and act like a short circuit giving voltage gain of less then one. No current flows in to the amplifier, as the feedback capacitor begin to charge up, its resistance decreases this result in producing an output voltage that continues to increase until the capacitor is fully charged. At this time the capacitor acts like an open circuit, which blocks the further flow of Dc current. The ratio of feedback capacitor to input capacitor now results in to infinity gain.The rate at which the output voltage changes or increases is determined by the value of resistor and capacitor, by changing this RC time constant value either by changing value of "C" or by changing value of "R".The time by which it takes to reach the saturation can be changed

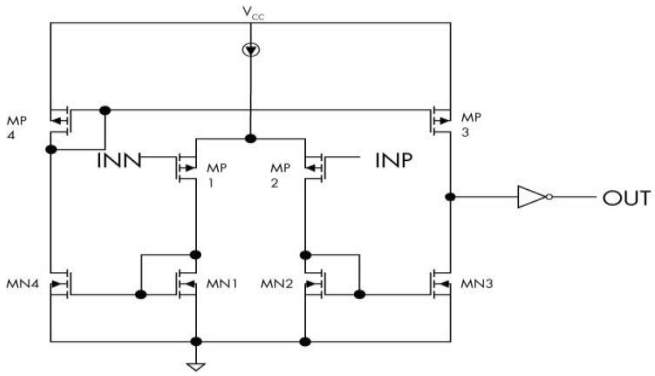

Fig.7. Comparator of sigma delta modulator

In fig 7 shows the comparator senses the charge imbalance produced at the preamplifier in the input and reacts to the imbalance so as to create desired digital output. It can also be called as current comparator. The total operation of the comparator is divided into two phase. When the clock is high, the transistor acting as switch closes and short circuits the outputs and set them to a certain DC level around Vcc

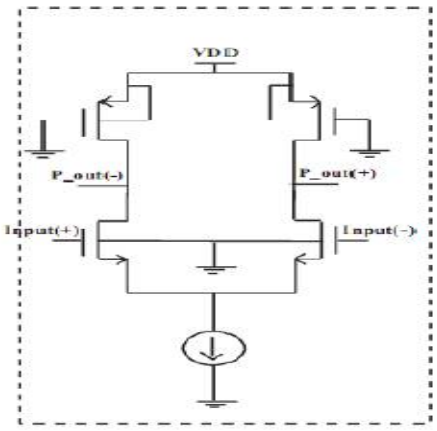

Fig.8.stucture of dynamic latch

In Fig.8 dynamic latch is driven with a clock signal. During the active phase of the clock (clk=1), the transmission gate is closed and the latch acts transparent where as the inverter is directly connected to the input. During the other phase (clk=0), the transmission gate is open and the output of inverter is determined by the node. Finally the D-Latch output given to the DAC to convert digital to analog process.

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

V. SCHEMATIC OF HV MUX WITH ADC

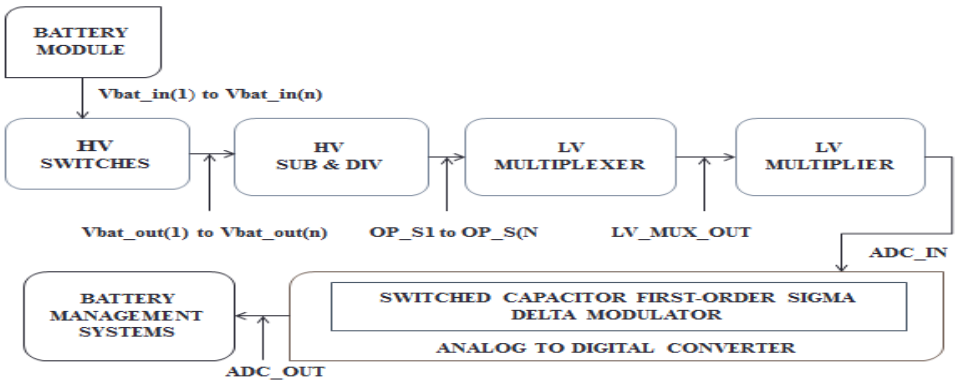

Fig.9.Overview of HV MUX with sigma delta ADC

Fig .9. shows overview of proposed HV MUX with sigma delta ADC .Here the HV MUX are simultaneously connected with sigma delta modulator .In previous technology the OTA techniques are used in this paper the OP-AMP techniques are used due to reduce the power consumption .

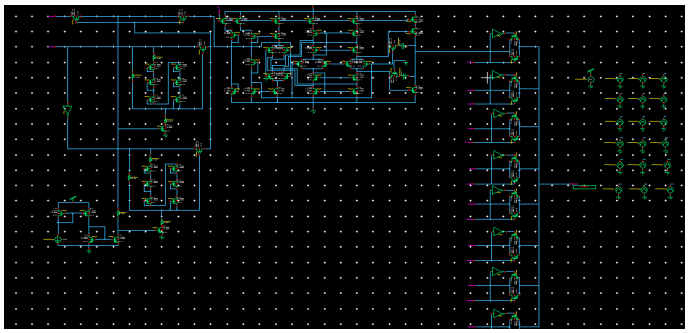

Fig.10.schematic diagram of one cell high voltage multiplexer

The Tanner EDA tool is used to implement the high voltage multiplexer . In this above discussed Thesis the single hv multiplexer cell upto LMUX is implemented in S-Edit and their Simulation Results are shown in fig.10

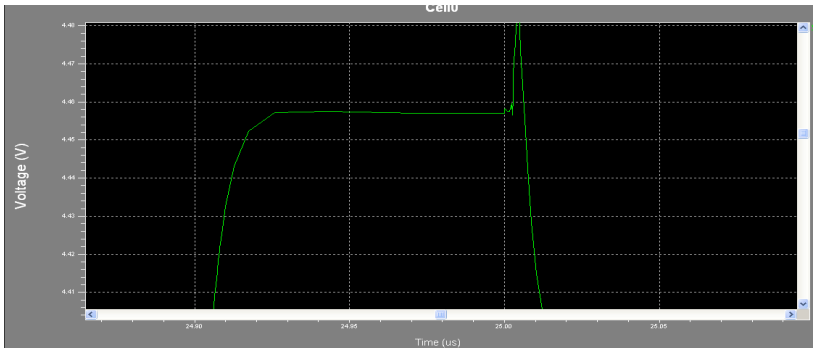

Fig .11. simulation result of hv switches and hv sub &divider with lv mux

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

The above simulation shows the output of hv multiplexer upto hv switches and hv subtractor with lv multiplexer .here the hv switches composed with the help of HVGVD and the level shifter .here the 2 transistor used to producted the over voltages with the help of parasitic diodes .Here the hv gate voltage driver used to prevent the over voltage damage and the level shift circuit used to limit the power dissipation in the battery management systems .The hv subtractor and divider is composed with the help of OTA technique.this OTA are used to enlarge output voltage range.In this OTA the enable pin is the power gating signal to activate the entire OTA for the sake of power saving.

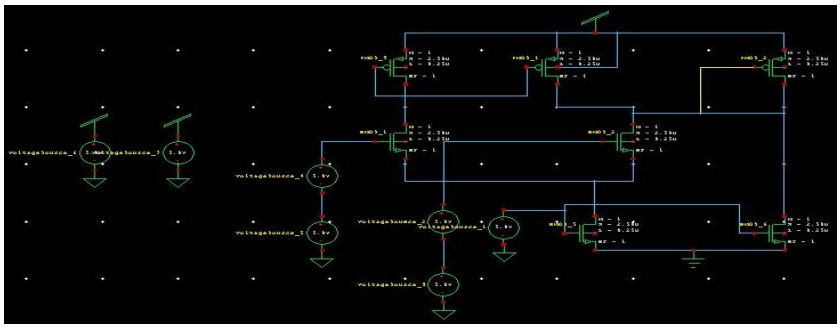

Fig.12.Schematic digram for OPAMP in sigma delta ADC

Here the HV MUX are additionally attached with sigma delta ADC in parallel .The sigma delta ADC are design with the help of OPAMP .In fig .12 shows schematic digram of OPAMP ,due to these OPAMP integrator circuit is formed and produce high performance output.

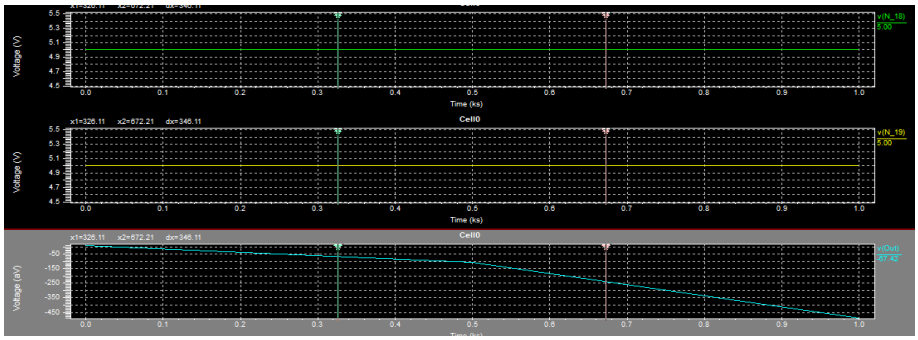

Fig.13. Simulation output of opamp

The opamp shows in Fig.13. her ethe opamp integrator output produce high effective signal due to high input frequency .

V. CONCLUTION

The design of HV multiplexer propose a total HV solution on silicon for BIMs. This design is implemented using a typical0.25 μm cmos process such that it can be easily integrated in a possible SoC solution for BMS. The measurement results justify a high performance analog HV multiplexer (HVMUX) with sigma delta ADC . Additionally the HV multiplexer are composed with parallel switched capacitor first order sigma delta modulator ADC .This new high voltage multiplexer gives the following features are High ADC accuracy and Reduced power consumption

ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

VI. FUTURE ENHANCEMENTS

In the BMS the HV MUX used to enable simultaneous measurement of esch of cell voltages and the individual cell temperatures in future additionally 13 parallel ADCs are provided per IC .these measure information will be give low power consumption in the battery management system .here MUX with sigma delta ADC are composed upto OPAMP .In future ADC are attached with comparator and DAC and to produce effective output.

REFERENCES

[1] E. K. F. Lee, "High-voltage tolerant stimulation monitoring circuit in conventional CMOS process," in Proc. Custom Integr. Circuits Conf., Sep. 2009, pp. 93–96.
[2] D. A. Adams, H. A. Barnes, M. D. Fitzpatrick, N. P. Goldstein, W. L. Hand, W. L. Jackson, et al., "A radiation hardened high voltage 16:1 analog multiplexer for space applications (NGCP3580)," in Proc. IEEE Radiation Effects Data Workshop, Jul. 2008, pp. 82–84.
[3]J. Borg and J. Johansson, "An ultrasonic transducer interface IC with integrated push-pull 40 Vpp, 400 mA current output, 8-bit DAC and integrated HV multiplexer," IEEE J. Solid-State Circuits, vol. 46, no. 2, pp. 475–484, Feb. 2011
[4] D. A. Adams, H. A. Barnes, M. D. Fitzpatrick, N. P. Goldstein, W. L. Hand, W. L. Jackson, et al., "A radiation hardened high voltage 16:1 analog multiplexer for space applications (NGCP3580)," in Proc. IEEE Radiation Effects Data Workshop, Jul. 2008, pp. 82–84.
[5] D. Andrea, Battery Management Systems for Large Lithium-Lon Battery Packs, Norwood, MA, USA: Artech House, 2010, pp. 47–52.
[6] M. Kultgen, "Managing high-voltage lithium-ion batteries in HEVS," Inf., News, Bus. Strategy Electron. Des. Eng., vol. 54, no. 7, pp. 45–52, Apr. 2009.
[7] R. Kliger, "Integrated transformer-coupled isolation," IEEE Instrum. Meas. Mag., vol. 6, no. 1, pp. 16–19, Mar. 2003.
[8] C.-H. Hsu, K.-C. Chang, Y.-C. Ou, K.-Y. Liao, and C.-L. Wey, "On the implementation of CAN buses to battery management systems," in Proc.IEEE Int. Midwest Symp. Circuits Syst., Aug. 2011, pp. 1–4.
[9] K. P. Ng, M. C. Lee, W. T. Chan, R. Barsatan, and M. Chan, "Universal high voltage multiplexer for CMOS OTP memory applications," in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits, Dec. 2008,pp. 1–4.