ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

Low Capture Power Scan shift Environment by using EDT Architecture

[1]M. Siva Kumar, [2]Dr.S.K.Srivatsa

[1]Associate Professor, Dept of ECE, K L University, Andhra Pradesh, India

[2]Sr.Professor, Bharath University, Chennai, India

ABSTRACT: This paper presents a new and comprehensive power-aware test scheme compatible with a test compression environment. The key contribution of the paper is a flexible test application framework that achieves significant reductions in switching activity during all phases of scan test: scan loading, unloading, and capture.

KEYWORDS: DFT, Flip Flop, LFSR, ATPG, Reconfigurable.

I.INTRODUCTION

On-chip test compression has quickly established itself as one of the mainstream DFT methodologies . It assumes that a tester delivers test patterns in a compressed form, and on-chip decompresses expand them into the actual data loaded into scan chains. Typically, decompresses fill don't care bits with random values, and therefore the amount of flip-flop toggling during test may result in a power droop condition that would not occur in the chip's mission mode. This necessitates managing tests such as scan or logic BIST so that they fall within certain power consumption constraints. Otherwise, the power dissipation can increase by a factor of 3 compared to the functional mode of operation, and is only expected to worsen with scan patterns already consuming 30x the mission mode's peak power . The bulk of test power consumption can also be attributed to unloading test responses with high transition counts. Excessive switching activity in scan chains and other parts of the circuit results in overheating or supply voltage noise, both causing a device malfunction, and thus loss of yield, reliability degradation, shorter product lifetime, or even permanent damage of a circuit.

Low power test data encoding schemes adopt conventional LFSR reseeding techniques to reduce the scan-in transition probability. In particular, the method of uses two LFSRs to produce actual test cubes and the corresponding mask bits. Outputs of both LFSRs are AND-ed or OR-ed to decrease the amount of switching. The use of extra seeds may compromise compression ratios, and therefore the scheme of divides test cubes into blocks and only uses reseeding to encode blocks that contain transitions. Other blocks are replaced with a constant value which is fed directly into scan chains. Some of the above schemes such as design partitioning and scheduling can reduce global power during both shift and capture. Even if they are employed, power reduction is often still necessary for the design partitions being tested in a given session. Thus, a method is required that is nonintrusive to the design and design flow; can control power during scan loading, unloading, and capture; and supports embedded compression with high compression ratios. In this paper, we describe a comprehensive, compression friendly scheme aimed at reducing switching activity during all scan test phases: scan loading, unloading, and capture. It employs a controller that either allows a given scan chain to be driven by a power-aware EDT decompress or, or by a constant value fixed for the entire scan load. The controller's configuration is held constant for all cycles of a given scan load but is reloaded for every pattern with minimal control data. The same controller may be used to decide which scan chains remain in a shift mode during the capture cycle by judiciously disabling scan clocks. This is affective at reducing toggling during capture and unloading, especially when the scan chains kept in the shift mode loaded constant values. An alternate method to reduce switching during capture uses ATPG to turn off clock gaters unnecessary to target certain faults. This approach allows ATPG to prevent a large number of flip-flops from changing their states with relatively few specified bits, and with no modifications to the design.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

II RELATED WORK

Patterns generated for scan-based tests have traditionally tended to ignore power consumption as their primary objective was to maximize the fault coverage regardless of switching activity. Moreover, the same generation process was aimed at reducing the number of vectors and thereby reducing the ATE time. Typically, ATPG uses dynamic compaction to reduce a pattern count. Starting from a test cube generated for a primary target fault, dynamic compaction expands this cube to cover other faults by assigning appropriate values to unspecified positions. Thus, the number of scan chains having specified bits gradually increases as dynamic compaction progresses. With the concern over test power dissipation, however, one needs to minimize the number of scan chains with specified bits while also minimizing a possible impact on the pattern count. As a result, scan chains with very low or zero fill rates may serve as a baseline in reducing scan shift power. Consider, as an example, results of experiments aimed at analyzing the number of scan chains populated by specified bits, and impact this quantity may have on a pattern count. A conventional EDT was used as the experimental platform. In particular, we try to limit the number of scan chains that feature specified cells as follows:

- dynamic compaction is carried out only if a test cube has less than 20% of scan chains with specified bits,
- half of scan chains with no specified bits are filled with a constant value (in the experiments these chains are selected randomly),
- logic values for the remaining scan chains are determined by the on-chip decompression logic.

III PROPOSED ARCHITECTURE

1.Low Power Test Architecture:- Observations presented in the previous section clearly indicate that on-chip test data decompression can be taken to a new level by appropriately engineering the low power scan test application. Since deterministic test vectors have typically only a small fraction of bits specified, the remaining scan cells can be either randomly filled with 0s and 1s, or they may assume other forms of filling without com promising test coverage. Furthermore, as shown earlier, very often locations of specified bits can be confined to a few scan chains. Consequently, we can feed these scan chains directly from a test data decompressor while replacing all don't care positions in the remaining chains with a constant value. Such an approach may significantly reduce the number of transitions during scan-in shifting. A solution implementing the above idea is shown in Fig. 1.Input channels provide compressed test patterns to the decompressor. The same channels can be used to deliver information to a control block. The control block comprises a control register and combinational XOR logic driven by data stored, in a compressed form, in the register. The control block outputs gating signals to AND (alternatively OR) gates such that indicated scan chains can be either connected with the decompressor or can be fed by a constant value of 0 (1) on a per pattern basis.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

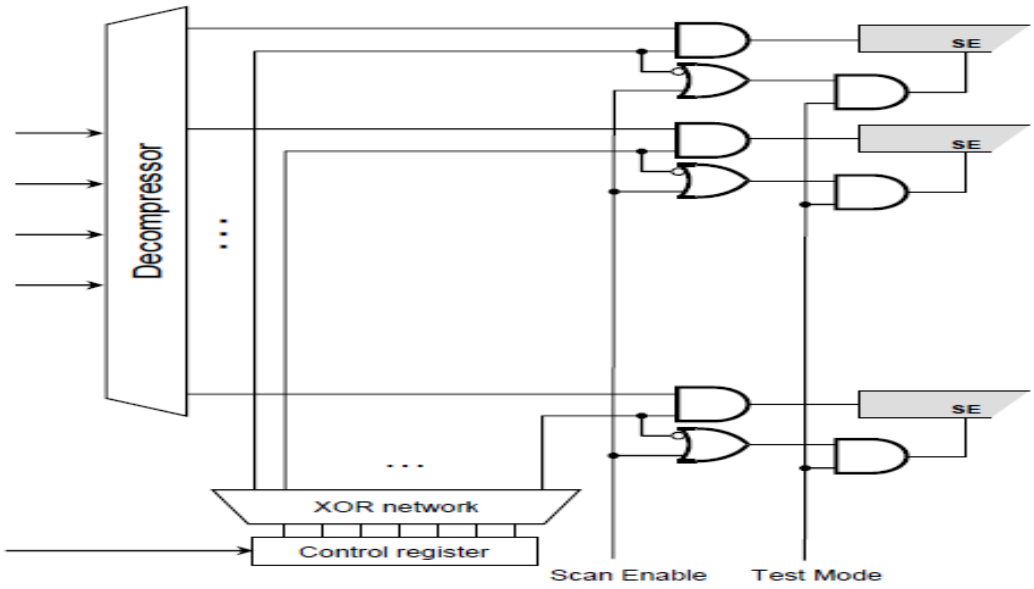

Figure 1 Scan Based Low Power Scheme

The bulk of power dissipation is attributed to responses that usually exhibit high transition counts. As shown earlier, reduction of capture and shift-out power can be achieved due to error propagation sites that are typically confined to a few scan chains, only. Thus, one can avoid capturing data that would overwrite the otherwise constant values being scanned in. Some extra safety precautions can be essential, however, when relying on this concept.
Although it may be safe, during capture, to maintain an asserted scan enable signal for a scan chain that loaded constant values, it is not safe to do so for a scan chain that loaded non-constant values from the decompressor. This is because scan paths are almost never timed to operate at functional frequencies. So if one shifts a non-constant content content of a scan chain at speed, the result can be deemed unpredictable. Assuring reliable values in such scan chains requires, therefore, masking out many scan cells, which in turn can severely affect compression. A way around this problem is to tie the control of the stimuli with that of scan enable such that only scan chains which load constant values are kept in the shift mode during capture.

This is the principle behind a solution shown in Fig. 1 (note that the *Test Mode* input is set to 1 for the entire test session). We assume that the same controller is used for constant stimuli and scan enable. As a result, only one solver is needed since the values of the stimuli and scan enable controls are now tied to each other. If a scan chain loads constant values, then its scan enable will be kept high during the capture cycle, forcing low toggling capture and scan shift-out operations. For a scan chain which must be loaded by the decompressor (de-asserted scan enable during capture), the corresponding low power controller output is 1, allowing the input *Scan Enable* to take over.

Note that it should be possible to partly separate controls such that every scan chain with a scan enable asserted during capture is loaded with constant values while those with scan enable de-asserted during capture can either load constant values or load values from the decompressor. This allows improved power reduction of the stimuli if one does not have sufficient granularity to control scan enable. In other words, some scan chains would load constant values even though those values may change during capture.

2.Scan Shift in Operation:

The combinational part of the control block is designed as an *m*-input *n*-output XOR mapping circuit, where *m* is the number of control bits, and *n* is the number of scan chains. In other words, each output of the block is obtained by XOR-ing certain control bits. The XOR network is configured in such a way that it guarantees high encoding efficiency, i.e., a close to 100% ratio of successfully encoded pre-specified gating signals to the number of control bits. The control circuitry operates as follows. For all scan chains having specified bits, the corresponding gating signals

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

should be chosen in such a way that the AND gate have 1 on its input. Consequently, these scan chains can be driven directly from the decompressor. This process continues until pre-specified power limits are reached. As for the remaining scan chains, one can determine, using the XOR network and the control bits found earlier, those gating signals that were not encoded. The gating circuitry of Fig. 1 allows the decompressor to drive approximately 50% of such scan chains, while the remaining ones receive a constant 0. Indeed, a single output of the XOR network is producing 0 with probability 0.5 (except rare cases when the number of asserted control variables is very small), and thus the gating signal reaches the AND gate and then a scan chain as a constant 0. Note that several experimental results [5] indicate lower switching activity when the scan chains are loaded with the constant 0 rather than the constant 1. Even if this is circuit-specific feature, it nevertheless appears to be the case across several designs.

Two constant stimuli. In certain applications it might be desirable or convenient to feed scan chains with both logic values of 0 and 1 acting as constant stimuli. Consider scan chains that were not the subject of encoding, as discussed in the previous paragraph. The gating circuitry shown in Fig. 2 allows the decompressor to drive approximately 25% of such scan chains, while 50% of them receive a constant 0, and 25% have a constant 1. In other words, roughly 75% of scan chains with no specified bits will have no transitions at all. Indeed, as shown earlier, a gating signal reaches the AND gate and then a scan chain as a constant 0 with probability 0.5. On the other hand, in order to get a constant 1, two gating signals are needed - one set to 0 and driving the OR gate, and the other one set to 1 and feeding the AND gate. Clearly, the XOR network outputs this combination with probability 0.25.

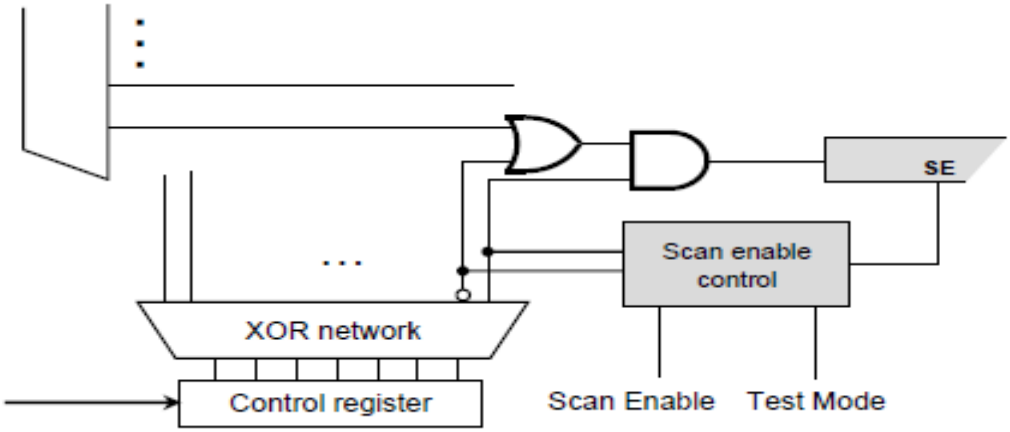

Figure 2 Producing Constant 0 and 1

The fraction of scan chains driven by the decompressor can be changed in the manner of Fig. 5 by adding a *biasing circuitry*, i.e., the group of AND gates driven by the XOR network. With these gates in place, the decompressor is capable of driving approximately 25% of scan chains. This percentage can be reduced even further by adding more inputs to the AND gates. For example, the third input reduces the percentage of scan chains driven by the decompressor down to 12.5%, while the fraction of scan chains getting the constant value of 0 increases accordingly, as shown earlier.

Reduction of control data volume. When generating test patterns, it is possible to make different test patterns sharing the same control data such that the control data can be loaded into the programmable controller only once for multiple test patterns and only the unique control data is stored in the external tester. To maximize the control data to be shared with different test patterns, the ATPG can be enhanced to prefer the control data that meets current requirement and is used by the test patterns generated before when there are multiple choices.
Reconfigurable biasing logic. To further enhance ability of a biasing circuit to reduce the switching activity during scan shift, it can be designed as a reconfigurable device. In its simplest form, it can allow a programmable selection of the XOR logic outputs employed to drive AND gates, as depicted in Fig. 3. It may also consist of multiple modules with different probabilities of forcing constant stimuli. A programmable controller is then used to select one of the biasing circuits. Depending on the implementation, the reconfigurable biasing circuit can be used in two modes:

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

- the selected biasing circuit remains unchanged during the whole scan shift period,
- various biasing circuits are chosen for different scan chain segments during scan shift.

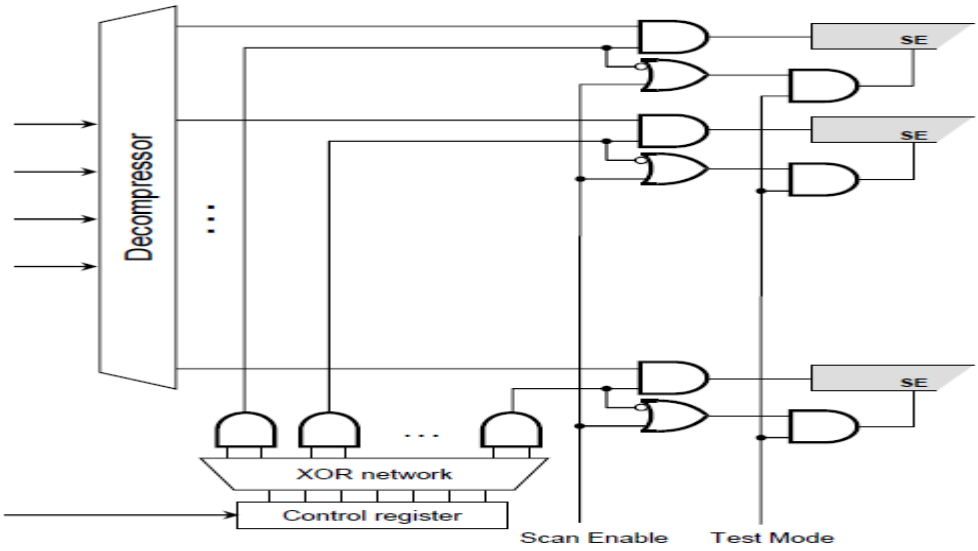

Figure 3 Biasing Circuit

3.Enhanced Shift in:

The low fill rates make it also possible to deliver the identical test data to scan chains for a number of shift cycles directly from the decompressor, thereby further reducing the total number of transitions. In order to implement this idea, however, a mechanism is required to sustain the outputs of a decompressor for more than a single clock cycle, while allowing the decompressor to change its internal state to ensure successful encoding of next specified bits.
Our low power solution assumes that the scheme presented in the previous section is integrated with the on-chip test data decompressor as shown in Fig. 4 (its stand-alone versions presented in [11]). The same data are now provided to the scan chains for a number of shift cycles through s*hadow register* placed between the ring generator and the phase shifter. It captures and saves, for a number of cycles, a desired state of the ring generator, while the generator itself keeps advancing to the next state needed to encode another group of specified bits. As a result, independent operations of the ring generator and its shadow register allow virtually any state which causes no conflicts with specified bits to reduce a transition count.

A single input channel suffices to facilitate the operation of the shadow register. Every shift cycle, a control bit is sent to the decompressor in order to indicate whether the shadow register should be reloaded with the current content of the ring generator. If a given control bit is set to 1, then the shadow register updates its state before the ring generator reaches its next state. Instead of the control channel, one can use the decompressor input channels to deliver the control information merged with the seed variables, as shown in Fig. 4. All inputs drive an XOR tree which basically computes a parity signal for input variables injected during a given shift cycle. If the parity of inputs is odd, then the shadow register is reloaded before new seed variables enter the ring generator. Otherwise, the content of the register remains unchanged. As a result, in addition to silent scan chains loading constant stimuli, one can reduce the degree of toggling in those scan chains that are driven directly by the decompressor, thus reducing the total switching activity even further.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

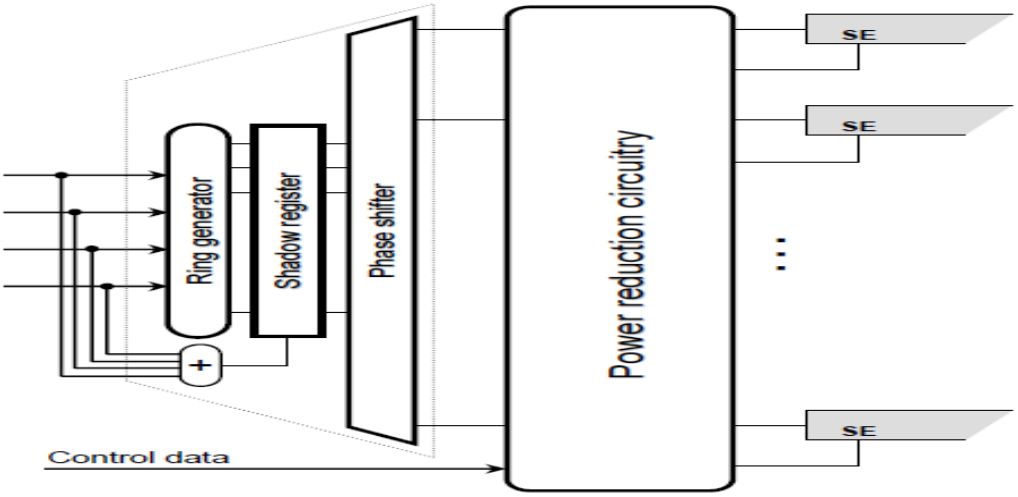

Figure 4 Shows Register in Decompressor

4.Caputure and Scan Shift out:-

Consider now scan operations during capture of test responses and shifting them out of the scan chains. Figures 1, 2, and 3 show the solution in which the same XOR network as before acts as a capture control circuitry that gates the scan enable signals. In Fig. 1, for instance, once all control variables are known, status of those scan chains that were not the subject of encoding will be determined such that approximately 50% of these scan chains may remain in the scan shift mode, that is, they do not record test results since the scan enable signal is asserted, while the remaining scan chains capture actual test responses. As a result, the power dissipation during capture cycles can be significantly reduced. Furthermore, many of the scan chains that do not capture test responses maintain their low toggle test patterns loaded earlier. Consequently, when the entire circuit is placed in the scan mode again, that preserved scan content facilitates suppression of flip-flop toggling toggling during shift out operations

Clock gating. Asserting separate scan enable signals during the capture cycles for each scan chain or group of scan chains that load constant values may not be practical in some design flows. An alternative solution with no impact on the design flow is to leverage the embedded clock gaters already available in many designs to reduce the power consumption. The clock gaters are simple devices inserted between a clock line and the corresponding state elements. If set properly, they prevent clock pulses from reaching selected flip-flops. As a result, the capture power can be reduced by forcing those memory elements to hold their states.

In a mission mode, the clock gaters are controlled by functional enable logic fed by scan cells. To support scan shift operations, clock gaters are forced on when a test mode or scan enable are asserted. It is worth noting that ATPG can justify the functional enable logic to its off-state, thus preventing many downstream flip-flops from toggling. This can be accomplished by using a relatively small amount of test data provided by scan chains. In other words, during capture, the clock gaters are controlled by scan values loaded through the EDT decompressor. Clearly, the primary objective is to meet the power constraints by disabling flip-flops with as few additional specified bits as possible to minimize impact on compression. Furthermore, many designs may feature a hierarchy of clock gaters. If all flip-flops in a specific area of the design do not capture any fault effects, a higher-level clock gater may be turned off by using fewer specified bits. The method for enhancing ATPG to reduce capture power by controlling clock gaters is described in the next section.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

IV EXPERIMENTAL RESULTS

The proposed low power schemes were tested on several industrial designs. This section reports results for some of them, ranging in size from 470K to 2.8M gates. The basic data regarding the designs, including the number of gates, the scan configuration, and the number of compressed channels are listed in the left part of Table I.

Table I. Circuit characteristics

Design	Gates	Scan chains (no × size)	Channels	EDT switching activity (%)			Peak WSA (%)
				Load WTM	Capture WSA	Unload WTM	
D1	470K	164 × 169	4	49.26	13.89	41.34	23.44
D2	1.3M	203 × 300	4	49.63	19.87	51.92	37.82
D3	2.0M	832 × 158	8	48.90	31.14	38.67	41.44
D4	2.8M	321 × 258	4	49.46	7.25	48.01	13.35

Table II. Clock gater control statistics

Design	Bits/cube	Gated FFs	FFs/bit	%FFs with gated clocks
D2	7.6	942	124	61%
D1	7.6	501	65	70%
D3	15.6	4433	284	91%
D4	5.1	553	107	52%
Average	9.0	1607	145	68%

Clock gater control. The motivation to have ATPG control clock gaters was to prevent a relatively large number of flip-flops from toggling using relatively few specified bits, which is a requirement for embedded compression. Table II quantifies those benefits. Since each CCC may affect multiple clock gaters, the statistics center on the CCCs rather than the individual clock gaters. The second column reports the average number of specified bits per CCC that must be provided by scan. This represents the average encoding capacity cost per CCC. The third column contains the average number of flip-flops whose clocks are shut off by one CCC. This provides the average benefit. The fourth column has the ratio of those two numbers: the average number of flip-flops turned off per specified bit. Finally, the last column contains the percentage of all flip-flops in the design whose clocks may be gated off. Obviously, if this percentage is not high, ATPG will be restricted in how much switching reduction is possible by this method alone. The design trend is towards greater use of clock gating especially for mobile devices or those where thermal dissipation is a concern. The first group of experiments addresses the load scan shift switching when a constant value of zero in conjunction with the decompressor shadow register are used to fill the scan chains. Moreover, a biasing circuitry of Fig. 3 is deployed to help maintaining the amount of scan chains driven by the decompressor at a desired level. Results shown in Table III provide the following information for each test case:

- low-power decompressor method(s) used: constant loading of scan chains (CL) and/or holding the decompressor output constant for multiple cycles (OH),
- the size of the control register,
- the switching rates for scan load, capture, and scan unload modes, respectively; note that reducing load switching has a positive impact on switching activity during capture and unloading of scan chains - this is why these two corresponding figures of merit are included in the table,
- a switching reduction factor, i.e., the ratio of the standard EDT switching (presented earlier, for each design, in Table I) to the low power switching,
- the peak capture cycle switching activity across all test patterns.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

In all experiments, the threshold was set such that when possible, at least 70% of the scan chains will be loaded with constant values. As can be seen, there is a significant reduction in the switching activity during scan loading *and* unloading. In addition, while not explicitly targeted by this method, there is often a reduction in the capture-cycle switching as well.

Table III. Experimental results – filling scan chains with constant values

Design	Method	Ctrl reg.	Low power switching activity (%)						Peak (%)	ΔPC (%)	ΔBCE (%)
			Load	Reduction	Capture	Reduction	Unload	Reduction			
D1	CL	48	15.87	67.78	9.97	28.22	13.67	66.93	22.93	34.47	-0.20
	OH		10.51	78.66	13.10	5.69	15.12	63.43	22.20	-16.45	-0.39
	CL+OH		2.03	95.88	9.57	31.10	5.16	87.52	20.98	30.13	-0.63
D2	CL	64	11.34	77.15	20.05	-0.91	29.14	43.88	27.29	33.46	-0.66
	OH		13.20	73.40	19.04	4.18	25.30	51.27	27.84	-0.17	-0.22
	CL+OH		3.69	92.56	19.92	-0.25	23.71	54.33	27.19	36.38	-0.85
D3	CL	256	11.04	77.42	19.64	36.39	11.95	69.10	32.14	12.03	-0.85
	OH		21.31	56.42	30.24	2.89	24.70	36.13	41.66	-7.15	-0.15
	CL+OH		6.37	86.97	20.11	35.42	9.77	74.73	32.21	4.92	-0.91
D4	CL	96	13.68	72.34	3.92	45.93	14.56	69.67	8.51	20.95	-0.93
	OH		12.63	74.46	7.10	2.07	20.84	56.59	13.28	2.93	-0.43
	CL+OH		3.59	92.74	4.00	44.83	6.89	85.65	9.17	16.32	-1.31

Table IV reports the individual impact of using the clock gater control method on the capture switching activity. The threshold was set such that when possible, no more than 25% of the flip-flops that are driven by clock gaters are allowed to be clocked. The amount of power reduction possible depends on various factors including the percentage of flip-flops that may be gated off, and how many flip-flops can be gated off with limited cost (encoding capacity). For designs like D3, where both criteria are wellsatisfied,significant power reduction is possible even through the design is set up for over 100x compression and therefore has limited encoding capacity. In addition to the reduction in average switching activity, the peak switching is often visibly reduced as well. In some cases, however, even though the average switching is significantly reduced, the peak switching is not because there are a few tests that necessarily generate significant switching activity. Consider for example the stuck-at-0 fault on the global signal that forces all clock gaters on. The pattern count in most cases is close to that of unconstrained ATPG.

Table IV. Experimental results – clock gaters

Design	Switching (%)		Peak (%)	ΔPC (%)	ΔBCE (%)
	Capture	Reduction			
D1	12.72	8.42	22.61	-11.86	-0.13
D2	16.08	19.07	38.00	23.13	-0.04
D3	31.26	57.42	41.54	15.96	-0.28
D4	4.58	36.83	10.15	-7.95	-1.16

Finally, both methods are jointly used in experiments reported in Table V, where the combined impact of both low power scan shifting and constrained capture on toggling rates is summarized. When the methods are combined, it is important not to over-constrain the number of scan chains that may load non-constant values. Such constraints limit how many clock gater control cubes may be merged, which is why for some cases, the capture-cycle power reduction using only the clock gater control method exceeds when clock gater control is combined with the low-power decompressor.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 6, June 2014

Table V. Experimental results – filling scan chains combined with clock gating

Design	Control register	Low power switching activity (%)						Peak (%)	ΔPC (%)	ΔBCE (%)
		Load	Reduction	Capture	Reduction	Unload	Reduction			
D1	48	2.41	95.11	8.73	37.15	5.28	87.23	18.43	38.46	-0.55
D2	64	5.26	89.40	18.67	6.04	21.46	58.67	26.57	37.78	-0.84
D3	256	6.58	86.54	9.31	70.10	8.43	78.20	31.76	38.70	-1.01
D4	96	3.53	92.86	3.53	51.31	6.61	86.23	9.13	29.59	-1.94

V CONCLUSION

In this paper, we propose a comprehensive scan test application scheme encompassing efficient techniques to reduce power dissipation in the continuous flow EDT environment during scan loading, unloading, and capture. Experimental results confirm that for industrial designs, our scheme results in substantial reduction of test power. Switching activity during scan loading and unloading is reduced by up to 96% (24x) and 87% (8x), respectively, using the proposed low-power decompressor. Average switching during capture is reduced by up to 70% using a combination of low-power decompressor and clock gater control. Using only clock-gater control, switching is reduced by up to 57%. The peak capture switching is reduced by up to 32%. Such significant power reductions create a margin that allows accelerating scan shifting which, in turn, effectively decreases test application time. It also enables more of the design to be tested in a given session, enabling a reduction in test time as well. The same methodology allows one to operate within specified power consumption budgets without compromising test quality. Finally, the presented approach fits into the core-based design paradigm, and complements design partitioning schemes for power reduction.

REFERENCES

[1] B. Benware, C. Schuermyer, S. Ranganathan, R. Madge, P.Krishnamurthy, N. Tamarapalli, K.-H. Tsai, and J. Rajski, "Impact of multiple-detect test patterns on product quality,"*Proc. ITC*, pp. 1031-1040, 2003.
[2] S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, andK. Roy, "Low-power scan design using first-level supplygating," *IEEE Trans. VLSI Systems*, vol. 13, pp. 384-395,March 2005.
[3] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S.Pravossoudovitch, "A gated clock scheme for low power scan testing of logic ICs or embedded cores," *Proc. ATS*, pp.253-258, 2001.
[4] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S.Pravossoudovitch, "Efficient scan chain design for power minimization during scan testing under routing constraint,"*Proc. ITC*, pp. 488-493, 2003.
[5] K. M. Butler, J. Saxena, T. Fryars, G. Hetherington, A. Jain,and J. Lewis, "Minimizing power consumption in scan testing: pattern generation and DFT techniques," *Proc. ITC*, pp.355-364, 2004.
[6] A. Chandra and K. Chakrabarty, "Low-power scan testingand test data compression for system-on-a-chip," *IEEE Trans. CAD*, vol. 21, pp. 597-604, May 2002.
[7] A. Chandra and K. Chakrabarty, "A unified approach to reduce SOC test data volume, scan power and testing time,"*IEEE Trans. CAD*, vol. 22, pp. 352-362, March 2003.
[8] M. Chiu and J. C.-M. Li, "Jump scan: a DFT technique forlow power testing," *Proc. VTS*, pp. 277-282, 2005.
[9] K.Y. Cho, S. Mitra, and E.J. McCluskey, "California scan architecture for high quality and low power testing," *Proc.ITC*, paper 25.3, 2007.
[10] R. M. Chou, K. K. Saluja, and V. D.Agrawal, "Schedulingtests of VLSI systems under power constraints," *IEEE Trans. VLSI*, vol. 5, pp. 175-185, June 1997.
[11] D. Czysz, G. Mrugalski, J. Rajski, and J. Tyszer, "New testdata decompressor for low power applications," *Proc. DAC*, pp. 539-544, 2007.
[12] V.P. Dabholkar, S. Chakravarty, I. Pomeranz, and S.M.Reddy, "Techniques for minimizing power dissipation in scan and combinational circuits during test application,"*IEEE Trans. CAD*, vol. 17, pp. 1325-1333, Dec. 1998.
[13] M. ElShoukry, C.P. Ravikumar, and M. Tehranipoor, "Partialgating optimization for power reduction during test application,"*Proc. ATS*, pp. 242-247, 2005.
[14] S. Gerstendorfen and H.-J.Wunderlich, "Minimized power consumption for scan-based BIST," *Proc. ITC*, pp. 77-84,1999.
[15] P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel,and H.-J.Wunderlich, "High defect coverage with low power test sequences in a BIST environment," *IEEE Design& Test of Computers*, vol. 19, pp. 44-52, Sept.-Oct. 2002.