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Design of FIR Filter Using SMB Recoding Technique

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ABSTRACT: Digital finite impulse response filters has a lot of arithmetic operation. Arithmetic operation modules such as adder and multiplier modules consume much power, energy and area in general. In order to reduce the area, delay and power consumption the multiplier module in FIR (finite impulse response filter) architecture is replaced by SMB (sum to modified booth) re-coder. . SMB performs direct recoding of sum of two numbers in its modified booth form. Modified booth is a prevalent form used in multiplication; it reduces the number of partial products into half. The proposed design for FIR filters have been designed using Verilog HDL and synthesized, implemented using Xilinx ISE and Modelsim.

KEYWORDS: Finite Impulse Response Filter; Modified Booth Recoding Technique; Partial Product; Sum to Modified Booth Re-Coder;

I. INTRODUCTION

Digital signal processing (DSP) is the mathematical manipulation of an information signal to modify or improve it in some way. The goal of DSP is usually to measure, filter and/or compress continuous real-world analog signals. Usually, the first step is conversion of the signal from an analog to a digital form, by sampling and then digitizing it using an analog-to-digital converter (ADC), which turns the analog signal into a stream of discrete digital values. Often, however, the required output signal is also analog, which requires a digital-to-analog converter (DAC). Modern consumer electronics make extensive use of Digital Signal Processing (DSP) providing custom accelerators for the domains of multimedia, communications etc. Typical DSP applications carry out a large number of arithmetic operations as their implementation is based on computationally intensive kernels, such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Finite Impulse Response (FIR) filters and signals' convolution. Finite impulse response (FIR) filters are widely used in various DSP applications. Nowadays, many finite impulse response (FIR) filter designs aimed at either low area-cost or high speed or reduced power consumption are developed. Multipliers consume the most amount of area in a FIR filter design. Product of two numbers has twice the original bit width of the multiplied numbers. We can truncate the product bits to the required precision to reduce the area cost. Here conventional multipliers are replaced by sum to modified booth re-coders (SMB) which produces only half the number of partial products (PPs) when compared with an ordinary binary multiplication.

II. RELATED WORK

In paper [1], Alexandru Amaricai et.al has presented a dedicated unit for the combined operation of floating point division fallowed by addition/subtraction called divide-add fused unit (DAF). The main issue regarding DAF is represented by the number of required quotient bits. Hence our analysis targets the optimum number of bits, for this purpose they introduced two units one favours accuracy and other favours performance namely pro-accuracy DAF and pro-performance DAF. In paper [12], C.Yeh et.al has presented a approach to data path synthesis from RTL, data paths are extracted into largest possible sum-of -products(SOP)blocks, thus making extensive use of carry-save intermediate results and reducing the number of expensive carry-propagations to a minimum. In paper [23], M. Daumas et.al designed a circuit which does not lengthen the time of one multiplication compared to the state-of-art encoding, if both

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the inputs are non redundant. Past re-coders have added critical path delay for the more frequent case where both inputs are non redundant. So the author has slightly modified an existing cell to accept a redundant binary number in place of the non redundant number by changing some connections.

III. PROPOSED METHOD

1.1 FIR Filter Design

Generally, FIR filter can be expressed as

$$Y[n] = \sum_{i=0}^{M-1} (a_i . x[n-1])$$

Where *M* represents the filter order, *y [n]* is the output signal and a_i represents the set of filter coefficients. If *x [n]* is the input signal applied, *x [n - i]* terms are referred as taps or tapped delay lines. Symmetric or anti-symmetric coefficients can be considered for a linear phase FIR filter. The implementation of a FIR filter requires three basic building blocks – multiplication, addition, and signal delay.

Design of FIR filter consists of four stages:

i. Choose a suitable filter order
ii. Find the coefficients for the corresponding filter order
iii. Realize the filter using a suitable structure
iv. Optimize the area of the realized filter to the maximum extend

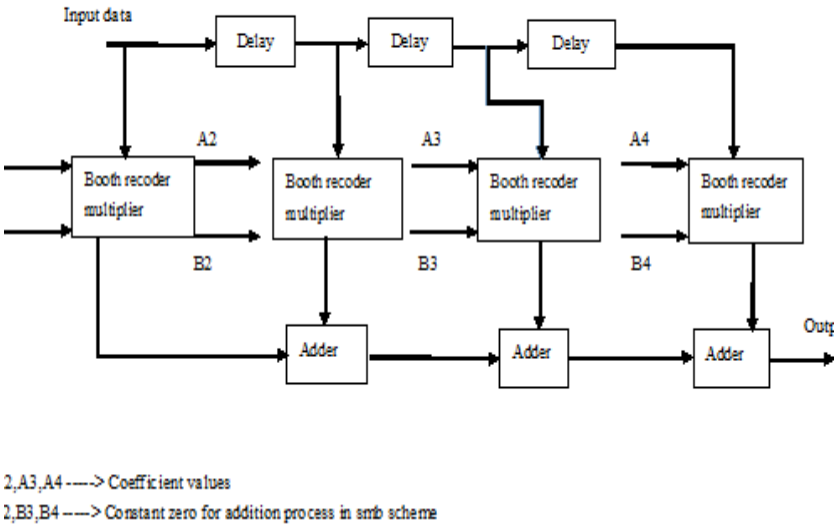

Fig1.proposed FIR filter

A system's performance is determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Here the multiplier module is replaced by sum to modified booth re-coder. The SMB re-coder saves the area and it is much faster than the conventional multipliers. The new proposed low area, low power-FIR filter is shown in the Fig.1

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1.5 Modified Booth Form

Let us consider the multiplication of 2's complement numbers X and Y with each number consisting of n = 2k bits. The multiplicand Y can be represented in MB form as:

$$Y = \langle y_{n-1}y_{n-2}.....y_1y_0\rangle_{2's} = -y_{2k-1} + \sum_{i=0}^{2k-2} y_i.2^i$$

$$\langle y_{k-1}y_{k-2}\ldots y_1y_0\rangle_{MB} = \sum_{J=0}^{K-1} y_j^{MB.}\, 2^{2j} \quad (1)$$

$$y_j^{MB} = y_{2j+1} + y_{2j} + y_{2j-1}$$

Digits y_j^{MB} ε {-2, -1, 0, +1, +2}, $0 \leq j \leq k-1$, correspond to the three consecutive bits y_{2j+1}, y_{2j} and y_{2j-1} with one bit overlapped and considering that $y_{-1} = 0$. Each digit is represented by three bits named s, *one* and *two*. The sign bit shows if the digit is negative (s = 1) or positive (s = 0). Signal *one* shows if the absolute value of a digit is equal to 1 (one = 1) or not (one = 0). Signal *two* shows if the absolute value of a digit is equal to 2 (two = 1) or not (two = 0). Using these three bits calculates the MB digits y_j^{MB} by the following relation:

$$y_j^{MB} = (-1)^s * [one_j + 2 * two_j]. \quad (2)$$

1.8 SMB-1 RECODING SCHEME

The first scheme of the proposed recoding technique is referred as *S-MB*1 and is illustrated in detail in Fig.4 for both even and odd bit-width of input numbers. As can be seen in Fig.4, the sum of A and B is given by the next relation:

$$Y = A+B = y_k \cdot 2^{2k} + \sum_{j=0}^{k-1} y_j^{MB} \cdot 2^{2j} \quad (4)$$

Where $y_j^{MB} = -2s_{2j+1} + s_{2j} + c_{2.j.}$ The encoding of the MB digits y_j^{MB} , $0 \leq j \leq k-1$. Bits s_{2j+1} and s_{2j} are extracted from the j recoding cell of Fig.4. A conventional FA with inputs a_{2j}, b_{2j} and b_{2j-1} produces the carry $c_{2j+1} = (a_{2j} \Lambda b_{2j}) V (b_{2j-1} \Lambda (a_{2j} V b_{2j}))$ and the sum $s_{2j} = a_{2j} \oplus b_{2j} \oplus b_{2j-1}$. As the bit s_{2j+1} need to be negatively signed, use a FA* with inputs a_{2j+1}, b_{2j+1} (-) and c_{2j+1}, which produces the carry c_{2j+2} and the sum s_{2j+1} (-):

$$C_{2j+2} = (a_{2j+1} \wedge \bar{b}_{2j+1}) \text{ v } (c_{2j+1} \wedge (a_{2j+1} \text{v} \bar{b}_{2j+1})) \quad (5)$$

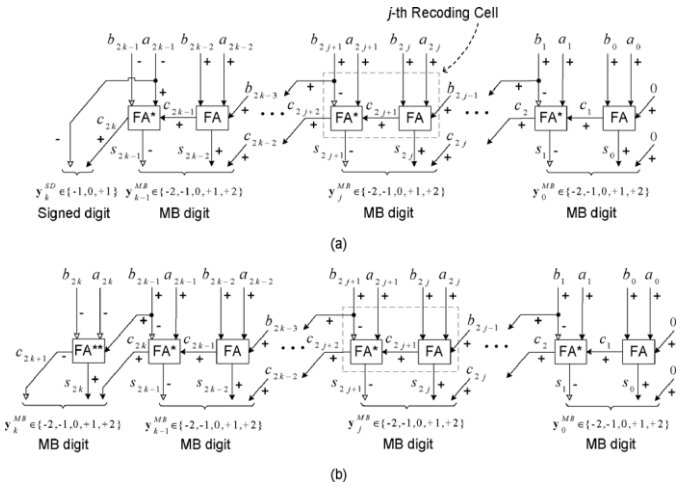

Fig.3*S-MB*1 recoding scheme for (a) even and (b) odd number of bits

Note that, based on equation $b_{2j+1} = 2 * b_{2j+1} - b_{2j+1}$, b_{2j+1} is driven to the FA* as negatively signed while it is also used with positive sign as an input carry of the subsequent recoding cell. It consider the initial values $b_{-1} = 0$ and $c_0 = 0$. When its form the most significant digit (MSD) of the *S-MB*1 recoding scheme, it distinguish two cases: In the first

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case, the bit-width of A and B is even, while in the second case, both A and B comprise of odd number of bits. In the first case, the MSD $y_{k,even}^{SD}$ is a signed digit and is given by the next algebraic equation:

$$y_{k,even}^{SD} = -a_{2k-1} + c_{2k} \qquad (6)$$

The critical path delay of *S-MB*1 recoding scheme is constant in respect to the input bit-width and is given by the equation:

$$T_{S\text{-}MB1} = T_{FA,carry} + T_{FA^*,sum} \qquad (7)$$

1.9 SMB recoding scheme

The second approach of the proposed recoding technique, S-MB2, is described in Fig.5 for even and odd bit-width of input numbers. It consider the initial values $c_{0,1} = 0$ and $c_{0,2} = 0$. The digits y_j^{MB} , $0 \le j \le k-1$, are formed based on s_{2j+1}, s_{2j} and $c_{2j,2}$. As in the S-MB1 recoding scheme, it uses a conventional FA to produce the carry c_{2j+1} and the sum s_{2j}. The inputs of the FA are a_{2j}, b_{2j} and $c_{2j,1}$. The bit $c_{2j,1}$ is the output carry of a conventional HA which is part of the (j-1) recoding cell and has the bits a_{2j-1}, b_{2j-1} as inputs. The bit s_{2j+1} is the output sum of a HA* in which it drives c_{2j+1} and the sum produced by a conventional HA with the bits a_{2j+1}, b_{2j+1} as inputs. The HA* is used in order to produce the negatively signed sum s_{2j+1} and its outputs are given by the following Boolean equations:

$$c_{2j+2,2} = c_{2j+1} \, V \, (a_{2j+1} \oplus b_{2j+1}) \qquad (8)$$

$$s_{2j+1} = a_{2j+1} \oplus b_{2j+1} \oplus c_{2j+1}$$

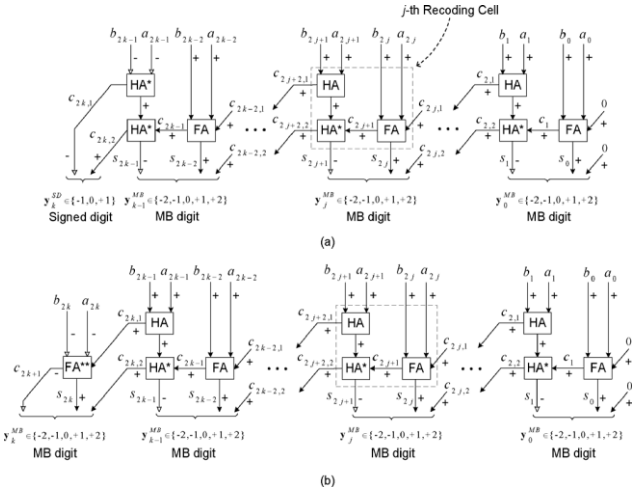

Fig.4 *S-MB*2 recoding scheme for (a) even and (b) odd number of bits

In case that A and B comprise of even number of bits, a_{2n-1} and b_{2n-1} are negatively weighted and the conventional HA of the (n-1) recoding cell is replaced by the dual HA* The MSD $y_{k,even}^{SD}$ is a signed digit and is given by the relation:

$$y_{k,even}^{SD} = -c_{2k,1} + c_{2k,2} \qquad (9)$$

2. SMB 3 recoding scheme

The third scheme implementing the proposed recoding technique is *S-MB*3. It is illustrated in detail in for even and odd bit-width of input numbers. It consider that $c_{0,1} = 0$ and $c_{0,2}$. It builds the digits y_j^{MB} , $0 \le j \le k-1$, based on s_{2j+1}, s_{2j} and $c_{2j,2}$. Once more, it uses a conventional FA to produce the carry c_{2j+1} and the sum s_{2j}. The bit $c_{2j,1}$ is now the output carry of a HA* which belongs to the (j-1) recoding cell and has the bits a_{2j-1}, b_{2j-1} as inputs. The negatively signed bit s_{2j+1} is produced by a HA** in which drive c_{2j+1} and the output sum (negatively signed) of the HA* of the recoding cell with the bits a_{2j+1}, b_{2j+1} as inputs. The carry and sum outputs of the HA** are given by the following Boolean equations:

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$$c_{2j+2,2} = c_{2j+1} \wedge (\overline{a_{2j+1} \oplus b_{2j+1}})$$
$$s_{2j+1} = a_{2j+1} \oplus b_{2j+1} \oplus c_{2j+1}. \qquad (15)$$

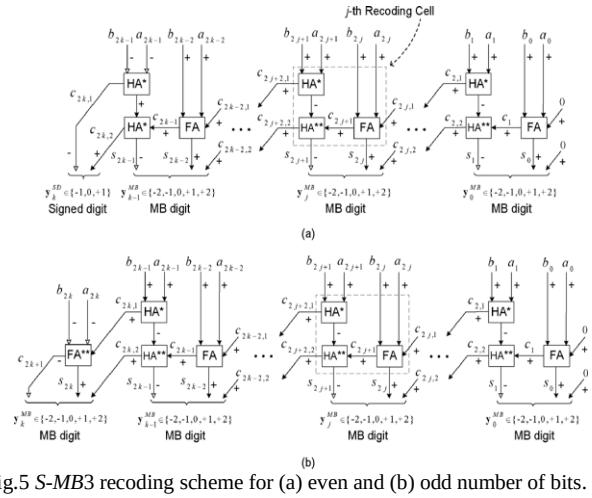

Fig.5 *S-MB*3 recoding scheme for (a) even and (b) odd number of bits.

IV. SIMULATION RESULTS

RESULTS FOR SIGNED INPUTS

By implementing the SMB recoding technique in FIR filter the fallowing area, delay and power consumption are achieved. The SMB technique is suitable for both signed and unsigned digits, hence the results are achieved for both signed and unsigned digits and the technique is applied for both odd and even number of bits. By comparing the results fallowing table is made.

SMB-1	**ODD**	**EVEN**
Gate count	3,054	3,492
Delay	41.724ns	40.515ns
Power consumption	155	146

SMB-2	**ODD**	**EVEN**
Gate count	3,054	3,492
Delay	41.724ns	46.214ns
Power consumption	155	151

SMB-3	**ODD**	**EVEN**
Gate count	3270	3,630
Delay	42.845ns	45.402ns
Power consumption	154	151

The above three tables shows the comparison of area, delay and power for signed digits in case of odd and even using SMB recoding technique.

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Vol. 3, Issue 4, April 2015

RESULTS FOR UNSIGNED INPUTS

SMB-1	ODD	EVEN
Gate count	3054	3492
Delay	41.724ns	46.214ns
Power consumption	155	151

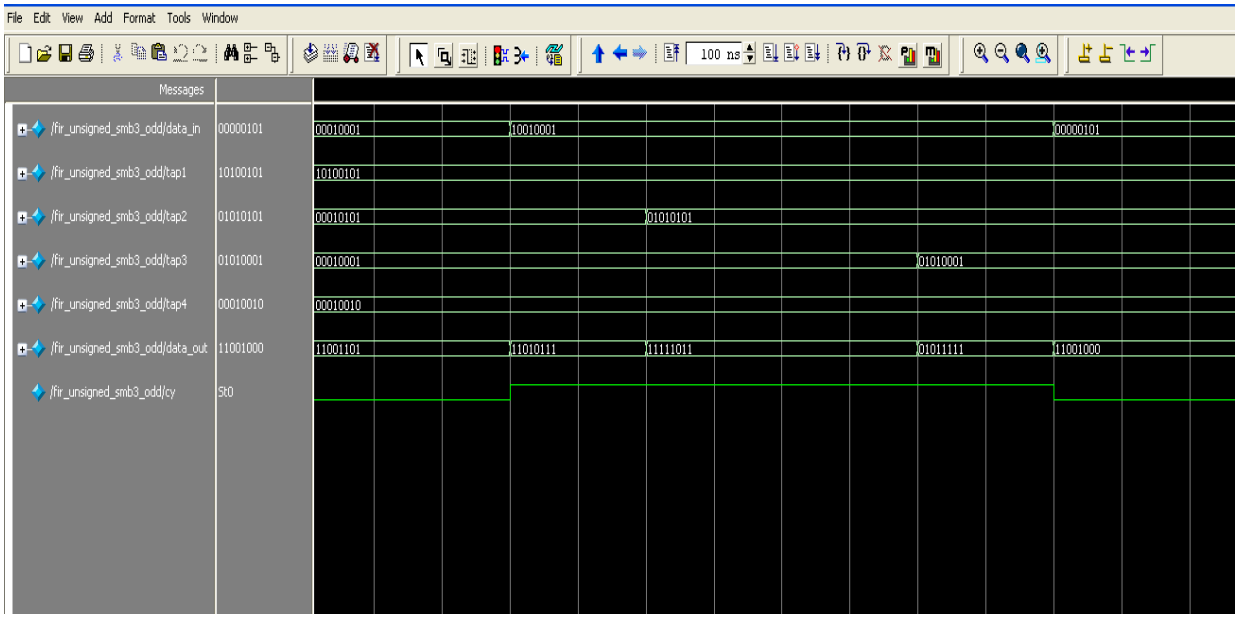
SMB-2	ODD	EVEN
Gate count	3054	3492
Delay	41.724ns	46.214ns
Power consumption	155	151

SMB-3	ODD	EVEN
Gate count	3270	3630
Delay	42.758ns	40.503ns
Power consumption	154	151

The above three tables describe the area, delay and power consumption of digits using SMB recoding technique.

OUTPUT WAVEFORM

The output waveform for the FIR filters using three SMB recoding schemes are shown below. This the output waveform for FIR filter with unsigned digits are shown here, similarly the waveform for signed digits also can be obtained.



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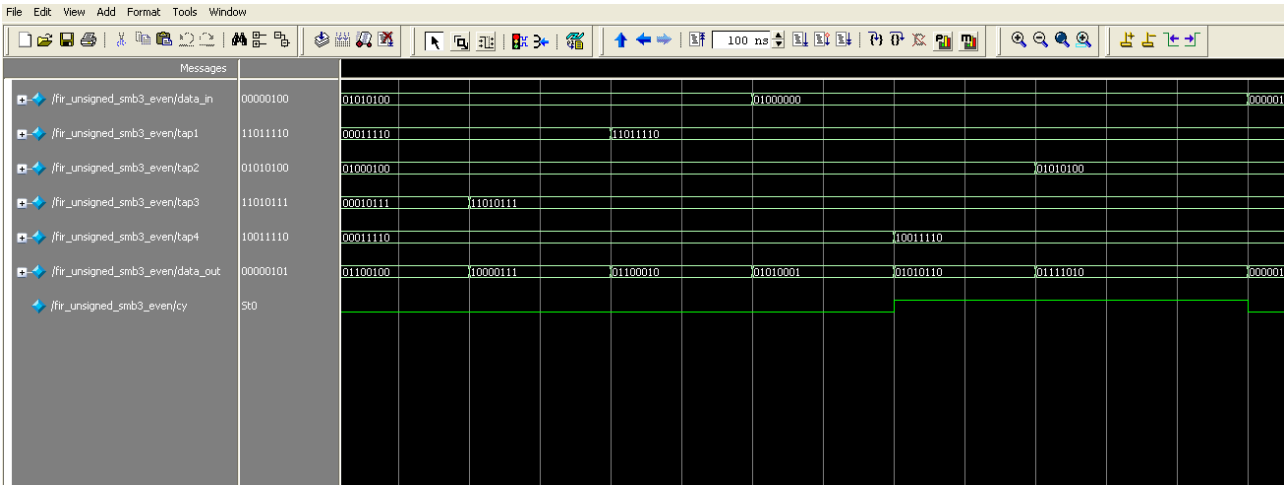

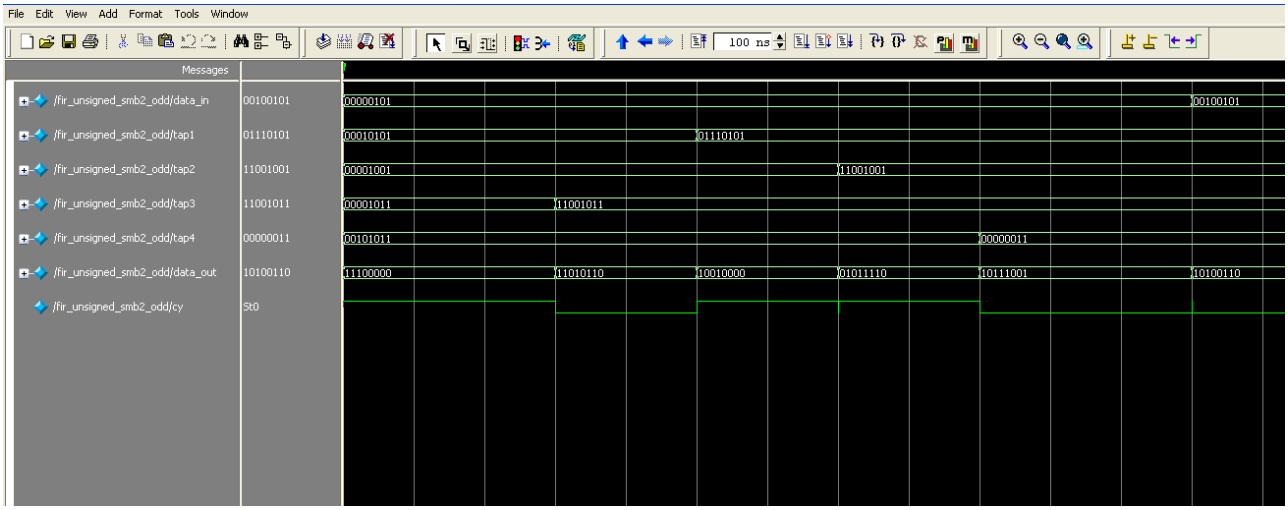

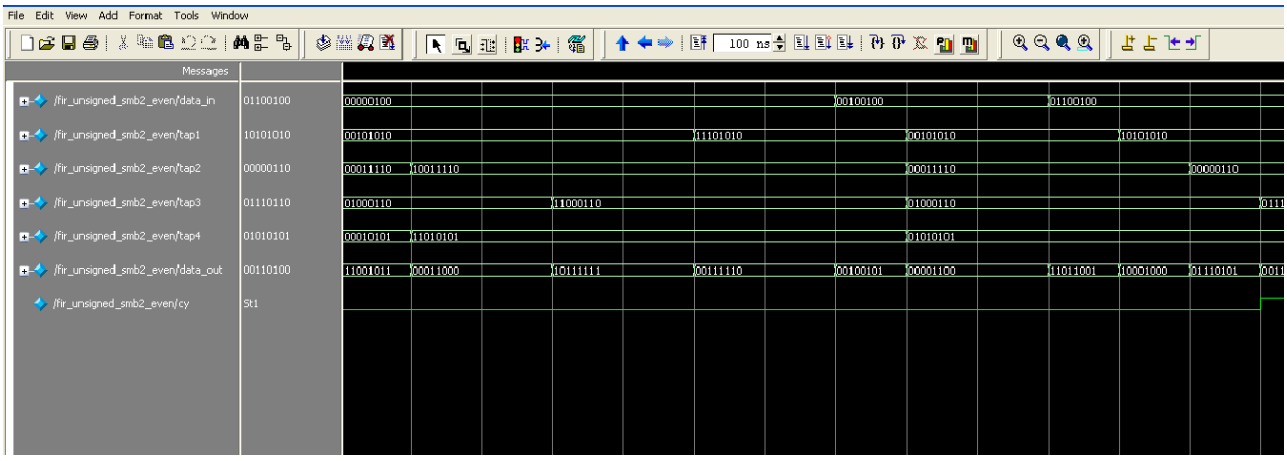

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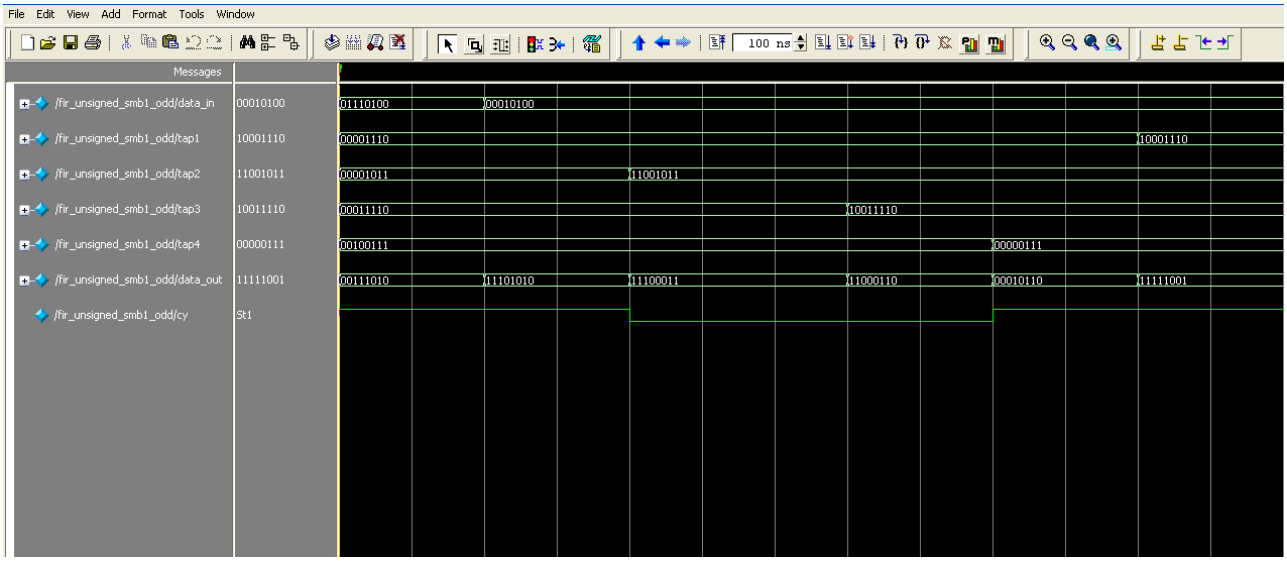

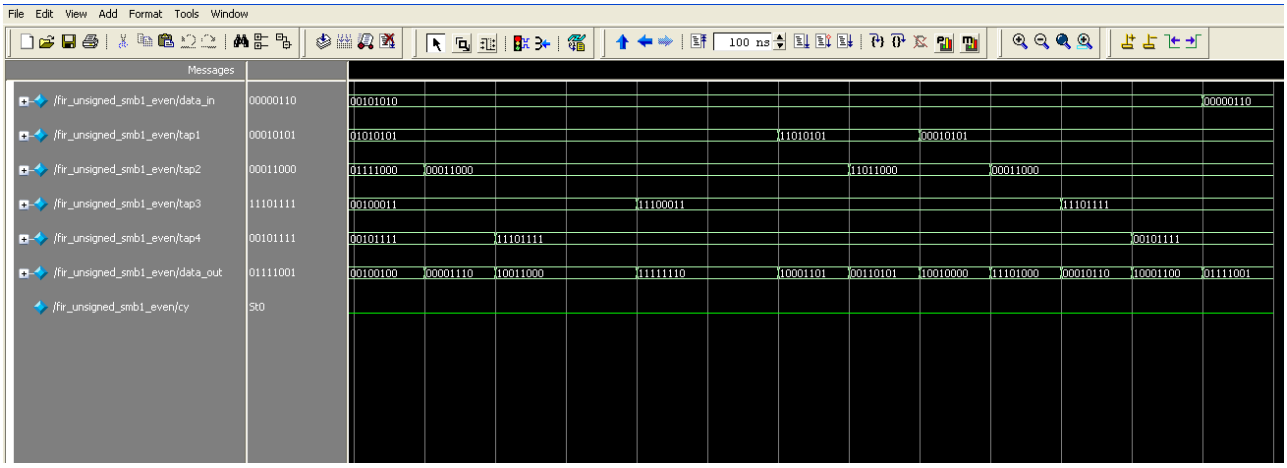

V. CONCLUSION AND FUTURE WORK

In this paper, it presents a Modelsim simulated results of finite impulse response (FIR) filter using S-MB recoding technique. Our design consists of three schemes, S-MB 1 recoding technique, S-MB 2 recoding technique and S-MB 3 recoding technique. The area, power consumption and timing complexity are analyzed for FIR using Xilinx. The S-MB techniques are applied for both signed and unsigned bits and it has two cases namely, S-MB technique in case of odd and S-MB technique in case of even. For both the cases the area complexity, power consumption and timing complexity is analyzed and compared with existing recoding techniques.

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BIOGRAPHY

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