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A Study of VHDL Implementation of Fast Sobel Edge Detection Algorithm

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ABSTRACT: The VHDL is an Hardware Description Language (HDL) for providing hardware based model of image processing algorithms. In this paper the aim is to present study of hardware model of Sobel edge detection algorithm for implementing on FPGA chips. The presented architecture provides the detection of edges of images . The Praposed design is based on Simulation and synthesizing of Sobel edge detection processor on Xilinx Spartan3 FPGA chip.

KEYWORDS: Hardware Description, Edge Detection, Sobel Algorithm, VHDL, FPGA.

I. INTRODUCTION

Hardware implementation is one of the most challenging issues in edge detection approaches for image processing in real time applications like image pattern recognition, segmentation and texture analysis. The task processing clock speed is a key designing parameter for hardware implementation of edge detection algorithms which also depends on the type of algorithms and its compatibility for hardware implementation. There are many algorithms were introduced for different pattern of image processing applications but due to their nature complexity and long processing time are not considered for hardware implementation. Normally, general simple and efficient algorithms are considered for real-time and fast hardware implementing [1].

II. RELATED WORK

In [2][7][8] there are some well-known methods for edge detection such as Prewitt, Canny, Sobel, and Roberts algorithms which are different in terms of performance on hardware, speed and simplicity. The Sobel operator is mainly used for hardware implementing due to efficiency and simple mathematical model that make it easy for real-time edge detection applications. In [10][12] described about edge detection technique using Sobel operator to achieve higher accuracy to detect as much as possible edges. In [11] author implemented edge detection method into FPGA and its performance analysis. VHDL and Verilog two hardware description languages are there to implement designs on FPGA

III. METHODOLOGY

The FPGA technology has been getting much attention by electronic engineers for implementing image processing applications. In [5] a new technique for face detection and in face there is lip feature extraction was proposed and implemented on field programmable gate array. The Design and implementation of a video based image edge detection system based on FPGA was presented in [6]. Now an improved canny edge detector and its real time realization on FPGA was presented in [7]. BAsic Implementation of FPGA based architecture of Prewitt edge detection algorithm using Verilog HDL was proposed in [8]. Simple Image edge detection based on FPGA was described in [9]. A novel FPGA-based architecture for Sobel edge detection operator was presented in [10].And also performance analysis of FPGA based Sobel edge detection operator was described in [11].

In this paper a real time FPGA based hardware architecture for implementing a real-time system for simple image edge detection based on Sobel operator used. In this proposed architecture, the edges of any images are detected

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separately in four directions; right, left, left diagonal and right diagonal. And, in two cases, one of the algorithm outputs is the resultant of horizontal and vertical directions and other is the resultant of left diagonal and right diagonal directions. All These outputs could be used depends on the application purpose.

Real-time image processing in digital electronics is used in different applications such as surveillance, city traffic management and some medical image processing. In These operations frequently require digital signal processing (DSP) algorithms for numerous vital operations [2]. Generally The processing of two dimensional images via computer is called as Digital Image Processing. Quantization and sampling is used to obtain a digital image from real image. In this method process of locating edges of an image is called as Edge detection. Detection of edge of an image is a very significant step for understanding features of images. The edges consist of noteworthy features and contained important information. They reduce the size of the digital image and filters out information that is treated as less relevant, preserving the important properties of an digital image [4]. So this edge detection proposal can be used in image processing field for motion detection and object tracking.

IV. HARDWARE ARCHITECTURE

This section presents the basic hardware ASIC architecture model for implementing real-time edge detection on FPGA based chips considering Sobel algorithm. In This proposed architecture is for gray scale images where each pixel is represented by 8 bits providing 1 byte of data. So, the intensity range changes from 0 to 255. The proposed architecture is shown in Figure 1 which consists of several operational blocks given below.

1. Array Generator
2. Window Processor
3. Comparator
4. RAM
5. Controller
6. Counter

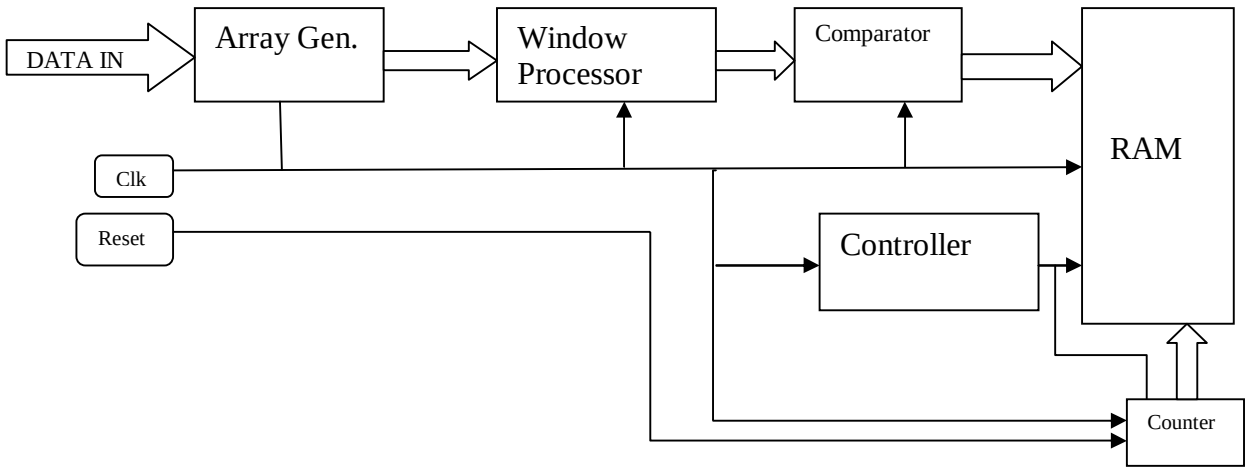

FIG 1: THE PROPOSED HARDWARE ARCHITECTURE OF IMPLEMENTING SOBEL ALGORITHM

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V. SIMULATION

Based on above hardware architecture the model for Image detection can be design for sobel oberator on Xilinx ISE Navigator tool and using VHDL hardware description language and design can be simulate using model sim simulator. Basically this proposed architecture based for FPGA implementation of sobel image detection algorithm.

VI. CONCLUSION

Hardware description of a real-time edge detection system based on FPGA considered of high-speed processing in image edge detection. A hardware model of Sobel edge detection algorithm for implementation on field programmable gate array (FPGA) was proposed. This proposed hardware based architecture computes the edges of gray scale images in four directions like horizontal, vertical, right diagonal and left diagonal. The Simulation results and synthesizing proposed Sobel edge detection processor on FPGA hardware Xilinx Spartan3 XC3S100 FPGA chip demonstrated the efficiency of proposed architecture for edge detecting of gray scale.

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