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A Literature Review on High Speed, Less Area 64 Bit ALU using Efficient Techniques

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ABSTRACT: In this paper, Authors have presented the literature on designing of high speed, less area 64-bit ALU using efficient techniques. The optimization of the proposed design will be done by using the different techniques. The parameters speed and area of the proposed design will be improved by using Carry Look Ahead Techniques. It also reduces the circuit complexity. The ALU is a fundamental building block of central processing unit of a computer which is used in the simplest microprocessors for purpose of maintaining timers. Previously, many efficient architecture have been introduced for the design of low complexity operation, but we have given the attention to the carry look ahead and reversible logic gate techniques. The proposed design of ALU will performs the mathematical, logical, and shifting operations like Addition, Subtraction, Multiplication, Increment, Decrement, Logical AND, Logical OR, Logical XOR etc. in the computer. In this paper, the efficient modules of ALU will be design using Xilinx software and simulation results will be verified on same platform using test benches.

KEYWORD: ALU, VHDL, EDVAC, DSP, CLA

I. INTRODUCTION

ALU is an essential part of processor. It plays vital role in performing arithmetical and logical operations on data. All rest of the elements of computer system such as control unit, register, memory, I/O are mainly responsible to bring data into the ALU for process and then to take results back out.ALU is a combinational type of circuit, which is able to perform entire register transfer operation from the source register through ALU and into the destination register during 1 clock pulse period. It is a basic building block of any microprocessor along with DSP processor that accomplish many arithmetic function grounded upon the control input selection. ALU is the heart of any microprocessor system.ALU bring about basic arithmetic function such as addition, subtraction and logical functions including logical AND, logical OR, logical XOR etc. These different functions of ALU are collocates with the help of set of fundamental units.

Now a days, increasing demands of gadgets like laptop, tablets, PCs forcing technologies to develop high speed processor. The speed of any processor is mainly depending upon computational time needs to finish the task in ALU. Adder and multiplier is main fundamental block inside ALU on which speed is depended. The system can be made chipper, more efficient and more flexible by reducing the number of core components like adder and multiplier in the circuitry.

The ALU takes as input the data to be operated i.e. operands and a code from the control unit indicating which operation to be performed. The output is the result of the computation which we are realizing.

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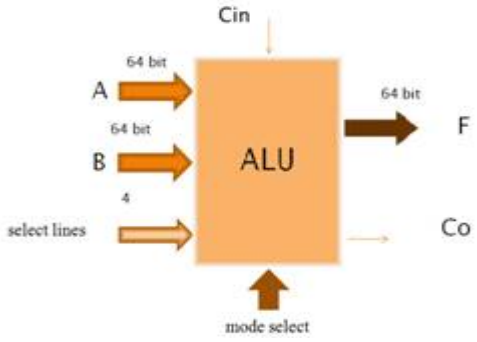

Fig 1. Block Schematic of 64 bit ALU

VHDL is a very powerful language for the programming as well as for design purpose and at the same time it is easy to inculcate along with full of Mysteries. Its benefit is that VHDL allows the description of a concurrent system. VHDL project is multipurpose and portable. The VHDL software interface used in this design reduces the complexity and also provides a graphic presentation of the system. The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described and verified before synthesis tools translates the design into real hardware (gates and wires). This software not only compiles the given VHDL code but also generates waveform results.

Existing Work on Efficient ALU Module

A new algorithm based design technique is suggested by Suchita Kamble, Prof. N.N. Mhala focused on the design for 8 bit ALU and it was implemented using VHDL Xilinx Synthesis tool ISE 13.1. ALU was designed to perform arithmetic operations and logical operation. The maximum propagation delay is 13.588ns and power dissipation is 38mW. They have implemented lower number of bit i.e. 8- bit [1].

A novel algorithm to design and implementation of low power 16-bit ALU with clock gating is presented by Ankit Mitra. Authors has include the power optimization at architectural level which demonstrated by the design of a 16- bit ALU using clock gating. The arithmetic unit of the ALU is based on a carry skip adder to reduce carry propagation delays. It is observed that clock gating reduces dynamic power dissipation of the ALU approximately [2].

Geetanjali, Nishant Tripathi introduced the VHDL implementation of 32-bit ALU. They suggest the behavioral design method for VHDL implementation of a 32-bit ALU using Modelsim 5.4a tool. Its functionality was discussed for all the operations specified. As per the nature of behavioral description, it is easy to convert the precision to 64- bit or more. But, this paper has some limitations regarding the improvement in the various parameters [3].

P Bhanusree,G Bhargav Sai,Y Ashwanth Kumar,K Sravan Kumar have designed VHDL implementation of 64-bit ALU. They introduced the behavioral modeling and structural modeling used for the implementation of 64-bit ALU. All the mathematical operations in the ALU are performed by means of repeated additions. Along with the basic operations of ALU multiplication and comparison are incorporated and designed as a single unit. The module is designed and implemented using VHDL and is simulated using Xilinx9.2i ISE[4].

Performance Analysis of High Speed Low Power Carry Look-Ahead Adder Using Different Logic style is presented by the Jagannath Samanta, Mousam Halder, Bishnu Prasad De. Comparative performance analysis of different static and dynamic CLA has been carried out by this work. They have shown different graphs which indicate performance of the CLA by the variation the channel length. According to Authors, this work will be helpful for designer to implement any type of digital VLSI adder circuits.

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Performance Analysis of 64-Bit Carry Look Ahead Adder has been focused by Daljit Kaur, Ana Monga. They have designed and shown Simulation results for 32 bit and 64 bit carry look ahead adder. Results are depicted for the performance parameters delay and chip area which has been slightly improved.

II. METHODOLOGY

It provides a efficient way for high speed, less area 64 bit ALU at the architectural level. The basic ALU consist of full adder techniques which uses more numbers of adders as well as gates results into increased delay and due to this there is occupation of more area which ultimately increasing the power dissipation. To make our system efficient, we have to use the technique which consists of relatively less number of adders which minimizes the delay and the occupied area is also less. Hence, the system becomes more faster than the basic one and the power dissipation will also get reduced. The following diagram depicts the block diagram of ALU:

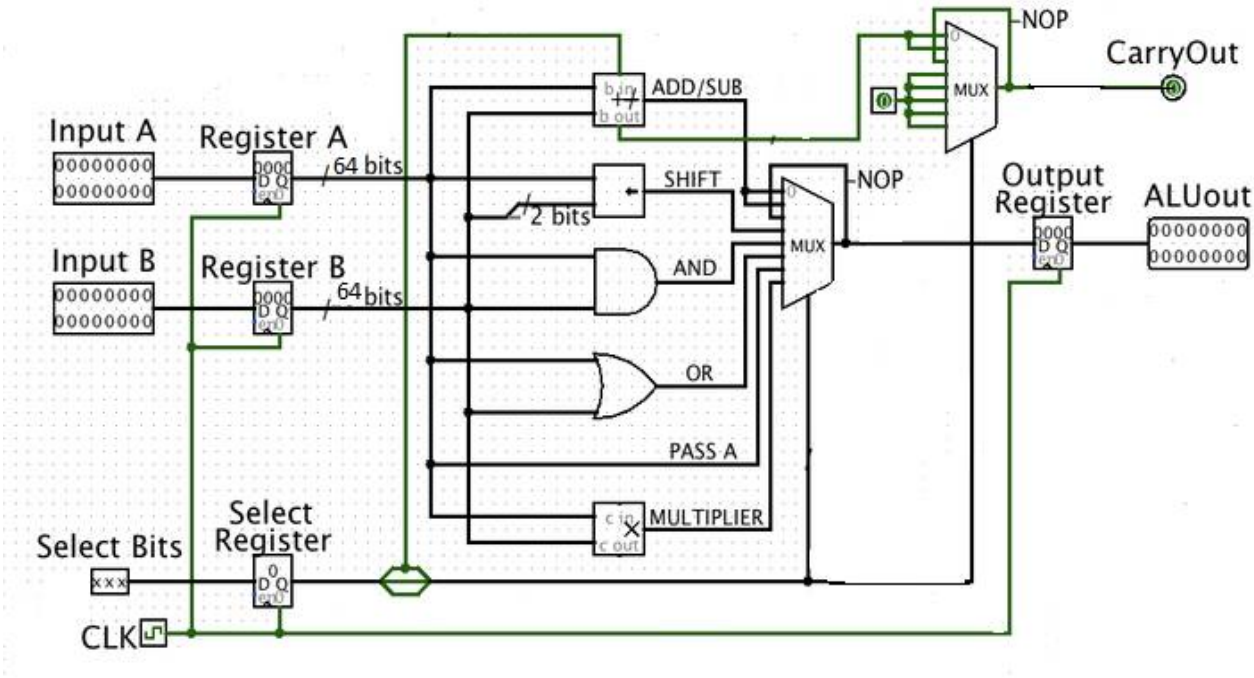

Fig 2. ALU Block Diagram

Delay is calculated by the following equation

$$\text{Delay} = \frac{\text{Constant} * C * Vdd}{W * (Vdd - Vt)^2}$$

The requirement of adders is minimized, results into the minimization of gates. Hence, the system will occupy less area. The following flow chart depicts the steps of architectural design flow:

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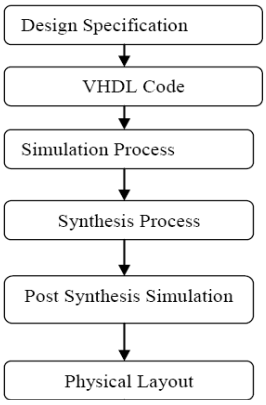

Fig 3. VHDL design flow

Authors are designing the efficient module of 64 bit ALU by using the efficient techniques like carry look ahead adder and reversible gate array to improve the essential parameters. These techniques help us in improving the system performance by minimizing the delay. Nowadays, Reversible gates are getting more importance due to its less heat dissipation. Also, it is prove that almost every Boolean function can be implemented using reversible logic gates. Every combinational circuit of basic reversible logic gates can be verified through simulations and the test benches.

The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.

Carry look ahead depends on two things, first is Calculation for each digit position whether that position is going to propagate a carry if one comes in from the right. Second is combining these calculated values to be able to deduce quickly for each group of digits, that group is going to propagate a carry that comes from the right.

Mode Select S3	S2	S1	S0	Cin	Result	Operation
0	0	0	0	0	A+B	Addition
0	0	0	0	1	A+B+1	Addition with carry
0	0	0	1	0	A-B	Subtraction
0	0	0	1	1	A+B+1	Subtraction with borrow
0	0	1	0	0	A+1	Increment
0	0	1	0	1	A-1	Decrement
0	0	1	1	0	A/2	Right Shift
0	0	1	1	1	A*2	Left Shift
0	1	0	0	0	NOT A	Compliment
1	1	0	0	1	A.B	AND
1	1	0	1	0	A+B	OR

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1	1	0	1	1	A XOR B	EX-OR
1	1	1	0	0	A XNOR B	EX-NOR
1	1	1	0	1	A NAND B	NAND
1	1	1	1	0	A NOR B	NOR
1	1	1	1	1	2's Compliment of A	2's Compliment

Table : Various operations controlled by select lines

III. CONCLUSION

The efficient module of the ALU has been discussed. After thoroughly studying these literatures we have conclude that the techniques which acquired are much more effective to improve the parameters of designed module of 64-bit ALU. These help in optimizing the system by using efficient techniques. The ALU design using carry look ahead and reversible logic gate approach increases the speed to a great extent but it increases the hardware complexity. The proposed methodology provides a systematic way to derive high speed system at a very less area. We have proposed the model of 32 bit and 64 bit ALU with efficient design approach using less area, high speed methodology. Also, Author efforts will be directed towards implementation of 64 bit ALU design with different circuit topology and optimization.

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BIOGRAPHY

Rajendra M. Rewatkar received his B.E. in Electronics Engineering, completed his M. Tech. in Electronics Engineering and submitted his Ph.D. from R. T. M. Nagpur University, Nagpur, India. He is an Academician, since last 19 years and presently associated with Datta Meghe Institute of Engineering, Technology and Research, Sawangi (Meghe), Wardha as an Assistant Professor. He has 17 publications to his credit in International Journals. He is a Life Member of ISTE and Institute of Engineers.