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Design of High Speed Vedic Multiplier Using K-Map Boolean Function Techniques

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ABSTRACT: This work propose the design of high speed vedic multiplier using the k-map techniques of ancient vedic mathematics that have been modified to improve performance.Vedic multiplier is the ancient system of logic table which has a unique technique of calculations based on truth table.The work has proved the efficiency of vedic method for multiplication which strikes a difference in the actual process of multiplication itself.It enables parallel generation of intermediate products,eliminates unwanted multiplication steps with zeros and scaled to higher bit levels using algorithm with the compatibility to different datatypes.It is most efficient technique giving minimum delay for multiplication of all types of numbers ,either small or large.Further the verilog HDL coding for 32x32 bits multiplication and implementation have been done and output has been displayed.

KEYWORDS: K Map, Boolean Expression, Array, DSP.

I. INTRODUCTION

The use of laws of Boolean algebra is one way of minimizing a Boolean logic function. Since minimization with the use of Boolean laws is neither a systematic approach nor suitable for computer implementation. A K-map intends to allow minimal Sum-of Products and Product-of-Sums. This is attributed to the fact that the formulae are claimed to be based on the "natural principles on which the human mind works". Hence this presents some effective algorithms which can be applied to various branches of engineering. The architecture of Multipliers can be generally classified into three categories. First is the "serial multiplier" which emphasizes on hardware optimization of chip area. Second is "parallel multiplier" which performs high speed mathematical operations, the drawback being relatively larger chip area consumption. The final one is "serial-parallel multiplier" which is a trade-off between time consuming serial multipliers and the area consuming parallel multipliers.

Vedic mathematics is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved – be it arithmetic, algebra, geometry or trigonometry. The system is based, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. A multiplier is one of the key hardware blocks in most digital signal processing systems. With advances in technology, many researchers have tried to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. The Vedic mathematics approach is totally different and considered very close to the way a human mind works. In this work, we try to present multiplication operations and the implementation of these using both conventional, as well as Vedic mathematical methods in VHDL language [1]. We highlight a comparative study of both approaches in terms of gate delays.

The multiplier is a basic building block in Standard Digital Signal Processors (DSP). Most of the DSP tasks require real-time processing with several multiplications. Multiplication is most important arithmetic operation having wide applications from normal multiplication in DSP. Multiplication process is used in many applications like

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instrumentation and measurement, communications, audio and video processing, animations, special effect, Graphics, image enhancement, Navigation, radar, GPS, and control applications like robotics, machine vision. Multiplication is the process of adding a number of partial products. Multiplication algorithms differ in terms of partial product generation and partial product addition to produce the final result. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications.

With time applications, many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other. The need of fast multiplication has gives rise to algorithms such as Baugh-Wooley method, Booth multiplier using recoding bits, Modified Booth algorithm (MBE). Although the MBE is most successful algorithms yet it is also a time consuming process. Nowadays, new methods are required for even faster multiplication strategies. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics [4]. By using this technique we can improve the computational speed of processor to perform fast arithmetic operation

The need of high speed and low power multipliers are increasing day by day in digital signal processing and high speed general purpose processor design. Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and Booth multiplication algorithm. The computation time taken by the array multiplier is comparatively less because the partial products are calculated independently in parallel. The mathematical operations using Vedic Method are very fast and require less hardware, this can be used to improve the computational speed of processors. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of high speed multiplier is increasing as the need of high speed processors are increasing. Higher throughput arithmetic operations are important to achieve the desired performance in many real time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications**.** In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. As the common digital signal processing algorithms spend most of their time multiplying, the processors spend a lot of chip area in order to make the multiplication as fast as possible. Hence a non conventional yet very efficient Vedic mathematics is used for making a high performance multiplier.

A. *Problem Statement*

Multiplication is an important function in arithmatic operations.multiplication based operations such as multiply and accumulate and inner product are among some of the frequently used computation intensive arithmatic functions currently implemented in many digital signal processing applications.since multiplication dominates the execution time of most DSP algorithms.so there is a need of high speed multiplier.digital multipliers are the core components of all the DSP processors and the speed of the DSP is largely determind by speed of its multipliers.Two most common multiplication algorithms followed in digital hardware are array multiplication and booth multiplication algorithm.In the existing system they use algorithm for the mulatiplication. It takes nearly 82.834ns for 32x32 bit multiplication. And also the vedic multiplier based on only the nikilam sutra takes 156.38ns delay for 32x32 bit multiplication.

II. RELATED WORK

DESIGN, IMPLEMENTATION AND PERFORMANCE ANALYSIS OF AN INTEGRATED VEDIC MULTIPLIER ARCHITECTURE

Ramachandran.S, Kirti.S.Pande says that Fundamental and the core of all the Digital Signal Processors (DSPs) are its multipliers and speed of the DSPs is mainly determined by the speed of its multipliers. Multiplication is the most fundamental operation with intensive arithmetic computations. Two important parameters associated with multiplication algorithms performed in DSP applications are latency and throughput. Latency is the “real delay of computing a function”. Throughput is a measure of “how many computations can be performed in a given period of

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time". The execution time of most DSP algorithms is dependent on its multipliers, and hence need for high speed multiplier arises.

Urdhva tiryakbhyam sutra illustration

Multiplication is based on an algorithm called Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. The Sanskrit term means "Vertically and crosswise". The idea here is based on a concept which results in the generation of all partial products along with the concurrent addition of these partial products in parallel. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in Figure.3.1. Since there is a parallel generation of the partial products and their sums, the processor becomes independent of the clock frequency. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The advantage here is that parallelism reduces the need of processors to operate at increasingly high clock frequencies. A higher clock frequency will result in increased processing power, and its demerit is that it will lead to increased power dissipation resulting in higher device operating temperatures. By employing the Vedic multiplier, all the demerits associated with the increase in power dissipation can be negotiated. Since it is quite faster and efficient its layout has a quite regular structure. Owing to its regular structure, its layout can be done easily on a silicon chip. The Vedic multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers, thereby making it time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

Nikhilam sutra illustration

The Sanskrit term Nikhilam means "all from 9 and last from 10". It is also applicable to all cases of multiplication, but it tends to be more efficient when the numbers involved are large. This is because, it just finds out the compliment of the large number from its nearest base to perform the multiplication operation on it. Larger the original number, lesser the complexity of the multiplication.

This sutra is illustrated by considering the multiplication of two decimal numbers (94 * 88) where the chosen base is 100 which is nearest to and greater than both these two numbers. The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (6*12 = 72). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 94 - 12 = 82 or 88 - 6 = 82. The final result is obtained by concatenating RHS and LHS (Answer = 8272).

DESIGN AND IMPLEMENTATION OF LOW POWER AND AREA EFFICIENT ADDER AND VEDIC MULTIPLIER FOR FFT

Silambarasan C.A. L. Vanitha says that the ever increasing demand in enhancing the ability of processors to handle the complex and challenging processes Resulted in the integration of a number of processor cores into one chip. This load is reduced by supplementing the main processor with Co-Processor. The Fast Fourier Transform (FFT) is a computationally intensive digital signal processing (DSP) function widely used in application and the speed of FFT depends greatly on the multiplier and adder. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. It is used for design a multiplier. Carry select adder (CSLA) is the fastest adder used to perform an arithmetic functions. The proposed design has reduced area and power as compared with the regular Adders and Multipliers. This work evaluates the performance of the proposed designs in terms of delay, area, power.

Vedic multiplier for FFT

Achieving a successful design means the system should be able to support different operating modes required by diverse applications with low power consumption requirement. Based on the idea of sharing two adders used in the Carry Select Adder (CSA), a new design of a low-power high performance adder is presented. The new adder is faster

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than a Ripple Carry Adder (RCA), but slower than a CSA. On the other hand, its area and power dissipation are smaller than those of a CSA. In a typical processor, Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multipliers. In computers, a typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operations.

The comparative study of different multipliers is done for low power requirement and high speed. This gives information of "Urdhva Tiryakbhyam" algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics also suggests more formulae for multiplication i.e. "Nikhilam Sutra" which can increase the speed of multiplier by reducing the number of iterations. This gives information of "Urdhva Tiryakbhyam" algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics also suggests more formulae for multiplication i.e. "Nikhilam Sutra" which can increase the speed of multiplier by reducing the number of iterations. Increasingly huge data sets and the need for low power in adders tend to increase. The traditional serial adders are no longer suitable for large adders because of its huge area and high power. All systems tend to trade off between speed and power. The computation time taken by the array multiplier is comparatively less, because the partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array. Large booth arrays are required for high speed multiplication and exponential operations which in turn require large partial sum and partial carry registers.

Multiplier Using Vedic Mathematics

Complex multiplication is of immense importance in digital signal processing (dsp) and image processing (ip).to implement the hardware module of discrete fourier transformation (dft), discrete cosine transformation(dct), discrete sine transformation (dst) and modem broadband communications; large numbers of complex multipliers are required. Complex number multiplication is performed using four real number multiplications and two additions/ subtractions. in real number processing, carry needs to be propagated from the least significant bit (lsb) to the most significant bit (msb) when binary partial products are add

By employing the Vedic mathematics, an n bit complex number multiplication was transformed into four multiplications for real and imaginary terms of the final product. "Nikhilam navatascaramam dasatah" sutra is used for the multiplication purpose, with less number of partial products generation, in comparison with array based multiplication. when compared with existing methods such as the direct method or the strength reduction technique, our approach resulted not only in simplified arithmetic operations, but also in a regular array like structure. The multiplier is fully parameterized, so any configuration of input and output word-lengths could be elaborated. Transistor level implementation for performance parameters such as propagation delay, dynamic leakage power and dynamic switching power consumption calculation of the proposed method was calculated by spice spectre using 90 nm standard CMOS technology and compared with the other design like distributed arithmetic, parallel adder based implementation and algebraic transformation based implementation. The calculated results revealed (16, 16) x (16, 16) complex multiplier have propagation delay only 4ns with 6.5 mw dynamic switching power.

A TRANSISTOR LEVEL ANALYSIS FOR AN 8-BIT VEDIC MULTIPLIER

Arun K Patro & Kunal N Dekate says that Power and area efficient multiplier using CMOS logic circuits for applications in various digital signal processors is designed. This multiplier is implemented using Vedic multiplication algorithms mainly the "Urdhva tiryakbhyam sutra", which is the most generalized one Vedic multiplication algorithm. A multiplier is a very important element in almost all the processors and contributes substantially to the total power consumption of the system. The novel point is the efficient use of Vedic algorithm (sutras) that reduces the number of computational steps considerably compared with any conventional method.

The Vedic Sutras

Depending on the various branches of mathematics, Vedic algorithms are divided into 16 sutras (algorithms), out of which two sutras are for multiplication as:

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- Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
- Urdhva-Tiryagbhyam – Vertically and crosswise.

This is based on Urdhva-Tiryagbhyam sutra of Vedic multiplication, which is the most generalized method for multiplication. This sutra is used for binary multiplication for making the digital multiplier. It can be synonymously called as "Vertically and Crosswise" method of multiplication. An illustration of this multiplication algorithm is shown in the Figure.3.8 below. Considering a digital hardware, a Vedic multiplier will be more power efficient and faster also as less number of steps required for multiplication. Also there is hardly any limitation attached to this multiplication algorithm.

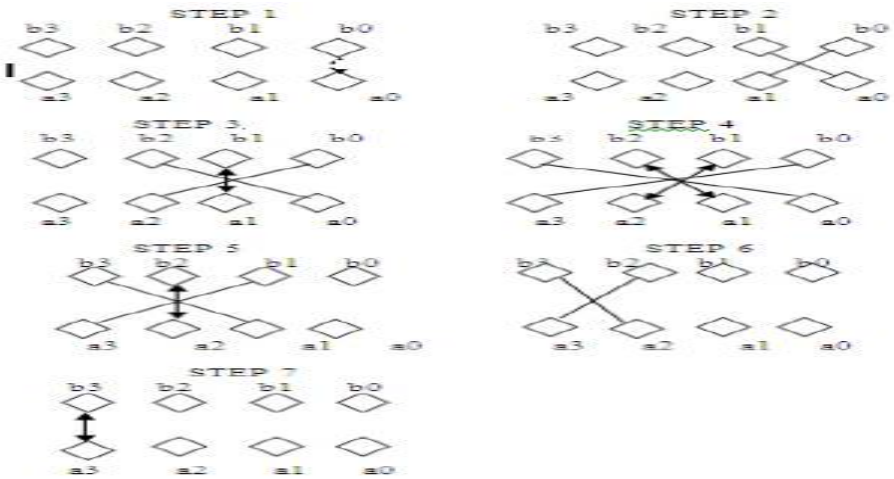

Figure.1 Line-Diagram for Urdhva-Tiryagbhyam Sutra multiplication

COMPARE VEDIC MULTIPLIERS WITH CONVENTIONAL HIERARCHICAL ARRAY OF ARRAY MULTIPLIER

Arushi Somani, Dheeraj Jain, Sanjay Jaiswal, Kumkum Verma and Swati Kasht says that Multiplication is an important function in arithmetic operations. A CPU (central processing unit) devotes a considerable amount of processing time in performing arithmetic operations. Multiplication requires substantially more hardware resources and processing time than addition and subtraction. Digital signal processors (DSPs) are the technology that is omnipresent in engineering Discipline. Fast multiplication is very important in DSPs for digital filter, convolution, Fourier transforms etc. This paper presents the comparative study of Vedic Multiplier are Urdhva Tiryakbhyam multiplier with Conventional multiplier Hierarchical array of array multiplier on various performance factors like power, delay, space, speed, Power Delay Product and Energy Delay Product.

Conventional Vs. Vedic Multiplication Scheme

The Vedic mathematics is the ancient system of mathematics which has a unique technique for fast mental calculations, based on 16 sutras. This approach is completely different from other multiplication algorithms and considered very close to the way a human mind works. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. It covers explanation of several modern mathematical terms including arithmetic, trigonometry, plain, calculus, quadratic equations, factorization and spherical geometry.

In a hierarchical implementation of multiplication based on an array of array technique. This multiplier architecture is based on generating all partial products and their sums. We have considered this architecture name as HAOA. This architecture shows moderate area and delay performance. This claimed that HAOA multiplier is faster

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than the corresponding array multiplier and Booth multiplier. Thus the proposed unsigned Array of Array multiplier circuit is designed with hierarchical structuring. It has been optimized using Vedic Multiplication Sutra "Urdhva Triyagbhyam" and Karatsuba-Ofman algorithm. It has showed large reduction in average power dissipation and in time delay as compared to Booth encoded radix-4 multiplier. It presented a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics. This Multiplier architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. The Urdhva – Tiryagbhyam sutra under Vedic mathematics is the general formula applicable to all cases of multiplication. The formula being very short and terse consists of only one compound word, means "vertically and crosswise".

III. PROPOSED WORK

It is more efficient when the numbers involved are large. It has also shown the effectiveness of this logic table to reduce the *N x N* multiplier structure into an efficient 4 *x* 4 multiplier structures. Vedic multiplier which is designed based on delay for 32x32 bit multiplication. A Network is a system of programs and data structures that approximates the operation of the human brain. A Network usually involves a large number of processors operating in parallel. A network is initially trained about data relationship. A network use several principles, including gradient based training, Vedic logic, genetic algorithm, Boolean Methods. Karnaugh Map is an efficient method of minimization for conventional logic design. It is used for 3 or 4 variables at most 6 variables. In our proposed system we modify the karnaugh map and propose a set of reduction rules for quantum Boolean circuit optimization. By applying these rules we can efficiently simplify a quantum Boolean circuit that has an arbitrary number of input variables. For this we propose an algorithm to simplify logic functions with any number of variables by using the modified karnaugh Map. A new fast simplification method is presented. Such method realizes karnaugh map with large number of variables. In order to accelerate the operation of the proposed method, a new approach for fast detection of group of ones is presented. Such approach implemented in the frequency domain. The search operation relies on performing cross correlation in the frequency domain rather than time one. It is proved mathematically and practically that the number of computation steps required for the presented method is less than that needed by conventional cross correlation. It is an efficient way of reducing Boolean function to a minimum form For the purpose of minimizing hardware requirements. Karnaugh Map is an efficient method of minimization for conventional logic design. It is used for 3 or 4 variables at most 6 variable. In our proposed system we modify the karnaugh map and propose a set of reduction rules for quantum Boolean circuit optimization. By applying these rules we can efficiently simplify a quantum Boolean circuit that has an arbitrary number of input variables. For this we propose an algorithm to simplify logic functions with any number of variables by using the modified karnaugh Map. Karnaugh map is used as a method for minimizing a Boolean expression. It is usually aided by a rectangular map of the values of the expression for all possible input combinations. Input values are arranged in a code, which is an ordering of 2 power n binary numbers such that only on bit changes from one entry to the next.

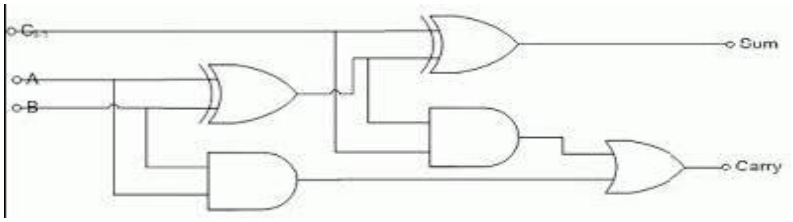

Figure 2: Full Adder Using K-Map

Full adder is a combinational circuits that can add three bits. The circuits consists of two half adders and one OR gate. The output of OR gate is the carry and the output of second XOR gate is the sum. It is possible that more than one reduction rules can be applied at the same time. We modify the karnaugh map and propose a set of reduction rules for quantum Boolean circuit optimization. Always combine as many cells in a group as possible. This will result in the fewest number of literals in the term that represents the group. Make as few groupings as possible to cover all minterms. This will result in the fewest product terms. Always begin with the largest group, which means if you can find eight members group is better than two four groups and one four group is better than pair of two-group. By

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applying these rules, we can efficiently simplify a quantum Boolean circuit. A shortcut hand reduction method known as Karnaugh Map.

A. *ADVANTAGES*

- Vedic formulae are claimed to be based on the natural principles on which the human mind works.
- Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one.

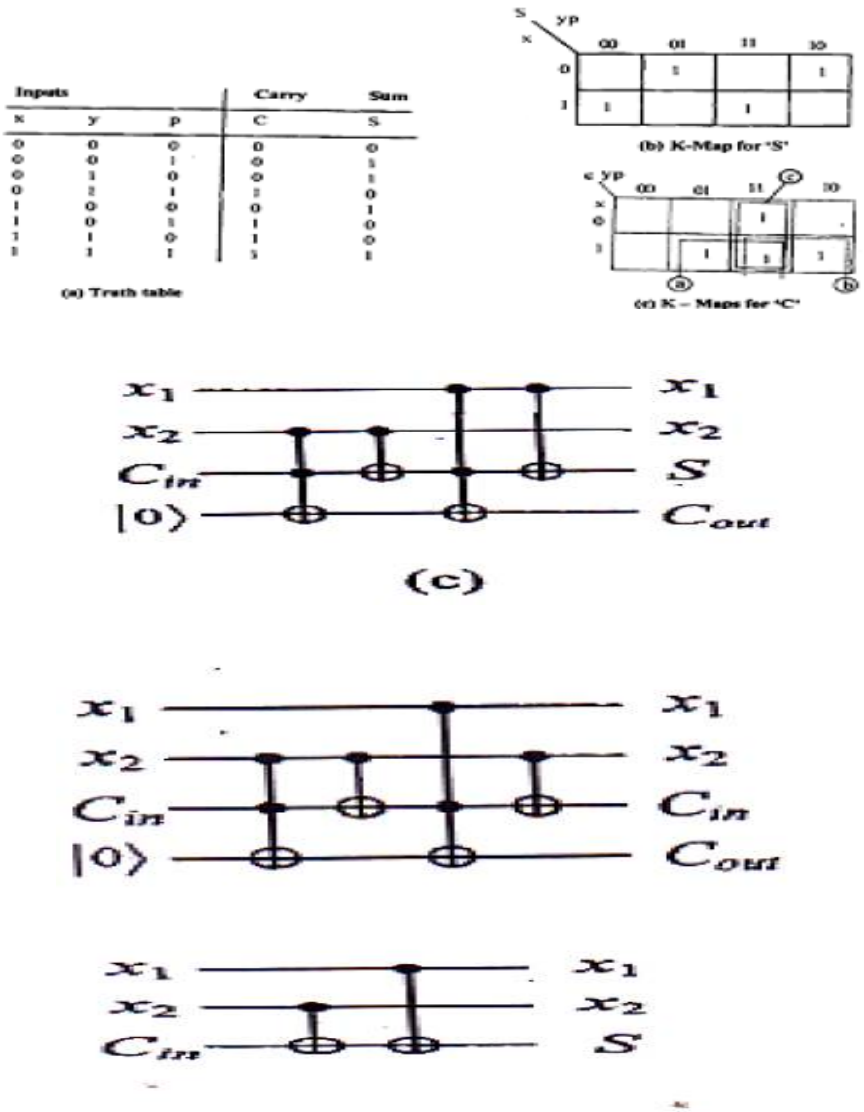

Figure 3: The K-Map for Sum and Carry

IV. CONCLUSION

The proposed algorithm is based on the looping of redundant terms. Therefore in order to take a closer look at how to loop two, four or eight 1‟s to get the least possible number of groups in a K-map table setting. Boolean algebra, Karnaugh maps, are methods of logic simplification. The goal of logic simplification is a minimal cost solution. A

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minimal cost solution is a valid logic reduction with the minimum number of gates with the minimum number of inputs. Venn diagrams allow us to visualize Boolean expressions, easing the transition to Karnaugh maps. Karnaugh map cells are organized in Vedic multiplier order so that we may visualize redundancy in Boolean expressions which results in simplification.

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BIOGRAPHY

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