ISSN(Online) : 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 4, April 2016

Design and Analysis of a maximum length 5-Bit Parallel Linear Feedback Shift Register using VHDL Structural Modeling

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ABSTRACT: Very Large Scale Integration is the latest most popular technology that has reduced the size of almost all electronic circuits and devices to a large extent. Out of the two coding languages for VLSI simulation i.e. Verilog and VHDL, the latter is the most preferred option for present designing because of its variety and efficiency in simulations. In this paper we present the design and analysis of a5-bit Linear Feedback Shift Register (LFSR) through the Structural Modeling method of VHDL coding. The paper aims at highlighting the design advantages and drawbacks of structural modeling over the other types of design modelling in VHDL, while creating a maximum length 5-bit LFSR using the software Xilinx9.2i.Moreover, Structural VHDL which has only been used for circuits with one or two components, if used to design more complex circuits can help the practical software visualization of these circuits possible, making the error corrections and technical advancements very easy.

KEYWORDS: Structural Modeling; LFSR; Behavioral Modeling; VHDL.

I. INTRODUCTION

VHSIC Hardware Descriptive Language (VHDL) is the software language in which the codes and logic are synthesized and burnt to create Very Large Scale Integrated (VLSI) Circuits. As technology is evolving day by day, challenges like efficient performance, power optimization, cost effectiveness and reliability are arising in VLSI. Finding out error locations in the big and complex VLSI circuits is also a tedious process.

Here we have implemented a 5 bit length sequence using Structural VHDL with maximum length feedback polynomial to understand the memory utilization, speed requirement and error detection capabilities of an LFSR circuit. Further, we have presented the comparison of performance analysis on synthesis and simulation results of a previously designed 5-bit LFSR through Behavioural Modeling [1] and our design of an LFSR through structural modeling. This would lead us to a better analytical conclusion whether our design of an LFSR through Structural Modeling is more efficient or not.

Although designing of LFSRs have already been done through the behavioural modeling method [1] [2] [3] [4], synthesis and analysis done by structural modelling concludes to different results. Structural VHDL allows designers to represent a system in terms of components and their interconnections, so rather than brain storming and finding out the logic behind the working of a circuit, designing in structural VHDL just requires the block diagram of the desired circuit. Thus, it is very easy to code a circuit in the Xilinx software using structural modelling. The target device that we have used is Xilinx Spartan 3A and performed simulation and synthesis using Xilinx ISE.

II. RELATED WORK

In [4] authors explained the various styles of VHDL modeling which include i) Dataflow modeling ii) Behavioral modeling iii) Structural modeling iv) Hybrid modeling. Out of these models the most preferred one for coding is the behavioral modeling as it is based on the logic and the behavior of the entities of the desired circuit. In dataflow modeling we just have to know about the Boolean algebra and how the data flows inside the program. The least

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abstract is the structural modeling where the design is stated almost exclusively as component instantiations with connecting registers and wires. The structural style of modeling comes into picture when we have to deal with bigger projects. The big project is divided into small modules and we have to design each module separately. At the end of the project each module is added as the component in the main program. In the Hybrid modeling any of the above mentioned.

A Linear Feedback Shift Register (LFSR) is a shift register whose input bit is a linear function of its previous state. Feedback around a LFSR's shift register comes from a selection of points (taps) in the register chain and constitutes X-ORing or X-Noring these taps to provide tap(s) back into the register. Register bits that do not need an input tap, operate as a standard shift register. It is this feedback that causes the register to loop through repetitive sequences of pseudo-random values. The choice of taps determines how many values there are in a given sequence before the sequence repeats. From [1] we get to know that for a 5-bit LFSR, if tap number 1 and 4 are X-ored or X-nored then the LFSR gives the maximum number of states of random variables which is equal to 2^n-1 states i.e. 31 states of random variables will be generated before the sequence repeats. Also, a seed value is to be given as the first input to the LFSR design.

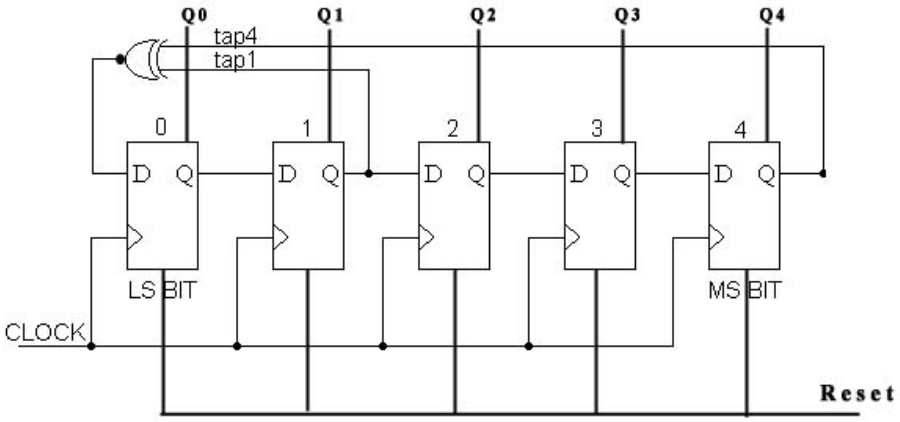

Figure 1: Block diagram for a 5-bit maximum length LFSR

Analysis of this LFSR design till now has been done only through behavioural modeling. Our main aim in this paper is to present the design from structural VHDL point of view and find out whether it is better to use structural modeling over the behavioural one, when it comes to designing larger complex circuits.

Table 1: Update of the Flip flops

Clock Cycle	0	1	2	3	4
X-NOR result of	1,4	0,3	2,updated FF0	updated FF1,FF4	updated FF3,FF0
Stored at Flip Flop	0	1	2	3	4

III. PROPOSED ALGORITHM

The above Figure 1 represents the block diagram of a 5-bit LFSR, consisting of 5 D-Flip flops (D-FF) placed in series, and providing an X-nored feedback of the outputs of 2nd and 5th D-FF[6].Output is taken from each flip flop with bits moving from LSB to MSB flip flop in each clock pulse. While using structural modeling to code our 5-bit LFSR, the block diagram can be divided in to 3 modules, separately designing each component of the circuit.The 3 modules are-

1. D-Flip flop design
2. X-nor gate design
3. Final LFSR design

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A. Design Considerations:

- Positive edge triggered clock is being used
- D-FF and X-nor gate are designed using behavioral modeling
- No initial seed value is given.
- For maximum length of random sequence to be generated the output of D-Flip flop 1 and 4 will be considered as taps (inputs to the X-nor gate).

B. Description of the Proposed Algorithm:

Aim of the proposed algorithm is to simplify the coding for complex circuits, run the LFSR circuit without giving any seed value and to check whether the final circuit has better memory utilization. The proposed algorithm is consists of three main steps.

Step 1: Designing of the D-Flip Flop:

It is a flip flop whose output Q is always equal to its input D whenever it is triggered by a clock pulse.[7]

PSEUDO CODE:

If clock is applied then,

```
If D=1 then
        Q=1
Else
        Q=0
End
End
```

Step 2: Designing an ex-nor gate:

Logic gates are the fundamental building blocks of electronic design. EX-NOR gate is the one whose output is high only when both of its inputs are different, otherwise its logic low.[8]

PSEUDO CODE:

```
If   input1= input2   then
        Output = HIGH
Else
        Output = LOW
End
```

Step 3: Designing the LFSR using structural modelling

PSEUDO CODE:

Instance 1: D-FF is called and is mapped as the 0^{th} shift register of LFSR structure.
Instance 2: D-FF is called and is mapped as the 1^{st} shift register of LFSR structure.
Instance 3: EX-NOR gate is called and mapped as the feedback path of LFSR structure.
Instance 4: D-FF is called and is mapped as the 2^{nd} shift register of LFSR structure.
Instance 5: D-FF is called and is mapped as the 3^{rd} shift register of LFSR structure.
Instance 6: D-FF is called and is mapped as the 4^{th} shift register of LFSR structure.

IV. SIMULATION RESULTS

The simulation studies involve the RTL schematics and test bench simulation outputs. The proposed structural modeling algorithm is implemented with Xilinx 9.2i. Proposed algorithm simulation results are compared with the post simulation values of the various parameters of behavioral modeling, to understand the positives and negatives of preferring structural modeling method over behavioral modeling.

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The program written in a new project of Xilinx is first checked for syntax errors and then synthesized using the implement design icon. Once the code is mapped in the software, all the information about the time taken for simulation, delays and memory space used for running the program comes up in the design summary.

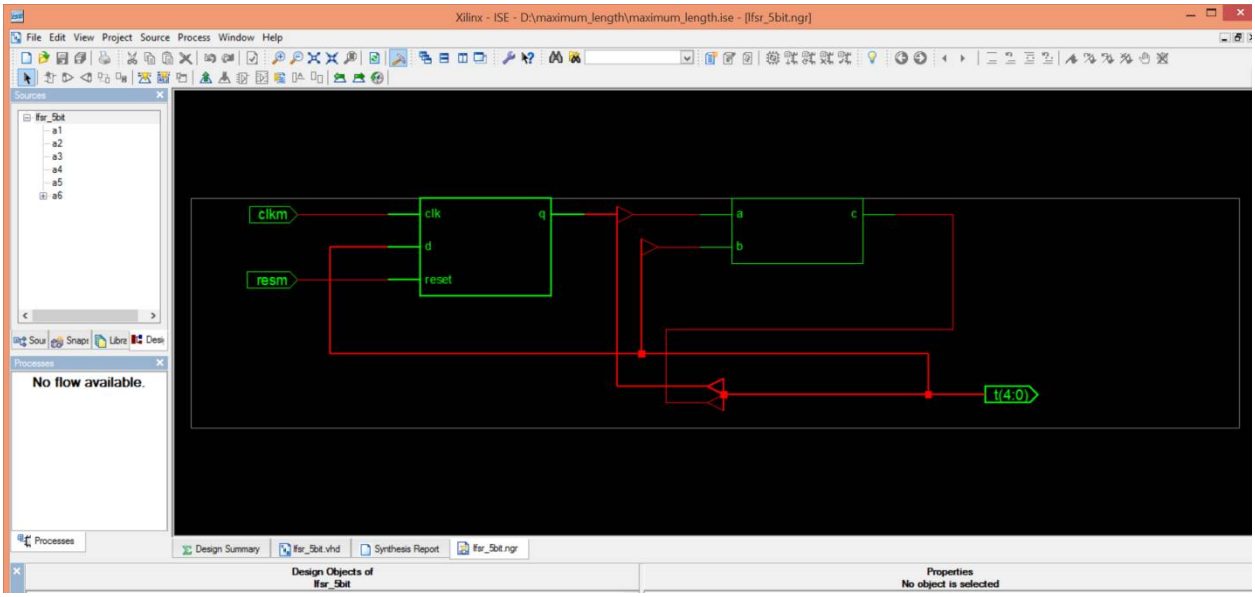

Figure2: RTL Schematic of Maximum length LFSR

The Figure 2 shows the RTL Schematic block diagram of our designed 5-bit, maximum length Parallel Linear Feedback Shift Register. The left block in the diagram shows the D- flip flops D0 to D4 and the right block is the X-Nor gate with inputs of a, b and output as c.

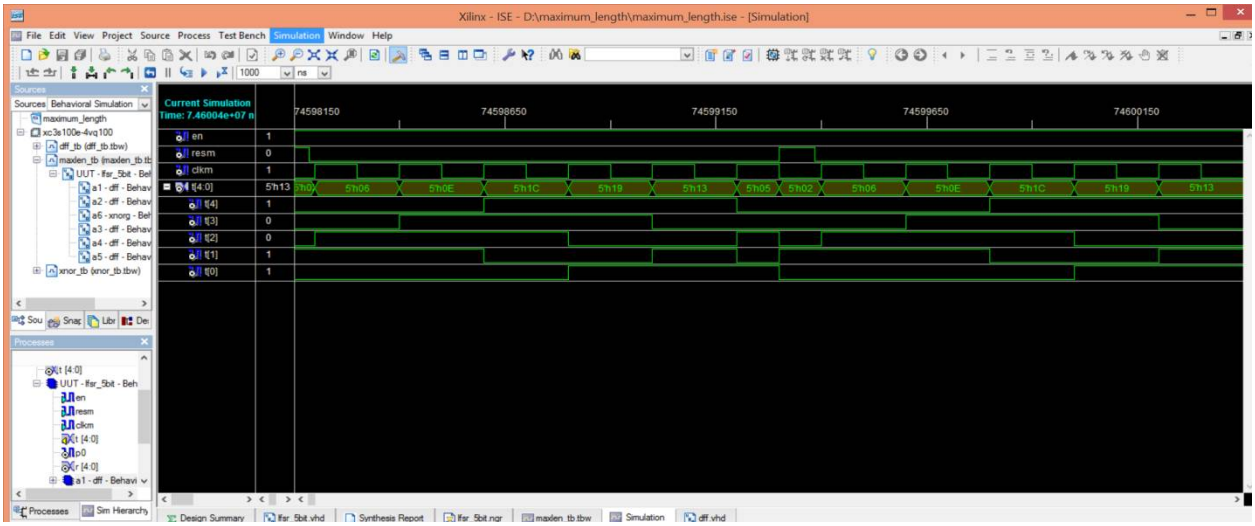

Figure 3: Test bench waveform of the maximum length lfsr.

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The test bench simulation result is shown in Figure 3. Along with the output waveform of each D-Flip flop it shows the hex code for each state of the maximum length LFSR. Each state is changing according to the changing clock pulse. Total of 31 hex values can be seen in the test bench output after simulation.

The following table shows the HEX values of the 31 states output as generated by the maximum length LFSR coded by us.

Table 2: Changing of the 31 states of our 5-bit maximum length LFSR.

present state	next state(Hex Data)
06 H	OE H
OE H	1C H
1C H	19 H
19 H	13 H
13 H	05 H
05 H	08 H
08 H	10 H
10 H	03 H
03 H	04 H
04 H	0A H
0A H	14 H
14 H	0B H
0B H	16 H
16 H	0F H
0F H	1E H
1E H	1D H
1D H	1B H
1B H	17 H
17 H	0D H
0D H	1A H
1A H	15 H
15 H	09 H
09 H	12 H
12 H	07 H
07 H	0C H
0C H	18 H
18 H	11 H
11 H	01 H
01 H	00 H
00 H	02 H
02 H	06 H

.

Once all the components are called, the entire circuit is reset once and then clock is applied. With the application of continuous clock pulses, the LFSR keeps on changing its output state.

The initial 31 states (2^5-1) [1] will be different from each other and random. After these 31 states it will start repeating itself. So, we can say that the maximum length 5-bit LFSR has a time period of 31 T-states.

V. ANALYSIS

We in this paper have chosen comparison based analysis to find out the pros and cons of Structural modeling over Behavioral modeling. For writing up a code through behavioral modeling, knowing the logic of the circuit is must,

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hence for circuits with complex and un-simplified logic, coding in VHDL gets a bit tedious, whereas structural modeling requires no logic and only the circuit diagram to get coded in VHDL. We considered the Design summary of the simulation as the basis of the comparison. The device utilization parameters, clock report, map report, static time and route simulation present in the design summary, are the basic deciding factors for concluding that structural modeling is better for designing larger complex circuits.

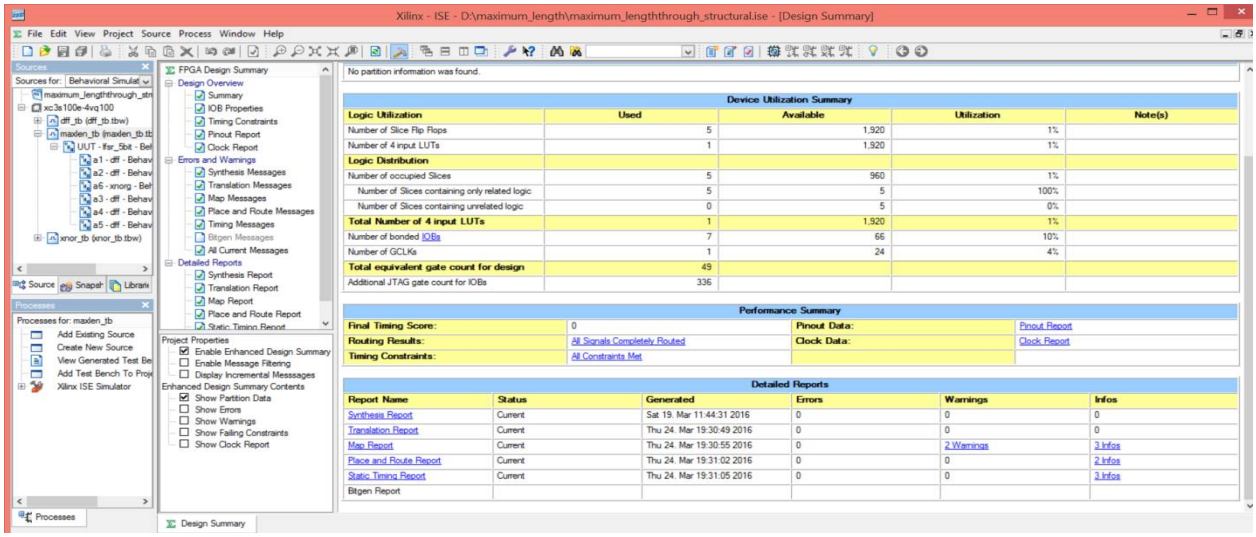

Figure 4: Design Summary of structurally modelled LFSR

Figure 4 shows the value of the various parameters obtained after the simulation and implementation of our design by using Structural Modeling. The values of the synthesis report, mapping and place report have been elaborated in the comparison table below.

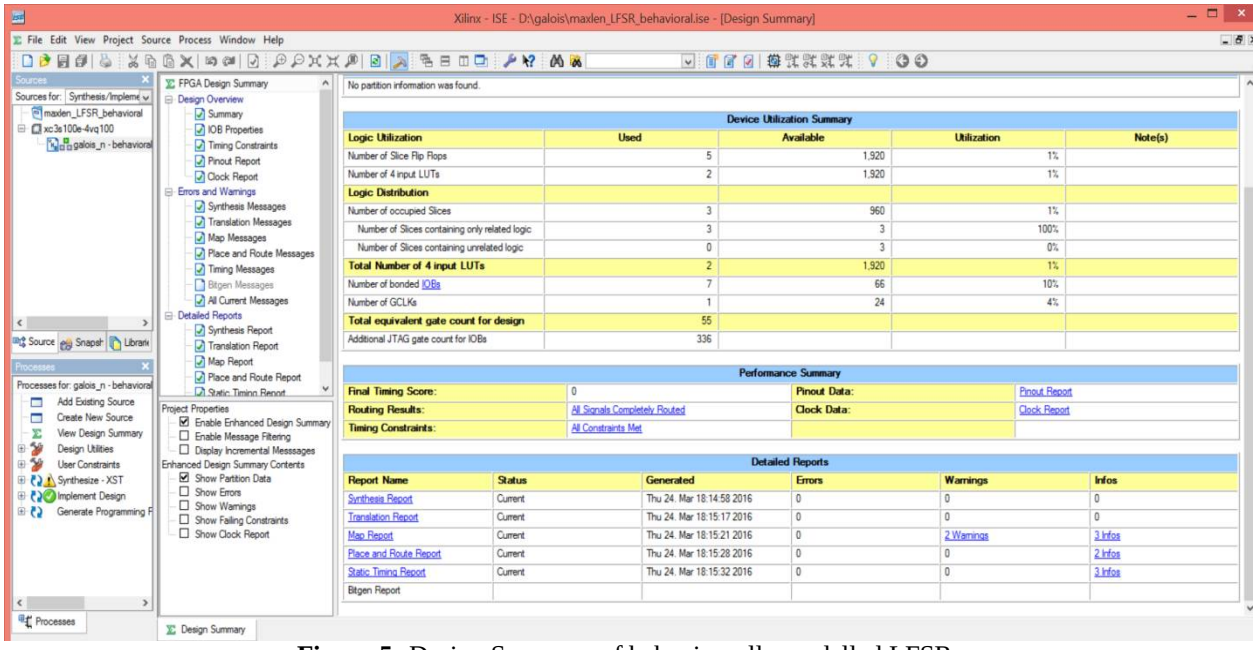

Figure 5: Design Summary of behaviourally modelled LFSR

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ISSN (Print) : 2320-9798

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Figure 5 shows the design summary of our maximum length LFSR when designed using behavioural modelling. The total equivalent gate count and number of LUTs required are more in number when behvioral modelling is used.

The following table shows the difference in the values of the various parameters in design summary of a structurally modelled and behaviorally modelled LFSR as given in the design summary of each.

Table 3: Comparison between the simulation results of a 5-bit LFSR designed through structural modeling and behavioral modeling.

Design parameters	Structural Modeling	Behavioral modeling.
Device Utilization		
1. Number of 4 input LUTs required	1	2
2. Gate Count	49	55
3. Fan out	5	3
Clock Report		
1. Net Skew	0.003ns	0.002ns
2. Maximum Delay	0.042ns	0.039ns
Time Report		
1. Best Case Achievable	2.053ns	2.034ns
2. Worst Case Slack	1.027ns	1.025ns
Map Report		
Real Time taken to map design	2 sec	1 sec
Peak memory Used	116 MB	119MB
Rate Simulation		
Number of Routable Networks	10	9
Total memory Usage	129236Kilobytes	128212Kilobytes

VI. Conclusion and Future Work

Design and analysis of a maximum length LFSR through structural modeling is discussed in this paper.The simulation results showed that though structural modeling causes more delay in simulation as compared to that of behavioral modeling, the proposed structural modeling algorithm has a lesser gate count and peak memory usage than the behavioral modeling algorithm. One of the most important advantages of structural hierarchical design is that one has a structural and practical modularization of the design with well-defined interfaces. This can reduce the design time considerably. Further, corrections and additions in the coding for even complex circuits is not a tedious process. Another function that one can perform during the structural design is to understand and verify the intended behaviour or logic of a design by studying the interconnections. So it is the easiest way of coding for first time users. Writing codes through structural modeling may seem lengthy, but for bigger and complicated circuits, it can be considered as the best choice for coding in VLSI.

VII. ACKNOWLEDGMENT

We would like to thank our institute Bhilai Institute of Technology, Durg and department for providing us ample opportunities to accomplish our research work. We are grateful to Mr. Saurabh Singh, Associate Professor, Bhilai Institute of Technology, Durg for guiding us with his valuable ideas and all others who directly and indirectly helped us in the completion of our paper. Finally we thank our families for being a constant source of support and motivation, throughout our work.

ISSN(Online) : 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

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BIOGRAPHY

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