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Review of Different Low Power VLSI Circuit with Interconnect Scatter

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ABSTRACT-Now-a-days transistor‟s performance had becoming slower due to the deep submicron VLSI fabrication process, where the interconnect cables were wider and thicker. For cable and transistor dimensions with feature size less than 10nm, but cable capacitance are now larger, and power dissipation in cables may be critical. Therefore due to the technology scaling, the power dissipation for global cables will increase with interconnect cable length. The plot of VLSI paths now-a-days has become very challenging. One of the main factors that degrade the path performance is the power dissipation. Especially in the deep submicron(DSM) regime, interconnect power dissipation becomes a dominant factor in the overall path performance. For reducing interconnects delay, buffer insertion and cable sizing are the effective methods. However, the large number of inserted buffers will consume large amount of power**.** Reducing the shortest path cablelength between sources to sink will also consume minimum power. The main factor affecting system performance in VLSI path plot is the interconnect delay. A successful VLSI plot nowadays depends heavily on a successful interconnect plot. Prior to deep submicron era, noise effect and delay optimized interconnect plots can be obtained by simply optimizing the interconnect topology.

KEYWORDS: VLSI Circuit, Low Power, Interconnect Scatter

I. INTRODUCTION

Very Large Scale Integration plot has tremendous growth over the last ten yearswith features sizes being downscaled from micrometer to nanometer regime. Moore‟s law states that the total number of transistors on a single integrated path doubles every 1.5 years.

The migration is from few hundreds of transistors on a single fragment to the few millions of transistors on a single fragment now-a-days. This significant migration is possible only by reducing the feature sizes of the transistor integrated path. The feature sizes have moved from few micro meters to few nanometers. Due to the increasing high complexity of modern VLSI fragment plot, Electronic Plot Automation (EDA) tools play an important role in delivering high system performance. VLSI physical plot process includes partitioning, floorplanning, placement, scatter and compaction (Chang et al 2000 & Chen et al 1999). In future, the tremendous growth of VLSI paths will rely on the development of physical plot automation tools.In the physical plot process, Scatter has been an important problem in VLSI backend

plot since the quality of scatter results has great impact on various plot metrics such as path delay, power consumption, fragment reliability and manufacturability etc. With the advanced fabrication technology entering nanometer scale, especially VLSI scatter has been facing more challenges. With devices operate at a higher speed, the interconnect delay and interconnect power dissipation become more significant. The problem of minimizing these interconnect delay and interconnect power dissipation has been addressed at scatter stage.

Scatter is the process of arranging path cables on a layout. In VLSI plot, scatter consists of determining shortest path between source to sink positions of all blocks on the layout, such that the cablelengths are minimized and constraints are satisfied. This work proposes the minimized interconnect power dissipation; the minimized interconnect delay, avoidance of the scatter path congestion.

The steps that make up the physical plot cycle are as follows. The process of dividing the fragment into smaller blocks is known as partitioning. This is frequently done to separate particular useful blocks and to make placement and scattering simpler. Partitioning can take place during the RTL plotting section, where the graphing engineer divides the entire design into submodules and plots each submodule (Kennings, 1994). Together, these modules make up a major module known as a "superior" module. According toAlpert&Kahng (1995), the direction partition is known as NPhard. The partitioning problem can be approximated in part by some ride.

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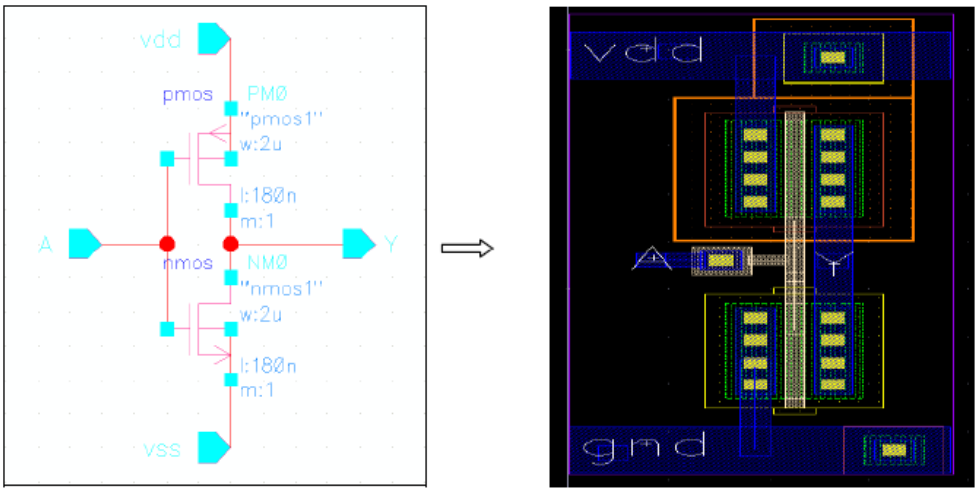

(a) (b)

Figure 1: Physical Design Process

Planning the floor The floor is an essential step in the hierarchical diagramming method of building modules. In that we have a set of rooms (modules) and prefer to determine the approximate area of each room based solely on the criteria, the difficulty of floor planning in a fragmented sketch is comparable to flooring planning in a building lot. adjacent solstice. A successful flooring planning step will accomplish numerous objectives, including reducing sign latency, facilitating the subsequent diffusion stage, and minimizing the entire fragmentation area. It also involves selecting the best design options for each block and the entire shard. After zoning, an estimate of the block's location can be made based solely on the block's range and type of features. According to Sait& Youssef (1995), the required connection region within the block should also be taken into consideration.

II. LITERATURE REVIEW

Very Large Scale Integration (VLSI) technology has two billion numbers of transistors that can be placed on a single fragment (Webb 2008). Such complex fragments require power efficient systems. A method was proposed by Webb (2008) to minimize the power consumption of the fragment and is also used to minimize the total cable length for scatter. The plot specifications pointed out by (Dorf 2006) can be used to solve the scatter problem by placing the collection of cells on a fragment. Unfortunately, it was very difficult to find the optimal scatter in polynomial time with deterministic breakthrough (Sharma et al 2012). However, there are many breakthroughs and techniques that are used to find better solutions in polynomial time (Sherwani 1998) solitary. Scatter is one of the complex tasks that accommodate large numbers of components that are connected and satisfy the performance constraints. Performance driven constraints can be controlled by minimizing total net cable length, electrical connection between two adjacent scatter layers and net separation (Sherwani&Bhingarde 1995).Electrical connection between two adjacent scatter layers has larger capacitance than cables, and since capacitance is directly proportional to power, the use of electrical connection between two adjacent scatter layers were minimized. Correspondingly, VLSI interconnect has also become a principal factor to determine the path performance in terms of reliability and cost (Bakoglu 1990) in DSM regime. Consequently, interconnect escalation was proposed in latest years for interconnect performance. Among these techniques, cable sizing escalation method is used to find proper cable width tapering and sizing function for interconnects to meet a definite objective function.Intuitively, the optimal cable sizing (OWS) was considered by (Cong 1996) to meet a definite objective function. Furthermore, in very large scale integration (VLSI) plot, interconnect delay dominates the path performance and complexity (Tang 2001).
Interconnect for deep submicron and nanometer plot has particularly become dominating factor in path performance and reliability. Thus the performance of the VLSI path depends on cable scatter and buffer insertion along the path. The techniques used for interconnect delay minimization are cable sizing, buffer insertion and buffer sizing (Ma et al 2003). PSO approach in VLSI scatter was first implemented by Dong et al (2009). The breakthrough was generally having shortest path in Minimum Rectilinear Steiner Tree (MRST) problem. The problem does not include any buffer and obstacle in VLSI grid graph. The major research issue in grid graph model is to obtain the optimal path which is having the minimum value of interconnect delay from source to sink. The scatter path is lastly obtained and then the buffer is inserted to minimize the delay.

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Buffer insertion is a technique, not only improve timing performance, but can also effectively reduce functional noise by recovering noise margins. The number of buffers necessary to achieve timing closure and meet noise requirements continues to rise with decreasing feature sizes. This problem is more acute in VLSIs, where, in addition to the basic standard building blocks, buffers must be prefabricated and distributed in the layout.

Therefore, it is essential to distribute dedicated buffers in VLSIs, and to plan for them well, prior to the fabrication of the fragment. The buffer insertion problem for VLSI plot has not been fully addressed in publications so far. The work considers that issue is (Wu et al 2004), where it is assumed that a uniform distribution of dedicated buffers is placed throughout the layout, and there is a ratio of 2:1 between number of logic cells and buffers everywhere in the path.Moreover, Dong et al (2009) have introduced a heuristic method to solve buffer insertion and cable sizing problem. However, this method did not handle scatter with obstacles. Without using any escalation technique or breakthrough, the mathematical equation become complex and many variables were used to solve this scatter problem.To solve the complexity problem, Particle Swarm Escalation (PSO) is an escalation technique which is an evolutionary computational technique developed by Ayob et al (2010). PSO is a robust escalation technique based on movement and intelligent of swarm et al (2010) employed particle swarm escalation (PSO) to solve buffer insertion problem in VLSI scatter, with considerations on cable and buffer obstacles. Intuitively, Yusof et al (2011) have also introduced a heuristic method similar to Dong et al (2009) to solve buffer insertion and cable sizing problem. However, this method also not considered the scatter breakthrough with obstacles in VLSI. Subsequently, Zulkiifli et al (2012) exploited particle swarm escalation breakthrough to solve buffer insertion problem in VLSI scatter for cable and buffer obstacles. Moreover, Mahanthi& Rao (2013) initiated the concept of stochastic based Particle Swarm Escalation breakthrough to optimize buffer location for finding the shortest path and to minimize the congestion between the cables.

III. PROBLEM STATEMENT

Though much work has been done on the performance analysis of VLSI scatter based on particle swarm escalation (PSO) breakthrough in the literature, in most of the works, there still lacks the concept of minimizing interconnect delay for optimal path from source to sink in VLSI Grid Graph model. Buffers and obstacles are used in the VLSI Grid Graph model in the literature for analysis. Furthermore, all the breakthroughs reveal in the literature are not scalable and they cannot hold cable sizing problem. Consequently, interconnect power dissipation is a major research issue in deep submicron (DSM) regime that affects the path performance.

The objective of this chapter is to study the impact of pre-detective technology model library functions using standard nanometer specifications for efficient scatter technique. The particle swarm escalation breakthrough is used for optimizing the link between source and sink. The manhattans bending is used for optimizing this breakthrough (Tep 2010). The shortest path VLSI scatter is to be established between the source and sink. Buffers are to be appropriately inserted using PSO breakthrough by implementing the shortest path scatter from source to sink. This proposed breakthrough is useful for finding the minimum power dissipation of buffers inserted in VLSI scatter. The closed form expression for power dissipation is to be derived and is to be simulated with numerical results.

IV. INTERCONNECT SCATTER

The Pre-detective Technology Model (PTM) library functions can be incorporatedusing nanometer technological specifications to optimize the power. The closed form expression for power dissipation is carried out in this chapter with buffer insertion as well aswithout buffer.

The plot of Very Large Scale Integration (VLSI) paths today has become complex and very challenging as anticipated by Moore‟s law. The device size and the switching delay have shrunk continuously. Since many generations ago, the device switching speed no longer limits the path performance, the cable delay becomes dominant. The cable delay or interconnect delay in an IC is the propagation time of signal between transistors. Thus in VLSI technology, interconnect delay reduction becomes an important concern. A significant part of signal delay is due to interconnect delay in deep submicron technology. This interconnect delay has to be predicted before layout, preferably during logic synthesis. The capacitive load on a net are detected using cable load models during synthesis before layout. The load is given as a function of fanout of net and path size cable load model.

For a given fanout, average load for nets is predicted using cable load models, but cannot be useful to predict the individual load of a net (Kapadia & Horowitz 1999). Nowadays, accurate interconnect delay is available after layout and scatter. Because of this, the processes such as synthesis, layout and scatter need to be done several times prior to the plot reaching the timing constraints. When this process does not converge will lead to the problems. To overcome this problem during technology mapping, accurate approximation on cable length has to be given to synthesis engine to achieve timing convergence.

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The signal integrity and performance of deep sub micrometer paths are dominated presently by crosstalk and Interconnect delay. The main reason is that decrease in feature size to the dimension of deep sub micrometer makes the coupling capacitances affect the performance of the path. This is because of increased thickness and decreased spacing of interconnect. A cable with smaller width will have more coupling capacitance. Coupling capacitance is highly sensitive to spacing. If coupling capacitance exists between adjacent or crossing cables then capacitive crosstalk is localized. Due to capacitive coupling, crosstalk called as noise effects the signal integrity and delay. Applying delay escalation methods such as proper cable sizing and spacing, the coupling capacitance impact is limited. A successful VLSI plot nowadays depends heavily on a successful interconnect plot. Prior to deep submicron era, timing optimized interconnect plots can be obtained by simply optimizing the interconnect topology.

Noise in Actual Cable length and Prime Interconnect Delay Approximation

After characterizing set of plots using the above explained cable length model, thecable lengths for various set of plots are approximated. These cable length approximates are good in some cases but very poor in some other cases. Individual cable lengths depend on other variables such as the name of the cells, names of the nets and the order of the cells which are not under user control. If any changes in these variables make changes in individual cable length but average cable length remains constant. The main reason is that if any changes in string variables (example cell name) used in data structures of place and route tool make a problem of a different placement. But this leads to variations in cable length. These variations in cable length are considered as noise which is an inherent variability of Place & Route engine. No one can control this variability. Therefore the individual cable length cannot be approximated beyond certain accuracy. But the noise floor level depends on the particular place and route tool. In order to measure the cable length accurately, in this work, the noise voltage for different interconnect length and width & coupling capacitance for interconnect spacing are analyzed for various nm technology.

Table 1: ISCAS and MCNC benchmark paths

Benchmark Paths	#I	#O	#Comp	#Nets	W_{avg}	N_{row}	AWL (Average Cable Length)	EWL (Approximated Cable Length)
apte	9	73	214	97	4.25	09	1888.24	1873.93
xerox	10	2	696	203	3.19	13	1991.02	1968.23
hp	11	45	264	83	4.51	07	1091.10	1079.44
ami33	33	42	480	123	3.93	12	2065.78	2054.18
ami49	49	22	931	408	2.93	16	3127.44	3028.04

Initially noise in cablelength less than 50 micron for various variables such asname of the cells, order of cells and name of nets are simulated as shown in Figure 2 using the ISCAS and MCNC benchmark paths. In Figure 2, horizontal axis represent actual cable length and vertical axis represent approximated length from actual layouts done for different cell names.

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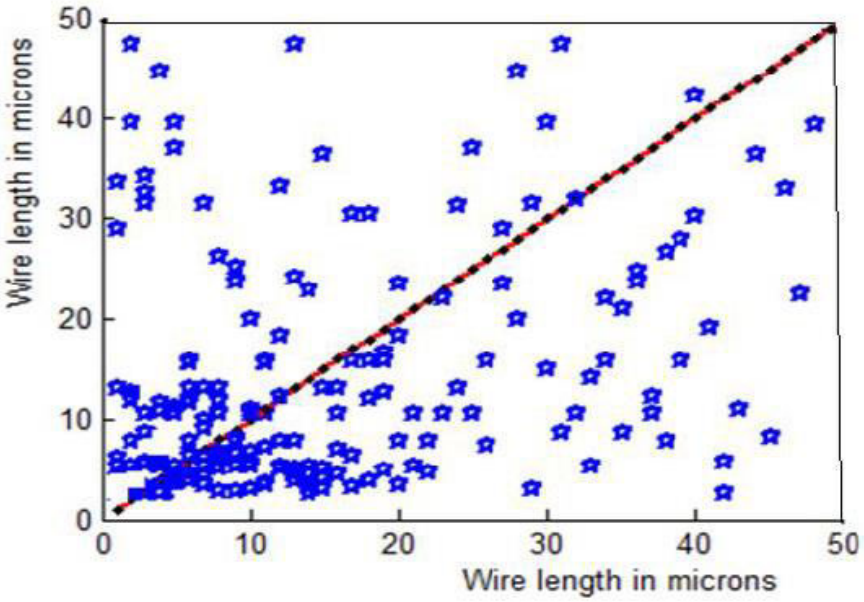

Figure 2: Variation Noise due to Random Variation

V. CONCLUSION

The closed form expressions for minimizing the total power dissipation using shortest path are calculated. The closed form solutions can be used to approximate the power dissipation in VLSI plots. The simulation results show that the simultaneous buffer insertion/sizing and wiring sizing is better than traditional uniformed buffer insertion in terms of optimal shortest path and optimal power allocation. The numerical and analytical results show that the global scatter breakthrough based on particle swarm escalation tool can efficiently bring down the fragment temperature to desired level, and finds the routable solution with better cable length characteristics.

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