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Design and FFT Analysis of Carry Look Ahead Adder

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ABSTRACT: This paper represents the design of 8 and 16 bit CLA in which the noise analysis for different bits of Carry Look Ahead Adder using full custom method is done. Moreover the 8 and 16 bit CLA is simulated which is analyzed in terms of noise and comparison has been done on account of surface area and SNR. The designs include transient analysis, FFT analysis and also evaluate the values of magnitude, phase, and group delay The layout designing is done on 300nm scaling using electric VLSI design system. And LTspiceIV is used for simulation work.

KEYWORDS: Carry look ahead adder (CLA), LTspiceIV, FFT, electric VLSI design system.

I. INTRODUCTION

To obtain any output in any circuit, some operations on the data are needed. Sometimes this can be in the form of arithmetic operations such as addition, subtraction, multiplication and division. These operations are widely used and play a vital role in various digital system such as digital signal processor (DSP) architecture, microprocessor, microcontroller, data process unit and in central processing unit. To perform these operations adders are used.

Adders are the basic building blocks which are designed to perform high speed arithmetic operations and are useful component in digital system as it is also used in address calculation, table indices, and same kind of operations. The basic arithmetic operation which adder performs is the addition of two binary digits. A combination circuit that adds two bits the scheme is called a half adder, and for three bits the scheme is called full adder.

II. RELATED WORK

In VLSI System, layout designing of CLA has been performed using various technologies. In paper[1], the author has given a method of designing an IC layout using 90nm technology. In which both semi-custom and fully custom method was used. And the performance of CLA was measured by comparing the result of semi-custom and full custom in terms of power dissipation and area efficiency. The result shows that, semi-custom method gives slow power consumption and small area in comparison with fully custom method. In paper[2], author aims on a concept of Short Pulse Power Gated Approach (SPOGA), a leakage power reduction technique. The analysis of the circuit was done by using 90nm technology in cadence GPDK. The values of power consumption of the circuit are interpreted from the transient analysis. The result shows that, the short pulse activated the logic block only for the needed short duration thereby reduced the unnecessary consumption. In this paper[3], CD(Constant Delay) logic was used for reducing the power dissipation and for the power delay product. Simulation was done by using H-Spice and delay was checked by Cosmo Scope Z 2007.03 software. The CD logic primarily concentrate on delay improvement at the critical path and yields better PDP. In this paper[4], different static and dynamic logic styles (such as CMOS,DCVS Pseudo NMOS,PTL &Domino logic) was used for the implementation of CLA. The performance was measured by comparing the result in terms of propagation delay, power dissipation, and their delay product. Simulation of circuit was done with the Tanner

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EDA tool, and considering different features size 150nm, 200nm, and 250nm.The result of this paper gives that minimum average power required in case of 4 bit standard CMOS CLA, and maximum average power for the 8 bit pseudo NMOS CLA implementation. This paper[5], focuses on the implementation and simulation of 4 bit, 8 bit & 16 bit of CLA based on verilog code and compared their performance in terms of area, delay, area delay product by using Xilinx as synthesis tool. The result show that carry look ahead adder had least area delay product. In this paper[6], different type of 8 bit adders are analyzed and compared for transistor count power dissipation, delay and power delay product. The performance was measured by comparing the result in terms of power dissipation and PDP. Simulation was done using Tanner environment with 90nm and 180nm technology. The result shows that the carry skip adder and carry look ahead adder uses least number of transistors. And carry skip adder has least PDP (Power Delay Product.). In paper[7], the author has given an alternative log n stage design which is nearly optimum with respect to regularity, area time efficiency ,and maximum interconnection wire length. The layout of CLA is highly regular when input output restriction, the addition of two n-bit numbers can be performed in time 0(log n).

III. CARRY LOOK AHEAD ADDER DESIGN

One widely known approach which employs the principle of carry look-ahead which solves the problem of delay in carry propagation by calculating the carry out in advance. This type of adder circuit is called as carry look-ahead adder. To add two binary numbers by using carry look ahead adders, we can save much computational time. CLA works on two signals Propagate(P) and Generate(G) signals for each bit position. Carry is generated when both the bit position is "1" and carry is killed in that position when either the input is "0". In most cases, P is simply the sum output of a half-adder and G is the carry output of that adder. P and G generate the carry out for every bit position. The signal for input carry C_{in} to output carry C_{out} requires an AND gate and an OR gate, which constitutes two gate levels. Fig 1 shows the CLA made up of using logics gates (XOR, AND & OR).

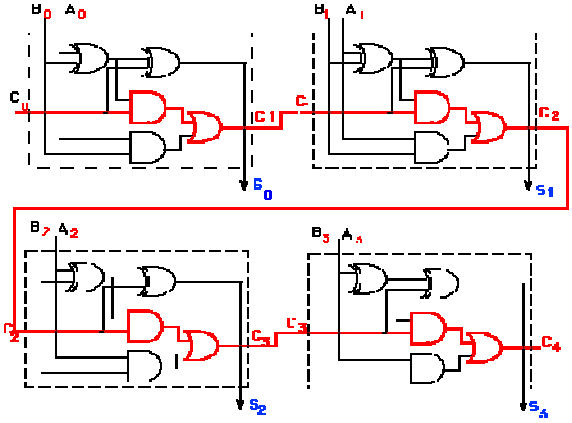

Fig 1. CLA using logic gates.

A. *DESIGN ISSUES*

The corresponding Boolean expressions are given here to construct a carry look ahead adder. In the carry look ahead circuit we need to generate the two signals carry propagate (P) and carry generator (G) as shown in equation (1) & (2). For sum and carry output equations are shown in equation (3) & (4) resp.

$P_i = A_i \oplus B_i$ (1)

$G_i = A_i \cdot B_i$ (2)

The output sum and carry can be expressed as

$S_i = P_i \oplus C_i$ (3)

$C_{i+1} = G_i + (P_i.C_i)$ (4)

Where i = 0,1,2…..n-1

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

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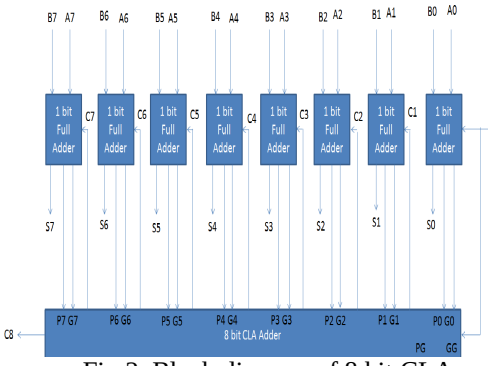

Fig 2. Block diagram of 8 bit CLA

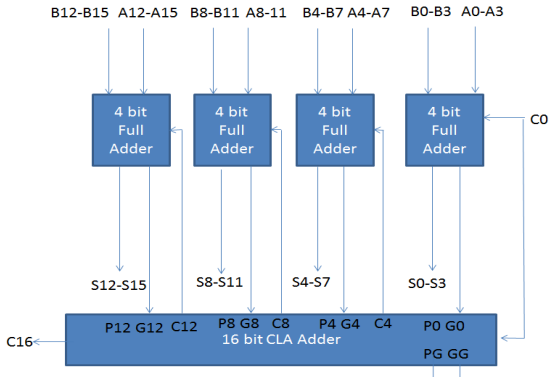

Fig 3. Block diagram of 16 bit

Fig 2 and Fig 3 shows the block diagram of 8 & 16 bit CLA which comprises of one bit full adders and four bit full adders respectively**.** The outputs of the full adder are carry propagate, carry generate and the sum of respective bits**.** And final carry is generated by CLA generator.

IV. DESIGN CONSIDERATION

The schematic circuit of the carry look ahead adder was drawn and debugging process had been carried out to ensure the design. The design of carry look ahead adder usably differs by the number of transistor used and circuit implemented with PMOS and NMOS circuits. Electric VLSI design system is used for layout designing that provide complete aids in designing the IC layout. It includes schematic editor, circuit simulator, schematic layout generator, layout editor, layout verification and parasitic extraction .Besides this LTspice IV was used for simulation work. It is a high performance spice simulator that includes a schematic capture and waveform viewer. It is used to simulate the output of both schematic and layout circuits.

TABLE I. MINIMUM WIDTH AND SPACING RULES

Layer	Type of Rule	Value
Poly	Minimum width Minimum spacing	2λ 2λ
Active	Minimum width Minimum spacing	3λ 3λ
Nselect	Minimum width Minimum spacing	3λ 3λ
Pselect	Minimum width Minimum spacing	3λ 3λ
Metal1	Minimum width Minimum spacing	3λ 3λ

There are some design rules that has to be followed to make an IC layout. This rule uses a universal parameter λ. Table I shows design rules for width and spacing.

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V. DESIGN AND EXPERIMENTAL DATA

The simulation studies involve the Fast Fourier Transform of Carry Look Ahead Adder. The layout designing is implemented here with electric VLSI design system software. In this we are comparing the results of 8 and 16 bit of CLA. Our result shows that SNR of CLA is high which is good for the system.
Design includes- First the layout design has been done on the Electric CAD software. After the layout has been done, the designed are checked with DRC i.e. Design Rule Check and ERC i.e. Electric Rule Check tools. After the DRC and ERC, we performed LVS i.e. Layout Versus Schematic which is used for checking the schematic and layout both. LVS is mainly used to check the compatibility between layout an d schematic. After that we performed FFT analysis of the carry result . The plot of the carryout is shown in the above Fig. 6 and Fig. 8. And FFT plot of the carry out is drawn for 8-bit and 16-bit is shown in the Fig.7 and Fig. 9.

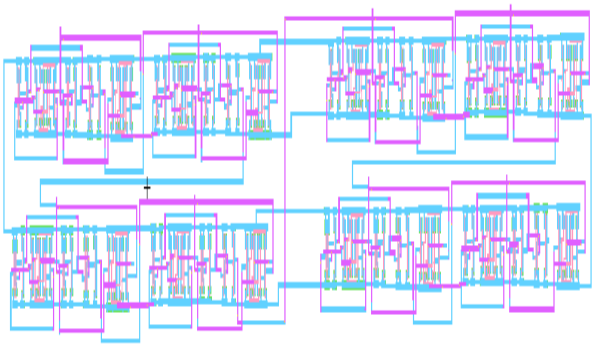

Fig 4. Layout designing of 8-bit CLA

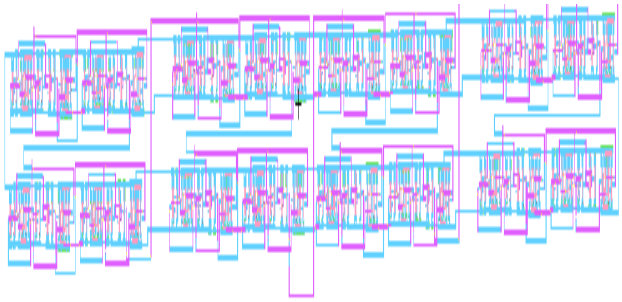

Fig.5 Layout designing of 16-bit CLA

Fig 4 and Fig 5 shows the layout design of 8 and 16 bit CLA. The layout design which is shown above has been done on the Electric CAD software.

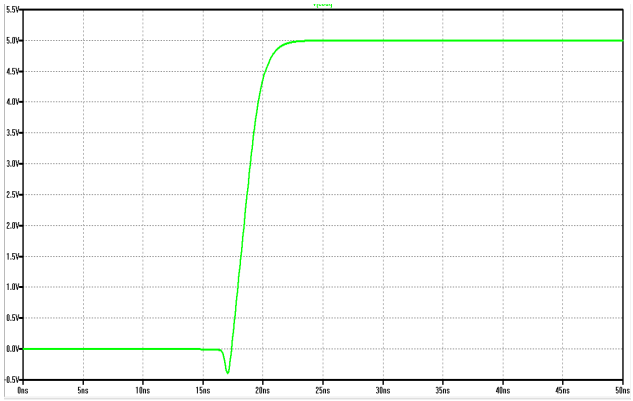

Fig 6. Simulation result of carry out of 8-bit CLA

Fig 7. FFT plot of carry out of 8-bit CLA

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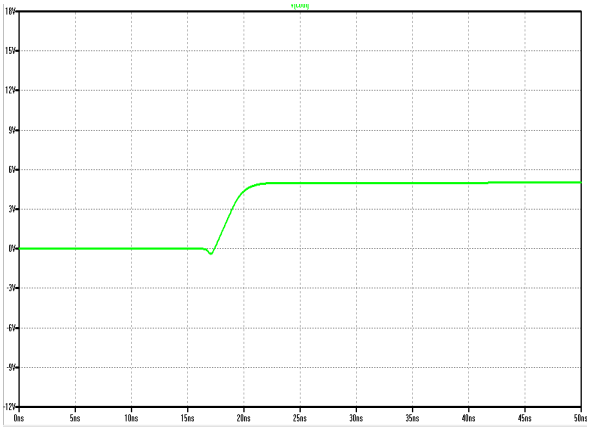

Fig 8. Simulation result of carry out of 16-bit CLA

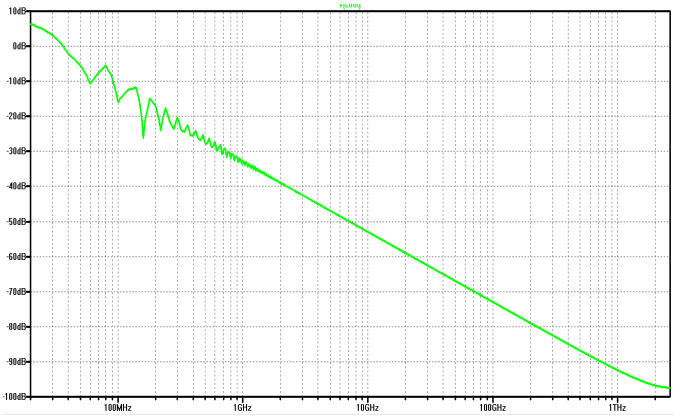

Fig 9. FFT plot of carry out of 16-bit CLA

The plot of the carryout is shown in the above Fig. 6 and Fig. 8 has been designed using LTspice IV software. And FFT plot of the carry out is drawn for 8-bit and 16-bit is shown in the Fig.7 and Fig. 9.

VI. METHODOLOGY

Defining the necessities and setting the requirements is an important thing in any Integrated Circuit. Theory to design scalable CMOS Adders and related design methodology is been described below:

Different adder circuits are elementary blocks in many present-day integrated circuits, which are not only employed to perform addition operations, but also some other arithmetic operations such as subtraction, multiplication and division. Half adder and Full adder are the examples of adders. Full adder is the basic building block of any adder circuit. Speed power and area are the three main design parameters for any adder circuit.

The applications of digital integrated circuit and logic design are available in our daily life, including Computers, calculators, video cameras etc. In fact, there always be requirement for high speed and low power digital products which makes digital design a future growing business. Adders are critical component of a microprocessor and are the core component of central processing unit. Furthermore, it is the core of the instruction execution portion of every computer. Adders comprise of combinational circuit which synthesizes of logic operations, such as AND, XOR, OR, and perform arithmetic operations, such as ADD and SUBTRACT.

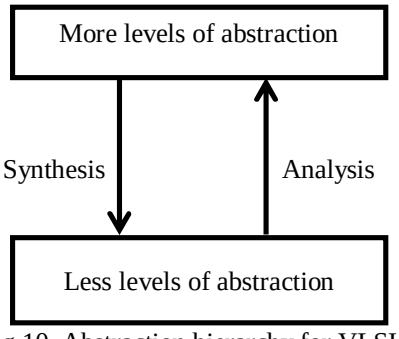

Fig 10. Abstraction hierarchy for VLSI adder1

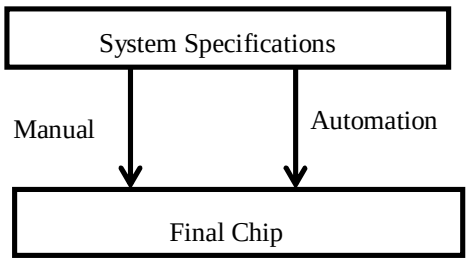

Fig 11. Abstraction hierarchy for VLSI adder2

Fig 10 and Fig 11 shows the different hierarchy for the designing of VLSI adders.
The design methodology is clear from following:

1. Defining the requirements and setting the specifications.
2. Design according to the Tool flow (EDA based).
3. Design of the Test circuits.
4. Simulating the Test results and optimization of the parameters

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The design methodology can be summarized as
1. Choosing the basic structure of the Adders.
2. Selection of the computational model using appropriate process technology.
3. Measurement and Optimization of Design parameters.
4. Our design methods usually differ by the number of abstraction levels and the complexities involved.

VII.RESULT

The transient and FFT analysis is done for 8 and 16 bit in terms of area and noise analysis. The proposed carry look ahead adder was designed using full custom method and surface area and SNR is calculated for both 8 and 16 bit CLA presented in the form of table below. And also enlist the values of magnitude, phase, & group delay in table III and table IV.

TABLE II. PERFORMANCE SUMMARY

Parameter	Presented Work	
	8-bit CLA	16-bit CLA
Surface area (in um^2)	1202	2412
SNR (in dB)	49.92	98.08

Table II shows the result of CLA in terms of surface area and SNR in dB. Area is calculated by the number of MOSFET used in designing of CLA.

TABLE III. ENLISTING FREQUENCY, MAGNITUDE, AND GROUP DELAY FOR 8-BIT CLA

S.no.	Frequency	Magnitude (in dB)	Phase	Group Delay
1	100 MHz	15.63	41.76	10.139 ns
2	1 GHz	-32.66	93.42	61.20 ps
3	10 GHz	-52.94	90.43	-1.97 ps
4	100 GHz	-72.97	93.44	1.833 ps
5	1 THz	-92.56	124.96	-95.20 fs

Table III shows the value of magnitude, phase, and group delay for 8 bit CLA for different frequencies i.e from 100MHz to 1THz.

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TABLE IV. ENLISTING FREQUENCY, MAGNITUDE, AND GROUP DELAY FOR 16-BIT CLA

S.NO	Frequency	Magnitude (in dB)	Phase	Group Delay
1	100MHz	-11.97 dB	46.38	9.23ns
2	1GHz	-32.45 dB	88.72	834.82ps
3	10GHz	-52.79 dB	90.52	2.98ps
4	100GHz	-72.85 dB	93.37	3.62ps
5	1THz	-92.26 dB	123.65	-141.7fs

Table IV shows the value of magnitude, phase, and group delay for 16 bi t CLA for different frequencies i.e from 100MHz to 1THz

VIII.ACKNOWLEDGEMENT

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IX.CONCLUSION

With the advancement in technology it has become possible to construct CLA of higher bits and to compute different parameters of CLA for different aspects. This paper presents the CLA for both the 8 and 16-bit. The CLA here is analyzed for two parameters i.e. surface area and SNR. The high value of SNR shows that the signal quality of the output signal is mostly free from noise and non-linearities. The higher the SNR, better is the signal quality at reception.

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