ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 10, October 2015

Noise Tolerant Current Mirror Footed Domino Logic

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ABSTRACT*:* Domino logic design is preferable for designing high performance circuits because of its high operationalspeed and less number of transistor requirement as compared to the static CMOS logic style. But this logic is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. A very small noise at the input of the dynamic logic can change the desired output of the circuit. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and consuming very less power as compared to other proposed circuit. In this paper we have proposed a novel circuit for domino logic named as current mirror footed domino logic which has less noise at the output node and has very less power consumption as compared to the basic domino footed and footless logic styles. Low unity noise gain (UNG) is achieved by using the current mirror footer and also reducing leakage current when PDN is not conducting.

KEYWORDS*:* Dynamic logic, domino logic, Delay, current mirror, noise tolerance, power consumption, robustness, technology scaling,

I.INTRODUCTION

The rapid advancement of VLSI circuit is due to the increased use of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled with technology. Due to larger number of devices per chip the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore noise pulses known as cross-talk can be generated leading to logic failure and delay of the circuit [1]. Again, when supply voltage is scaled the threshold voltage of the device needs to be scaled to preserve the circuit performance, which leads to increase in the leakage current of the device.

Due to high speed and low device count especially compared to complementary CMOS, dynamic-logic circuits are used in a wide veriety of applications including microprocessors, digital signal processors and dynamic memory [2]. Dynamic circuit contains a pull-down network (PDN) which realizes the desired logic functions. According to the basic theory, the dynamic logic circuit will precharge at every clock cycle. As the the clock signal frequency is high, the circuit is introduced with a lot of noise which consume extra power and slows the circuit.

In this paper, we have proposed a new C`MOS domino circuit technique, which can reduce the noise of dynamic logic dramatically. This circuit also increases speed and decreasesthe power dissipation of the circuit as compared to other domino logic styles. Section II demonstrates the basic footed and footless domino logic styles. Section III describes the proposed current mirror footed logic technique and its operation. Section IV shows the simulation result of the current mirror circuit. Section V compares the results of the proposed current mirror circuit with the basic footed and footless domino logic circuit techniques. Section VI concludes the paper.

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II. DOMINO LOGIC STYLES

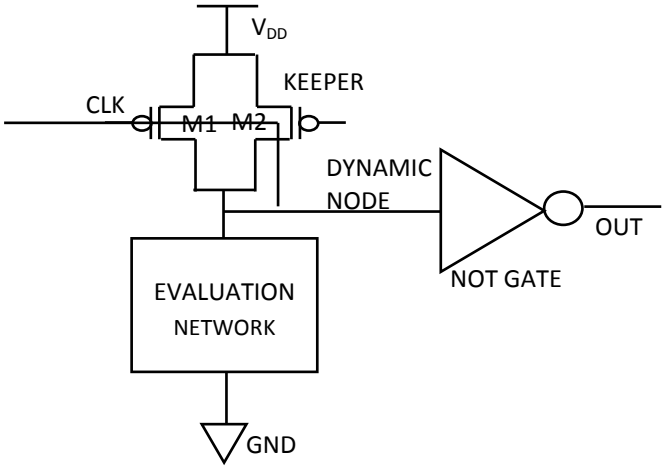

Fig.1 Basic domino footless logic

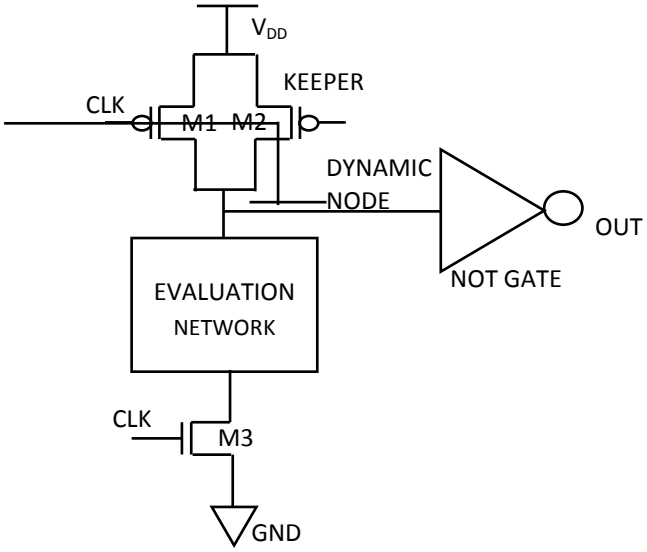

Fig.2 Basic domino footed logic

Fig. 1 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging PMOS gets ON and the dynamic node is connected to the V_{DD} and gets precharge to V_{DD}. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period, when all the inputs are at logic 0, the dynamic node should be at logic 1. But the wide fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the subthreshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at a gate input, the keeper may not be able to restore the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent upon V_{GS}. So in the presence of noise impulse the gate voltage increases, which leads to increase in V_{GS} and the dynamic node gets wrongly discharged.

To compensate the leakage current at the dynamic node a week transistor called keeper transistor is used. Keeper transistor prevents the charge loss and keeps the dynamic node at strong high when PDN is OFF. In the first domino

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proposal [3] the gate of the keeper transistor is tied to ground, therefore the keeper is always on. If at the beginning of evaluation the pull-down network (PDN) turns on, the dynamic node tends to discharge through the PDN. However, the keeper is injecting charge to the dynamic node as it is always on. This is called contention. Furthermore, a potential DC power consumption problem is generated. To alleviate the potential DC power consumption problem a feedback keeper was proposed in [4, 5].

Fig. 2 demonstrates the domino footed domino logic. This is the advances version of the footless domino as it contains a footer transistor in the circuit. This footer transistor acts as the stacking transistor. (Stacking effect - Subthreshold leakage current flowing through a stack of series-connected transistors reduces, when more than one transistor in the stack is turned off. This effect is known as the stacking effect).

As noise of domino gates is always more important in domino CMOS logic than the area, energy dissipation and delay issues, so recently several techniques have been proposed [6,7] to reduce the noise of dynamic circuits. All the techniques have reduced the noise sensitivity but there are many drawbacks with area, power dissipation and delay.

III. CURRENT MIRROR FOOTED LOGIC

The proposed current mirror footed circuit technique is illustrated in Fig. 3. In this circuit M_1 is the precharge transistor which inputs the clock signal (CLK). M_2 is the keeper transistor which prevents the charge loss and keeps the dynamic node at strong high when PDN is OFF. M_3, M_4, M_5 and M_6 are the four footer transistors which play a great role in making the circuit noise tolerant and consume lesser power as compared to the basic domino circuit techniques. The transistors M_3 and $M_4$are added to provide stacking effect to the circuit, which can reduce the leakage current during the evaluation phase. However, the evaluation delay of the circuit can be increased by increasing the size of the stack in the footer. To reduce this evaluation delay, a current mirror transistor (M_6) is added in parallel to the evaluation network of the current mirror footed domino circuit technique. Which can increase the discharging current the inputs is high. Transistor M_5 acts as a feedback path fromthe output node to the gates of current mirror M_4 and M_6. The source of M_5 is grounded. As a result, in presence of noises at inputs M_9 turns off the current mirror path and stops discharging the dynamic node.

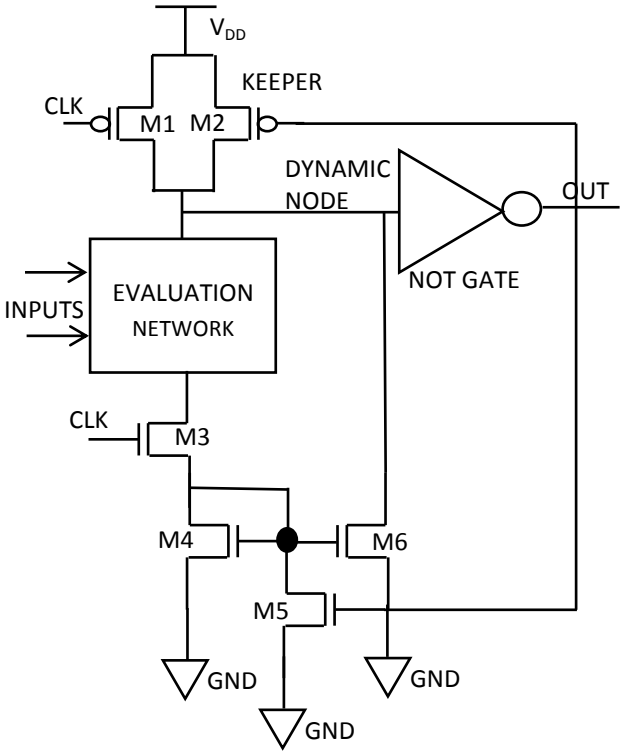

Fig. 3 Current mirror footed domino logic

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The proposed circuit worksas follows:

In the pre-charge phase, when the clock is low, the circuit is in the pre-charge mode, and the dynamic node gets pre-charge to high. When the footer transistor(M_3)is turned off a verysmall leakage current passes through M_4 pulling an eligible current from the dynamic node.

In the evaluation phase when the clock is high, this circuit show significantly improved noise immunity due to the stacking effect provided by the transistor M_4.

When the clock is high, if all the inputs are zero, the setwostacked NMOS transistors M_3 and M_4 substantially reduce the sub threshold current.

However, when at least one of the inputs switches to high, the mirror transistor pulls large current from the dynamic node resulting in a high to low transition on the dynamic node. In this case, output of the gate goes high turning on the NMOS transistor M_5 disabling the current mirror. For the rest of evaluation phase current mirror remains OFF.

IV. SIMULATED RESULTS

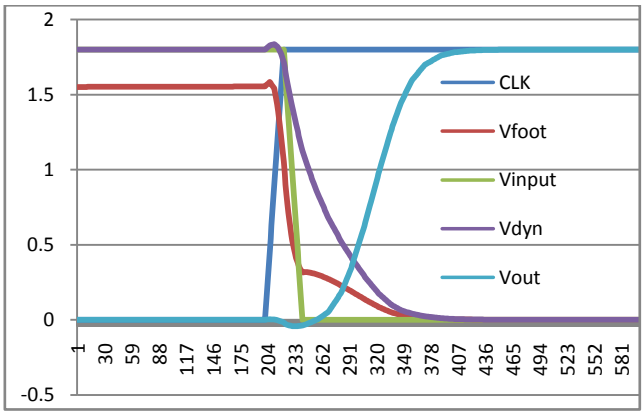

Fig. 4 Simulated waveform of proposed scheme

Fig. 4 illustrates the simulated waveform of proposed scheme. It includes the transient voltage waveform of CLK, footer voltage, input voltage, dynamic node voltage and output voltage. This is the simulated output in the evaluation period of the clock. In the evaluation period, when one of the inputs makes a transition from 1 to 0, the dynamic node also gets a transition from 1 to 0 and simultaneously the output changes from 0 to 1.

V. COMPARISON RESULTS WITH OTHER LOGIC TECHNIQUES

UNITY NOISE GAIN

Unity noise gain (UNG) describes a method of leakage measurement of the circuit. For robustness measurement, identical noise pulses were applied to all inputs in the evaluation phase, and the amplitude of the noise at the output of the static OR gates were measured as shown in Fig. 5. While applying noise pulses, the pulse were kept constant at 30 ps (typical gate delay at 180-nm technology) and the amplitude of the output noise was observed for different amplitudes of the input noise. The metric we used for leakage and noise robustness comparison is the unity noise gain (UNG), defined as the amplitude of the input noise that causes the same amplitude of noise at the output [15] UNG (2). We used a pulse noise to simulate cross-talk type of noise at the input. The effective noise depends on both the amplitude and duration of the noise pulse. The input noise level can be increased by increasing either the noise pulse duration or amplitude. In our experiments, we change the input noise level by changing its amplitude.

$$UNG = \{V_{noise}; V_{noise} = V_{out}\}$$

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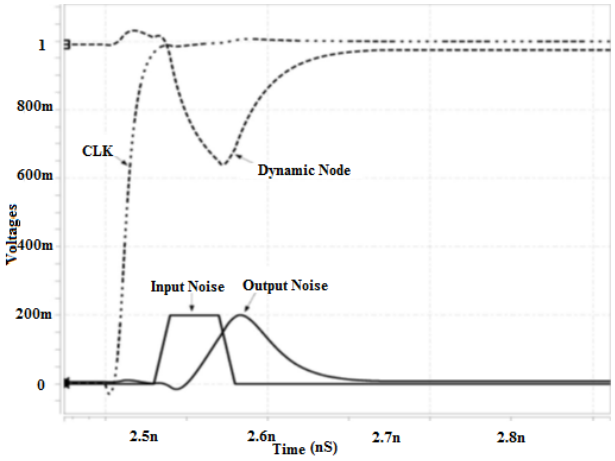

Fig. 5 UNG-delay curves for wide dynamic OR gates

Table 1 and Fig. 6 compares the UNG of the proposed circuit with the footed and footless domino circuits in tabular form and histogram form respectively. In both the cases the fan in of the OR gate varied from 2 to 32 and the UNG were calculated in the same environment for all the logics and found that the proposed current mirror is having high noise tolerance capacity as compared to the other two schemes. The circuits were being simulated with UMC 90 nm technology using cadence spectre. The simulated voltage is 1.8 V and the operational frequency is 200 MHz simulated in 27^{O}C.

Table 1 Unity Noise Gain Comparison with basic circuits under Same Delay (UNG Normalized To V = 1V)

Fan-in	Basic Domino Footless	Basic Domino Footed	Proposed Scheme
2	436	567	800
4	409	530	810
8	376	493	823
16	332	448	825
32	301	426	844

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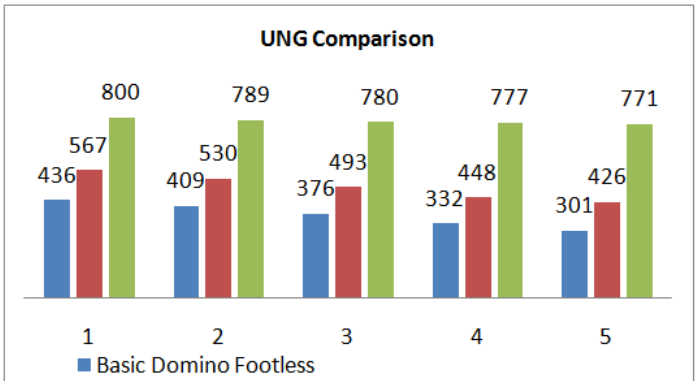

Fig. 6 UNG comparison under Same Delay (UNG numbers normalized to V = 1V) shown in histogram formfor OR gate varying from 2 input to 32 input

Table 2 UNG and performance measurement with different width of M6 for the proposed circuit at 90 nm technology for an input of 2

Width of M_6	UNG (normalized to V_{DD}=1V)	Power	Delay
0.12 um	800	1.34 E-8	3.11 E-10
0.18 um	795	2.55 E-8	2.66 E-10
0.24 um	796	2.61 E-8	1.75 E-10
0.30 um	791	2.78 E-8	1.79 E-10
0.36 um	790	3.12 E-8	1.65 E-10
0.42 um	790	3.22 E-8	1.50 E-10

Transistor M_6 plays a crucial role in terms of leakage and performance of gate in the proposed scheme. Its high width improves the performance by making the speed more but penalty paid is slightly less noise robustness and more power consumption. Table 2 shows the UNG, power and delay measurements for various widths of M_2 which was simulated with UMC 1.8 V and 90 nm technology. Table 3 demonstrates the powerdissipation for the proposed circuit and the basic domino circuits simulated for 2 input OR gate in 1.8 V with UMC 90 nm technology using cadence spectre. It shows that this scheme also reduces the power dissipation of the circuit dramatically.

Table 3 Power comparison for different circuit techniques simulated for 2 input OR gate

Logic styles	Power in um
Basic footless	93.9
Basic footed	40.6
Proposed	22.7

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VI.CONCLUSION

In this paper, a noise tolerant current mirror CMOS domino logic circuit technique has been proposed, which also have less power consumption. The simulation work was done with 180 nm and 1.8 V CMOS process. The results show that the proposed scheme is highly noise tolerant. It shows UNG i.e. unity noise gain nearly double to the basic CMOS domino circuits. Proposed circuit also shows less power consumption i.e. nearly 10 to 20 % of power saving as compared to the previous footed and footless domino logics. Also the circuit is flexible for wide variety of dynamic logic styles and adequate for large fan-in gates.

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