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Low power Design 6T SRAM Using Different Architecture

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ABSTRACT: This paper deals with the design and analysis of 1Kb Static Random Access Memory (SRAM) at 180nm, focusing on optimizing power and delay. In this paper two types of architecture is used to design SRAM, one is bank partitioning architecture and other is using matrix array. The key of low power operation in the SRAM is to reduce the word line capacitance and bit line capacitances. In memory bank architecture SRAM is divided into 4 blocks with each block having equal capacity of 256b.. The power dissipation is reduced to 78% in the circuit containing memory bank because in memory bank wordline capacitance and bitline capacitance are reduced as only one bank is selected at a time and all the other remain in standby mode at the expense of 6.930% more transistor count. Speed is also improved by 23% in the architecture containing memory bank. All the simulations are performed using IC flow tools at TSMC 180nm technology. The proposed memory circuit has applications in SoC and NoC.

KEYWORDS: 180 nm, low power, VLSI , enable decoder. SRAM

I. INTRODUCTION

Memory is an important part of computer and microprocessor based system design. It is used to store data or information in terms of binary number (0 or 1). Also data that is used in program as well as for executing the program are stored in the memory. Therefore memory is required for temporary as well as permanent storage of data in digital system. Generally memories are of two types (1) RAM and (2) ROM. ROM is also called as permanent memory as it is designed once, another way we can say that it is used only for reading purpose. While RAM is used for both read and write. RAM is again classified in two types SRAM and DRAM. Here in this paper SRAM memory is designed.

Since memory is an array type of structure, so cost per bit of the memory decreases with the cell area. For smaller memory cells, we can achieve larger storage capacity in the given silicon area. Hence the technology with the smallest feature size available should be used for the memory design. The aggressive technology-scaling trend is driven by the requirement of large amount of inexpensive memories for most of the computing and networking applications. CMOS is an excellent choice due to its superior noise margin, scaling capability, mature process, worldwide availability, and low cost and low static power consumption [5]. However, static power consumption is worsening with the scaling of the technology due to significant reduction in threshold voltages. Hence it is more challenging to design the low-power SRAMs in the technologies 0.18um and below since the SRAM consumes significant static power due to sub threshold leakage [15]. An SRAM is matrix of static volatile memory cells, and it addresses decoding functions integrated on-chip to allow access to each cell for the read and write functions. The basic architecture of the SRAM contains one or more rectangular arrays of memory cells with control circuitry to decode addresses for few basic and special operations.

II. ARCHITECTURE OF 1 KB 6T SRAM

The 1 Kb SRAM organizations is random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. Here two type of SRAM architecture is designed. One is simple architecture containing 5x 32 bit row and column decoder (Fig1) and other is bank partitioning based architecture. In bank partitioning based architecture entire SRAM is be divided into 4 blocks as shown in Fig 2, with each block is of 8 x 32

columns, where each word is 32 bits. Block decoder of 2 x 4 sizes is chosen to select one block at a time keeping rest of the block in ideal state. Depending on the address of 2
x 4 decoder one out of four 3 x 8 decoder becomes on and one can perform read and write operation in the bank connected to 3 x 8 decoder.

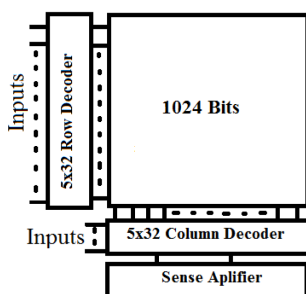

Fig 1:One Kb-SRAM Core

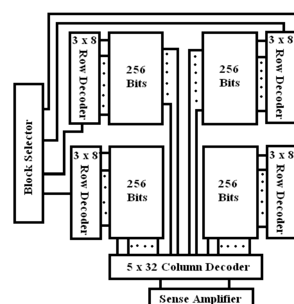

Fig 2: One Kb-SRAM Core Partitioning

III. TECHNICAL WORK PREPARATION

III(I). Cell and Core

SRAM cell contains two cross-coupled inverters forming latch and the two access transistor connecting these invertors to the complimentary bitlines to communicate with outside the cell. The access transistor is the NMOS transistors, As long as the access-transistors are turned off, the cell keeps one of its two possible steady states. The schematic of the SRAM cell is shown in

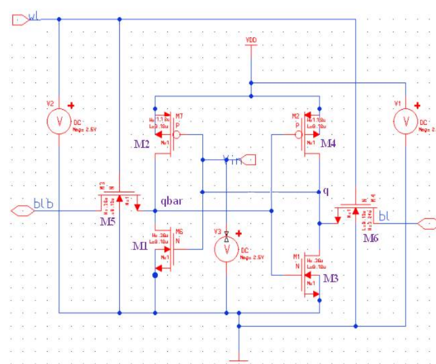

Fig 3: Six-T SRAM Cell

fig 3. In both read and write operation common word line (wl) signal controls the accessibility to the cell nodes q and qbar through two access transistors. Ideally all the cells are kept at low W/L ratio but a careful sizing is necessary to avoid accidentally writing a 1 into the cell. When word line is enabled for reading, the series combination of two NMOS transistor pulls down the BL' line to ground. For a small sized cell, the transistor sizing should be as minimum as possible. From the plot we got cell ratio should be greater than 1.0.

III(II) Sense Amplifier

The main function of the sense amplifier is to amplify the small voltage swing (voltage difference of bit lines) in large bit line, reduce delay, and power dissipation by reducing large voltage swing. The schematic of the differential voltage sense amplifier is shown in the fig 4

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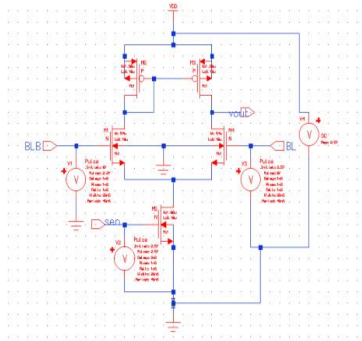

Fig 4: Differential Voltage Sense Amplifier [1]

This type of sense amplifier is used to improve noise immunity and speed of the circuit. Voltage swing on the bitlines is limited due to the large capacitances, so any noise on these lines may cause an error in the reading process. The differential voltage sense amplifier attenuates common-mode noise and amplifies The main function of the sense amplifier is to amplify a small analog signal differential voltage that developed on the bit lines blbar and bl by a read accessed cell to full swing digital output signal. When a difference is created between the bit lines, sense amplifier senses it and amplifies it to give the output.

III(III) 1 Kb 6-T SRAM Memory

The schematic of 1Kb SRAM without memory bank and using memory bank is shown below in fig 5 & fig 6. It contains four memory banks, each of having a capacity of 256 cells. At a

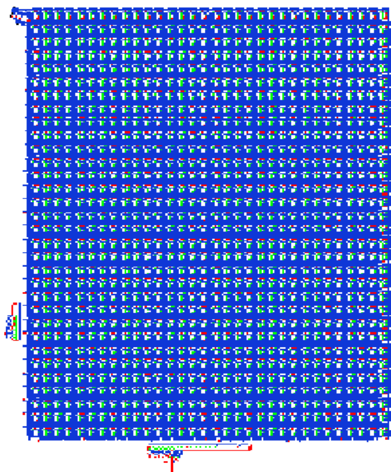

Fig 5: One Kb SRAM without Memory Bank

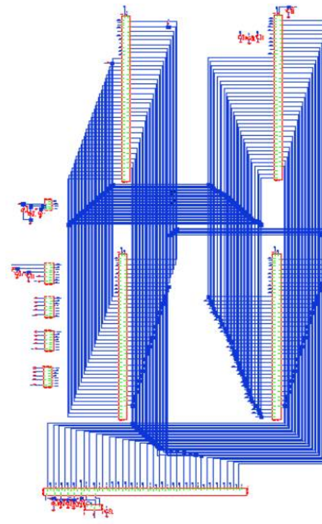

Fig 6: One Kb SRAM with Memory Bank

time, only one memory bank is selected depending upon the address of block selector. When the bank is selected, memory cell can be accessed depending upon the address of row and column decoder. The power consumption is decreasces why memory bank is used in SRAM. This is cause of one bank is enabled ,at that time all the other remaining blocks are at n standby mode.

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S.No.	Component	Transistor Count	
		Without Memory Bank	With Memory Bank
1.	Precharge Circuit	96	384
2.	Sense Amplifier	160	640
3.	Decoder	420	668
4.	1 Kb SRAM	6146	6146
	Total	6822	7838

Table 1: Transistor count in 1 Kb SRAM

The main source of power consumption in SRAM cell is bitlines and wordlines. In bank partitioning the capacitance along the word lines and bit line reduces so power dissipation also reduces.

IV. RESULT AND DISCISSION

PARAMETER ANALYSIS OF SRAM CELL

IV.I Simulation result of SRAM Cell

In figure 7 simulation result of SRAM cell shown , to write data 1, write signal is asserted and the word line is pulled high, the q node starts to rise to vdd

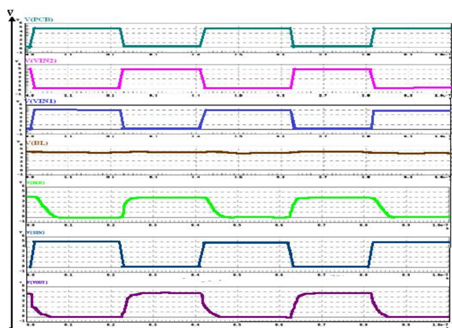

Fig 7: Simulated Waveform of 1 k b SRAM with Sense Amplifier

while the qbar node starts dropping down to gnd. When data is written in SRAM cell the precharge circuit become on, which is initially in off state and the voltages on the bit lines blbar and bl become equalized. Read operation starts by disabling the pre-charge circuit and enabling the word line 'wl' which causes the bit line blbar to decrease at a linear rate while the other bit line bl to remains at high value i.e. constant
that is shown in the waveform.

IV(I).II(a). Static Noise Margin

SNM quantifies the amount of voltage noise required at the internal nodes of a bit line to flip the cell's content. SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS devices.

The noise voltage at which the nodes voltages change the cell logic states is known as static noise margin of the cell, and can be taken as the relative cell DC noise margin. After simulation of the SRAM

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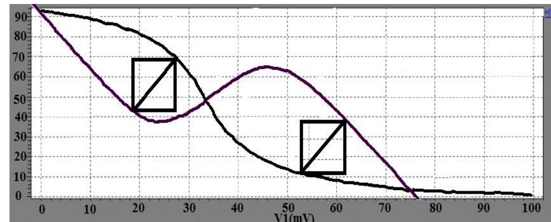

Fig 4.2: butterfly curve for SNM

cell, we will get figure above. Practically we can't get butterfly structure so the graph is rotated according to x-y coordinates just like a figure given below to get butterfly structure .Since by knowing the diagonals of the maximum embedded squares we can calculate the sides. The squares have maximum size when the lengths of their diagonal D1 and D2 are maximum the extremes of this curve correspond to the diagonals of the maximum embedded squares.

SNM = side of the smaller of the two maximum squares embedded inside the loops of the SRAM cell's transfer characteristic.

$$SNM= D/ \sqrt{2}$$

IV(I)II (b). Data Retention Voltage (DRV)

Data Retention Voltage (Vdr): Min. power supply voltage to retain high node data in the standby mode. There are two nodes (q and qbar) of the SRAM cell for storing value either 0 or 1. Then decrease the power supply voltage until the flip the state of SRAM cell or content of the SRAM cell remain constant. When Vdd scales down to DRV, the Voltage Transfer Curves (VTC) of the internal inverters degrade to such a level that Static Noise Margin (SNM) of the SRAM cell reduces to zero. So Data Retention Voltage is 0.6V as shown in the fig4.6.

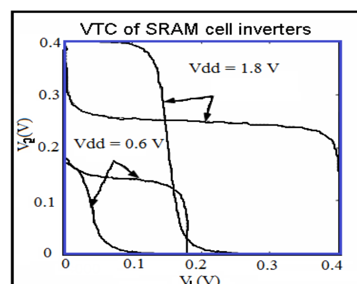

Fig: 4.3 Waveform for DRV

IV(I)II (c). Read Margin (RM)

Based on the VTCs, we define the read margin to characterize the SRAM cell's read stability. We calculate the read margin based on the transistor's current model. Experimental results show that the read margin accurately captures the SRAM's read stability as a function of the transistor's threshold voltage and the power supply voltage variations. The static read margin is preferably greater than the static write margin

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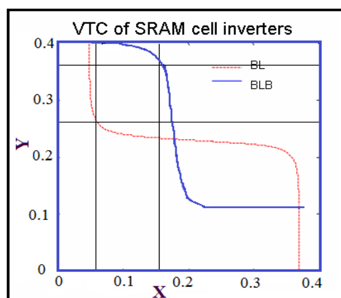

Fig 4.4: Waveform for Read Margin

IV(I)II (d). Write Margin (WM):

Write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell. The

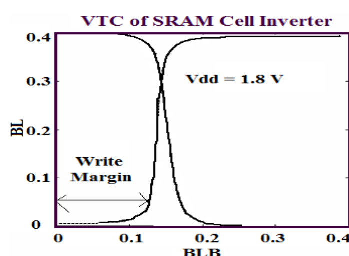

Fig4.5: Waveform for Write Margin

write margin value and variation is a function of the cell design, SRAM array size and process variation. Write margin is directly proportional to the pull up ratio. Write margin increases with the increases value of the pull up ratio. So be carefully you have to design SRAM cell inverters before calculating the write margin of SRAM cell during write operation. Pull up ratio is also fully depends on the size of the transistor. Parameter of SRAM cell is listed below in table 4.1

Parameter	Value
Technology	180nm
Vdd	1.8
SNM	200mV
DRV	0.6 V
Write Margin (WM)	0.446V
Read Margin (RM)	0.327V

Table 4.1: Parameters of SRAM Cell

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S.No.	Vdd	Without memory bank		With memory bank	
		Power(mW)	Delay(nS)	Power(mW)	Delay(nS)
1	1.8	9.0475	21.981	1.0909	13.298
2	2.0	14.6818	17.265	2.2124	10.986
3	3.0	62.9057	12.351	4.6871	9.010
4	4.0	143.6574	10.174	9.4112	7.935
5	5.0	258.156	8.869	16.3612	5.470

Table 4.2: Comparison of Power and Delay between containing 1Kb SRAM memory bank and without memory bank with varying Supply Voltage

IV(II) Sense Amplifier Parameter Analysis

Speed of sense amplifier increases when corresponding vdd increases but power dissipation also

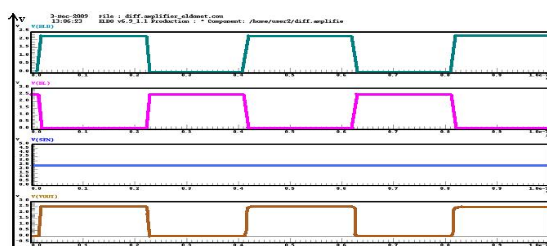

Fig 4.6: Simulated Wave form of Sense Amplifier

increases. When we increases threshold voltage of input transistors then corresponding delay are also increases. The main reason of power consumption during high vdd is the time window of transition

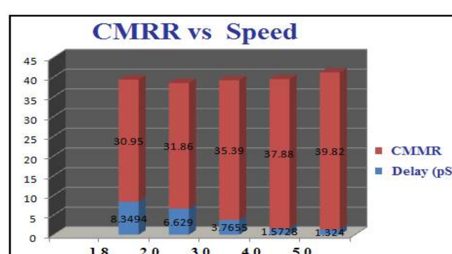

Fig 4.7: Increases of Speed wih increases of CMMR

region are large so device found more time to short between Vdd and ground. It will be computed from the formula P= CV2F. In the case of CMRR it value should be high for any amplifier. Same thing is also applicable for sense amplifier. Speed of sense amplifier increases when CMRR increases. The reason behind that better CMRR helps to suppressed common mode signal.

V. CONCLUSION

For SRAM cell we have calculate SNM, DRV RM and WM. Architecture containing banks have less power dissipation and high speed at the expense of 6.930% more transistor count as comparison to architecture without memory bank. In memory bank architecture power consumption is less. The reason behind that, at a time only one

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memory bank is enabled and other banks remain in standby mode Use of sense amplifier also have good impact on power consumption.

Until recently, the 6T cell architecture was reserved for niche markets such as military or space that needed high immunity and low power components. However, with commercial applications needing faster SRAMs, the 6T cell may be implemented into more widespread applications in the future. Much process development has been done to reduce the size of the 6T cell.

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