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# Design and Simulation of Low Power Full Adder using Footed Diode Domino Logic

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**ABSTRACT**: In this paper a new technique to reduce power dissipation for domino logic circuits has been projected. In this paper a diode is put on the foot of 1-bit full adder domino logic circuit which develop the power reduction as compared to projected and conventional 1-bit full adder domino logic. NMOS as a diode is used and due to the extra diode, in precharge stage leakage current get reduce this is because of the Stacking Effect. For simulation we were using Cadence Spectre tool at 180nm CMOS technology. Comparison between conventional & proposed logic styles has been done. The result of simulations shows an improvement of 58% and 38% power as compared to the standard conventional full adder domino & full adder using pseudo domino logic.

**KEYWORDS**: Full Adder, Domino Logic, Cadence, Spectre, Footed Diode, 180 nm technology.

## I. INTRODUCTION

Dynamic circuits are very useful in circuit design to reach higher speed, smaller area and potentially lower power consumption due to fault-free operation. There are many difficulties in designing and verifying this class of circuits. Low power circuits mainly deals with power saving. Domino logic circuits are more power efficient and comparatively faster, because these circuits have half the transistor count with respect to the complementary static circuits.

Low power and high speed logic design circuits [5] continue to get more attention in consideration of product manufacturing. In today's world power saving has become very important than all other aspects. Dynamic logic circuits came into the picture because of its power efficient circuitry. Domino logic circuits are more power efficient and mutually faster, Domino logic is basically a dynamic logic circuit followed by an inverter. The clock signal is used to control the operation of domino logic circuit [6]. The domino logic circuit consist of two phases. The first phase, when Clock is low(0), is called the precharge phase and in the second phase, when Clock is high(1), is called the evaluation phase [6]. In the initial phase, the output is driven high thoroughly (no matter what is the values of the inputs) because the transistor at the bottom is turned off, so it is impossible that the output to be forced low during this phase. During the evaluation phase, Clock is high, and the transistor in the bottom is turned ON.

## II. RELATED WORK

### Conventional domino logic

Conventional domino logic consists of a dynamic gate followed by a static inverter. Generally, the dynamic gate used is of n-type and called pull down network. The logic gate operated under two conditional phases called pre-charge phase & evaluation phase respectively. Clock signals are used to control the operation of domino logic circuit, when the clock pulse goes high the logic circuit is operating under the evaluation phase and when the clock pulse goes low then it operates under pre-charge phase. Under pre-charge phase when clock is low, PMOS Ml is on and a dynamic node named as Z is charged up to VDD. During evaluation phase clock NMOS transistor M2 is on and PMOS Ml is off .So it is up to input combination whether the node Z is isolated from ground or not. In evaluation phase when input combination is high then dynamic node Z is directly connected to ground so it will discharge to zero [8].

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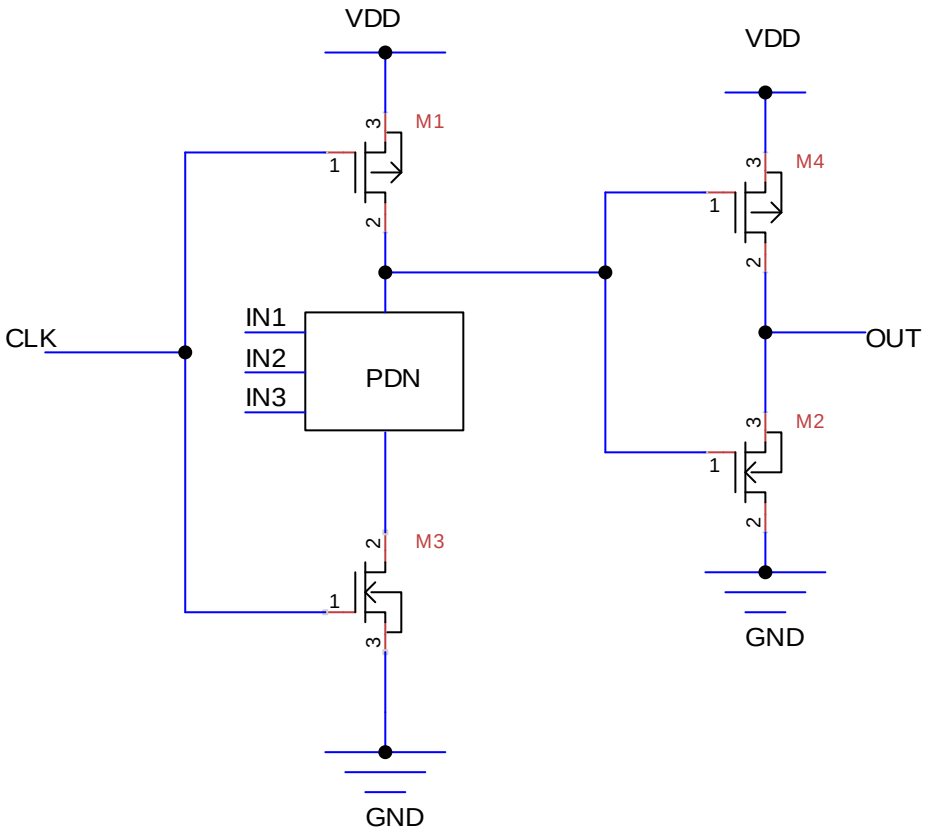


Fig.1. Conventional Domino Logic

**PSEUDO DYNAMIC BUFFER BASED DOMINO LOGIC**

In conventional domino logic more power is dissipated, to overcome this problem Pseudo dynamic buffer based domino logic has been introduced. There are two phases in PSEUDO dynamic based domino logic:-

• Evaluation phase- in this phase when clock pulse is kept high then the PMOS transistor Ml is turned off and NMOS transistor M2 is turned on so, the dynamic node Z discharge through node B that's why output node became high(one).

• Pre-charge phase- in this phase when clock pulse is kept low(zero) then the NMOS clock transistor M5 becomes on and dynamic node Z gets charged to VDD• The output is still high because the clock pulse turns off the transistor M2 so output node is not able to discharge.

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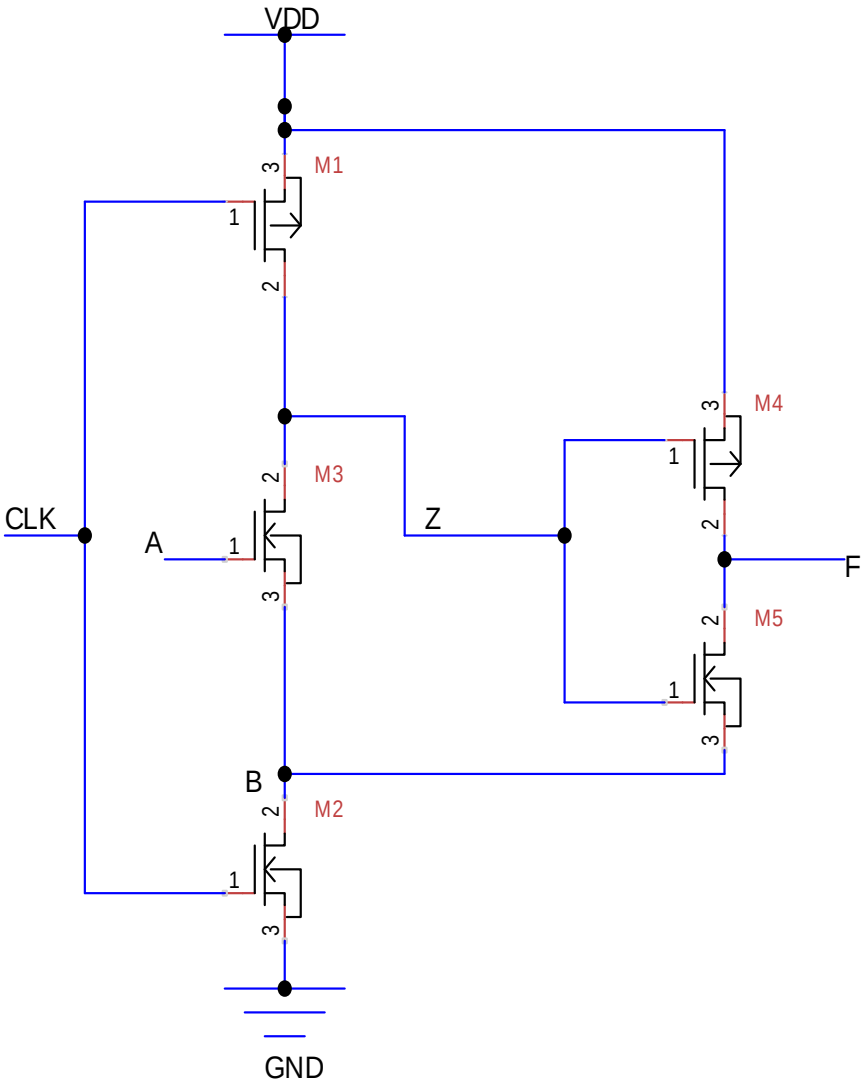


Fig.2.Pseudo dynamic buffer based Domino Logic

**FOOTED DIODE DOMINO LOGIC**

In the projected circuit NMOS transistor is put in the foot of the circuit which work like a diode in between GND and M2 clock transistor. In the circuit shown in the fig.3 the source of the NMOS transistor M5 is connected to the node B rather than the GND. An NMOS transistor which works like a Diode is introduced in the circuit whose gate is shorted with drain and connected with the source of the NMOS clock transistor M2, the source of NMOS transistor M6 is connected to GND. In this circuit when input A is low then dynamic node Z is always charged high and output is kept low indifferently of operating phase.

When input A is high then the circuit operates under two phases that are pre-charge and evaluation.

• Evaluation phase- in this phase when the clock pulse is kept high then the PMOS transistor M1 is turned “OFF” and NMOS transistor is turned “ON” as the result, the dynamic node Z discharge through node B and for this reason output node became high.

• Pre-charge phase- in this phase when the clock pulse is kept low then the NMOS clock transistor M5 is turned “ON” and dynamic node Z get charged to VDD• The output is still high because the clock pulse turns off the transistor M2 so that the transistor M6 is also off and therefore output node is not able to discharge. Due to “Stacking Effect” power is compensated.

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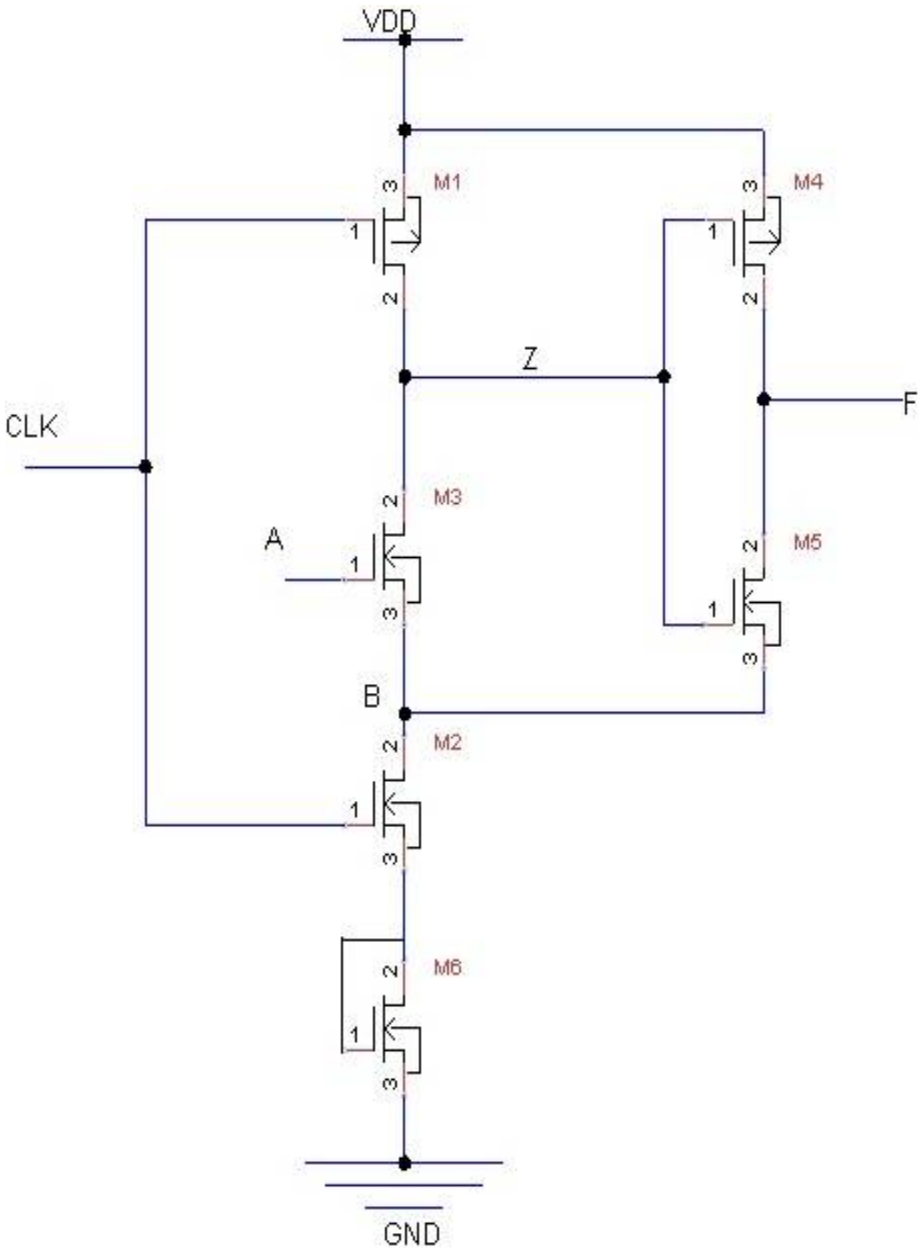


Fig.3.Footed Diode Domino Logic

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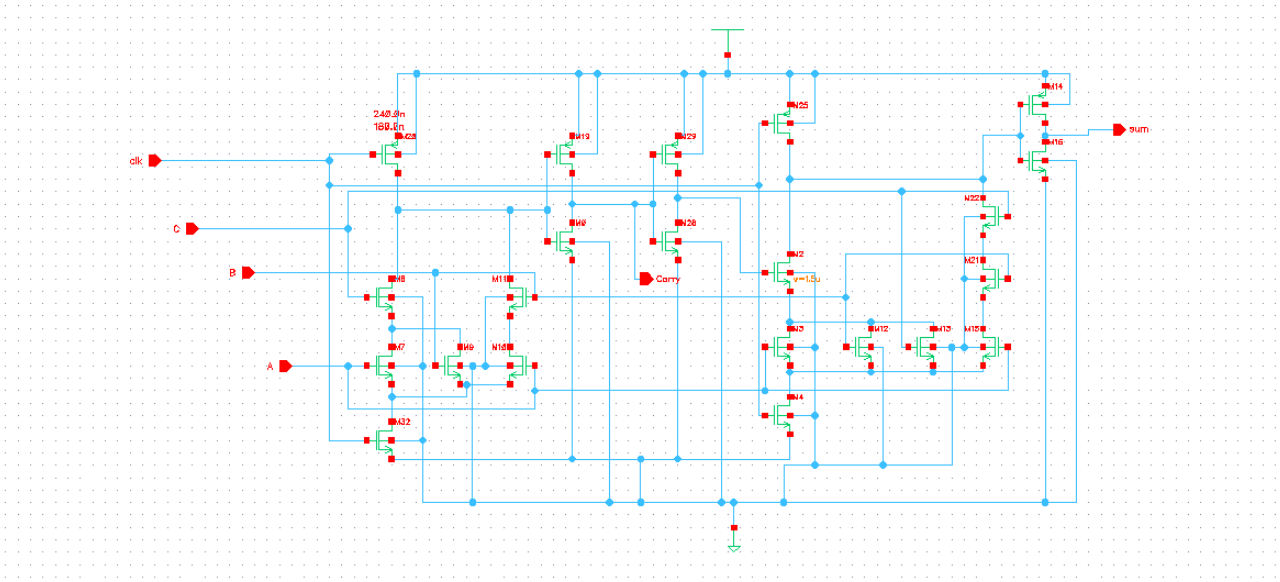
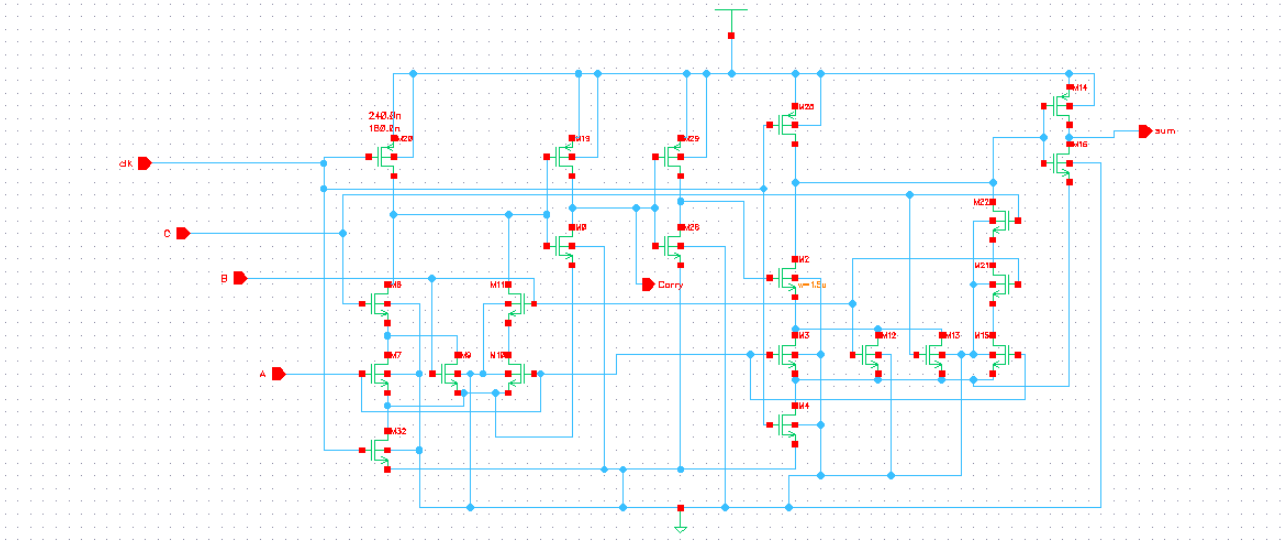
## III. PROPOSED WORK

**Full Adder Using Conventional Domino Logic**




full adder design by using domino logic consisting of dynamic gate followed by an inverter.

**Full Adder Using Pseudo Dynamic Based Domino Logic**




In the proposed domino logic, the pre-charge pulse is prevented from propagating to the output node of the buffer, resulting in a decreasing power consumption in the Output stage of the domino gate.

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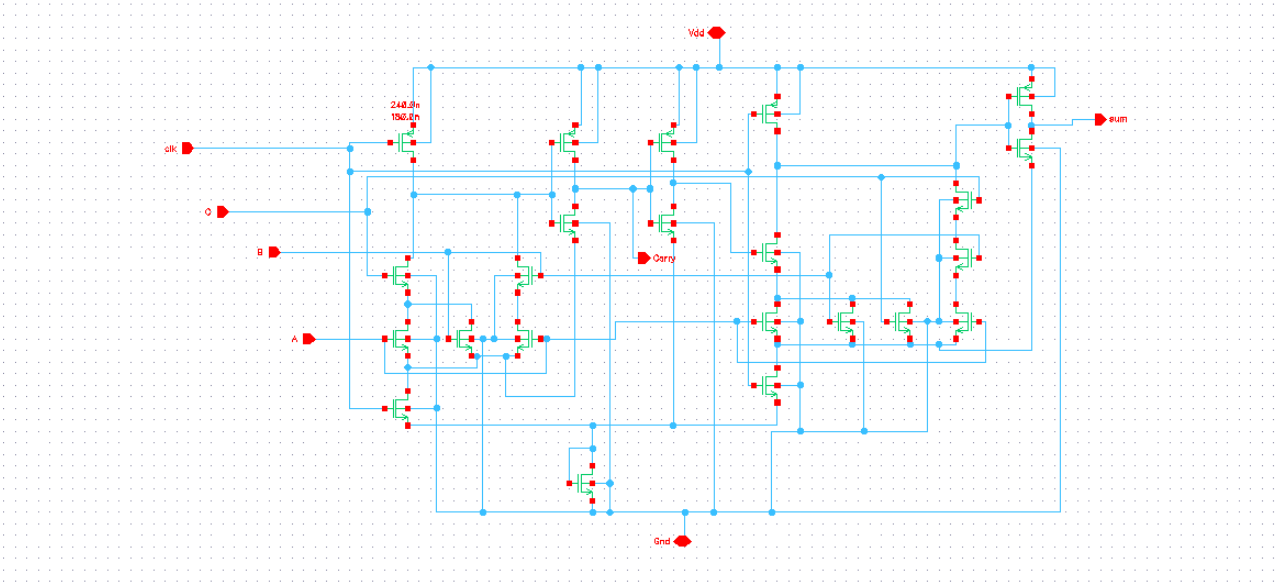


Performance degraded in a circuit is due to propagation of pre-charge pulse from dynamic node to the output node. The PDB based design for domino logic compensates this problem up to some extent but there is always a room for improvement. One NMOS was introduced in the foot whose gate and drain is shorted this phenomenon is known as stacking effect by which the leakage current becomes low so that the power dissipation also become low.

## IV. SIMULATION RESULTS

The performance of the projected work has been evaluated using 180nm standard CMOS technology. In order to show the power saving of our proposed circuit design, simulation was performed using cadence spectre simulator for 180nm standard CMOS technology.

| PARAMETER'S | Conventional Domino Full Adder | Pseudo Based Domino Full Adder | Footed Diode Based Domino Full Adder |
|---|---|---|---|
| Power consumption (μ W) | 29.91E-6 | 20.46E-6 | 12.56E-6 |
| Sum Delay (p s) | 116.4E-12 | 87.67E-12 | 24.63E-12 |
| Carry Delay (p s) | 89.38E-12 | 74.87E-12 | 13.1E-12 |

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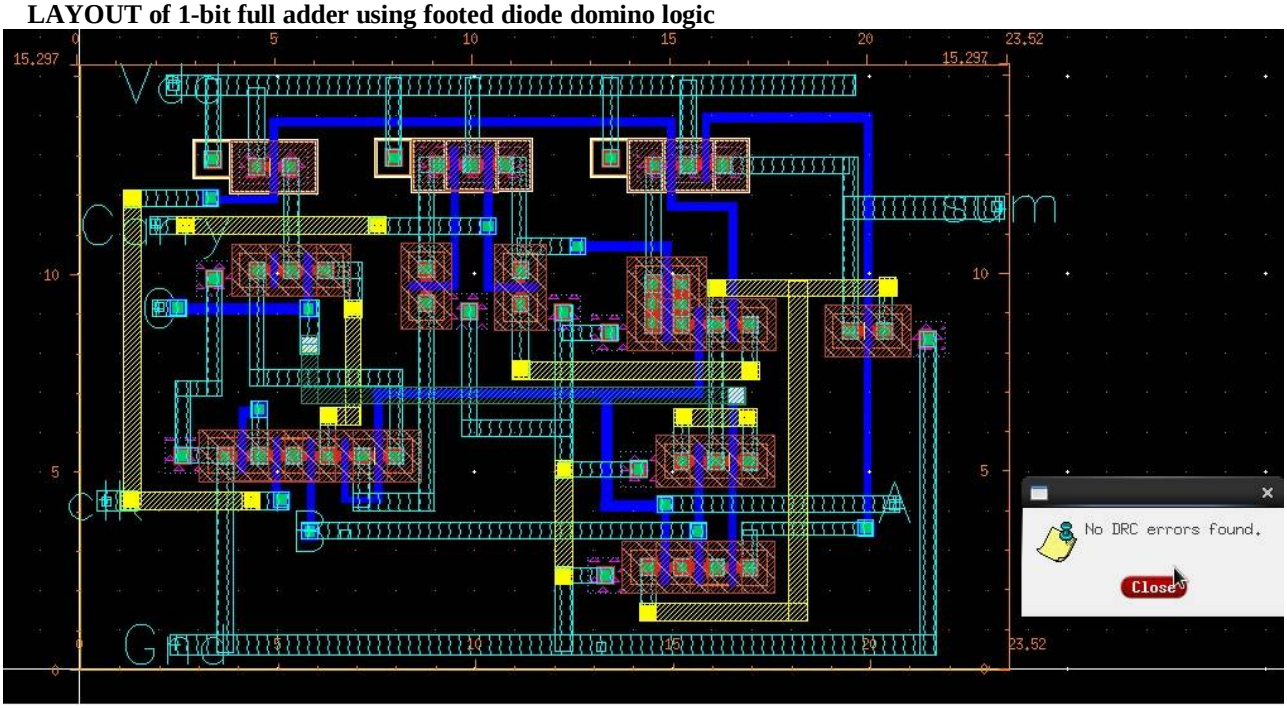
**LAYOUT of 1-bit full adder using footed diode domino logic**




As the result shows there is no DRC (Design Rule Check) error.

## V. CONCLUSION AND FUTURE WORK

As the conventional and PDB techniques have number of drawbacks like more power consumption, increased leakage current, noise problem, pre-charge pulse propagation and more delay, a novel technique called Footed Diode Based Domino Technique is introduced. The projected work shows the power consumption comparison between our proposed logic styles with convention logic design techniques and Pseudo based domino logic at 180nm standard CMOS technology. Footed diode based Full Adder can be used in many Digital circuits.

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