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Characteristics of AlGaN/GaN HEMT with P-Type GaN Gate and AlGaN Buffer

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ABSTRACT: Here we present a 1.5 ampere normally-off GaN transistor for power applications in p-type GaN gate technology with a modified structure. A higher threshold voltage is achieved while keeping the on-state resistance low by using an AlGaN buffer instead of a GaN buffer. P-GaN gate GaN transistors with AlGaN buffer therefore yields higher breakdown voltages as compared to standard GaN buffer. The impact of gate metal work function on the gate current of P-GaN gate HEMT is studied with TCAD device simulation.

KEYWORDS: AlGaN/GaN, P-GaN, Breakdown Voltage, Threshold Voltage, Confinement.

I. INTRODUCTION

GaN Based High electron mobility transistors are used in the field of high power electronics because of their superior properties, such as high switching frequency, high break down voltage, high mobility and good thermal stability [1-3]. For conventional AlGaN/GaN HEMT structure, Two Dimensional Electron Gas (2-DEG) exists in interface of GaN due to strong built in polarization electric field in the AlGaN/GaN hetrostructure [1]. The 2-DEG cannot easily depleted by the shottky gate contact at zero bias. Such a depletion mode behavior excludes GaN based transistor from most power electronics applications. In order to achieve enhanced mode HEMT [2], several technologies have been developed to raise the conduction band energy level underneath the gate contact to obtain a positive threshold voltage. For instance P-GaN [3,4] cap layer on the top of AlGaN barrier depletes the 2DEG carrier in the channel. In this paper, AlGaN/GaN Double Heterojunction High Electron Mobility Transistors (DH-HEMTs) with an AlGaN buffer layer [5] is presented, which leads to a higher potential barrier at the backside of the 2-DEG channel and better carrier confinement. This remarkably reduces the drain leakage current and improves the device breakdown voltage [5-7]. The breakdown voltage of AlGaN/GaN DH-HEMTs is significantly improved compared to conventional lGaN/GaN HEMT. In the conventional AlGaN/GaN HEMT structure, the 2-DEG induced by spontaneous and piezoelectric polarization is confined in an approximately triangular potential well formed at the interface between the AlGaN barrier and GaN buffer. However, due to the lower potential barrier height of the GaN buffer layer, also known as the insufficient confinement of the 2-DEG in the channel, it is easy for the 2DEG to overflow from the potential well into the GaN buffer layer, thus causing a buffer layer punch through effect and deterioration of the characteristics[7].

II. STRUCTURE

The device is an AlGaN/GaN/AlGaN Hetrostructure which is made on a Silicon Carbide (SiC) substrate. SiC is preferred over Si and Sapphire as substrate for GaN based structure [8,9]. The layers are composed on the SiC ubstrate. The first layer is a 1 µm thick AlGaN buffer formed with a carrier concentration of 1×1013 cm-3 and the mole fraction of Al is 5%. The AlGaN buffer layer acts as a back-barrier and suppresses source-drain punch-through currents in the off-state [10]. The next layer is a 10 nm GaN channel which is form with doping concentration as small as 1×109 cm-3. Above the channel, we form a spacer layer of AlGaN, with a thickness of 2 nm. This spacer layer is undoped and the mole fraction of Al is 20%. On the top of this spacer layer, we form a 13 nm AlGaN barrier layer with high doping of 5×10 16 cm-3 and mole fraction of Al is 20%. To keep the device off in the normal condition, we form a 100 nm P-aN cap layer with very high doping of 1 × 10 17 cm-3. The spacing between gate to drain is 10 µm, source to gate is 2 µm and gate length is 3 µm.

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III. SIMULATION AND RESULTS

This proposed device is simulated with TCAD Silvaco and results are presented below[11].

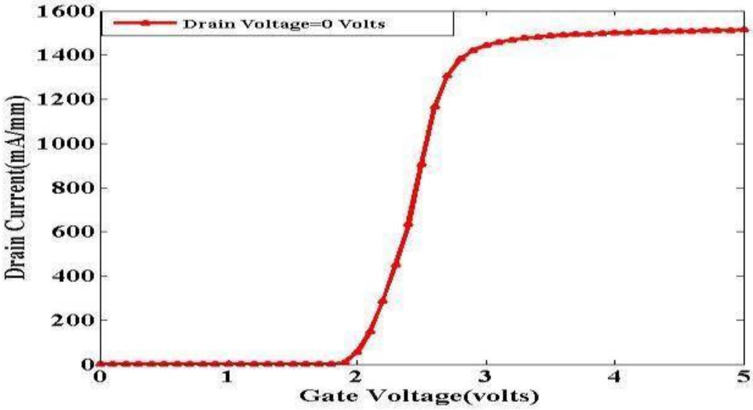

Fig 2: Drain Current vs Gate Voltage characteristics

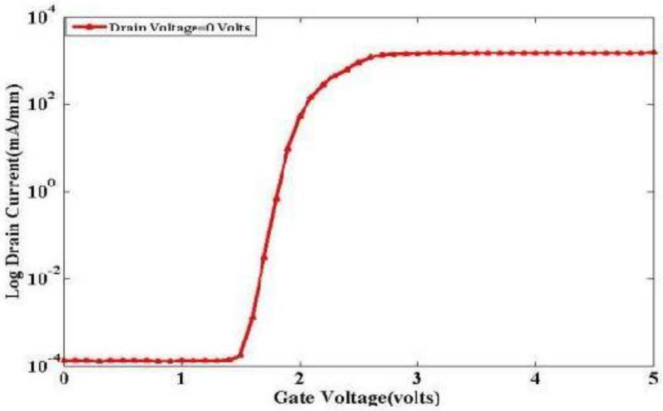

Fig 3: Logarithmic Drain Currentvs Gate Voltage

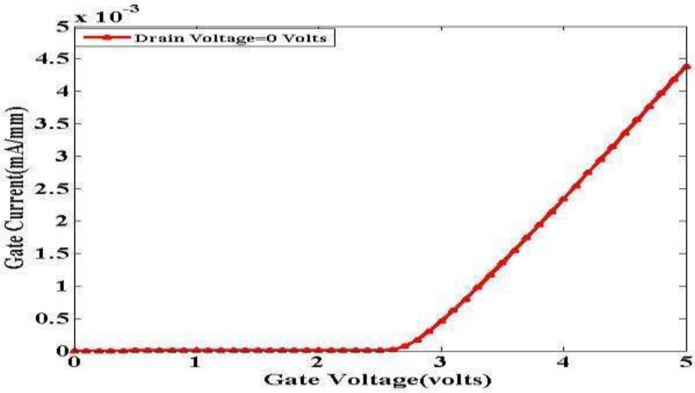

Fig 4: Gate Current vs Gate Voltage characteristics

Fig 2 above shows the variation of drain current with respect to gate voltage, when drain voltage is 0 volts. The device exhibited normally off operation with a threshold voltage of ~2 volt and maximum drain current 1500 (mA/mm). We have used P-GaN to make our device normally-off. In Fig 3, we observe Ion/Ioff ratio is about 107 for the device. Fig

4 shows the variation of gate leakage current with respect to Gate voltage and it comes out to be 0.0045 mA/mm which is fairly low. In this measurement, the positive gate bias corresponds to a reverse-bias condition at the junction between the Schottky gate metal and the P-GaN layer. In Fig 5 drain current is plotted against gate voltage for different P-GaN Cap layer thickness. When thickness of P-GaN cap layer increases, the threshold voltage increases accordingly but the maximum drain current is always constant

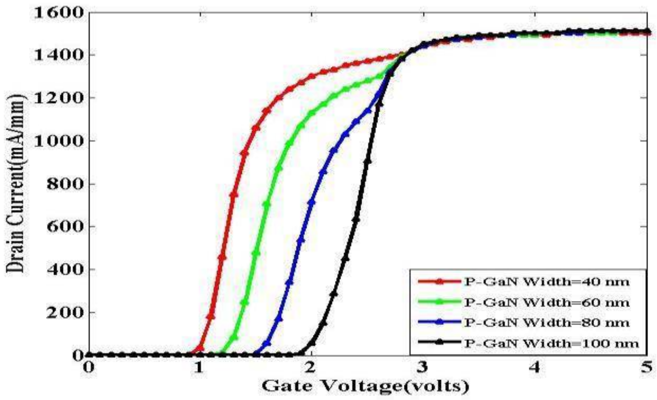

Fig 5: Variation of Drain Current with variation in P-GaN width

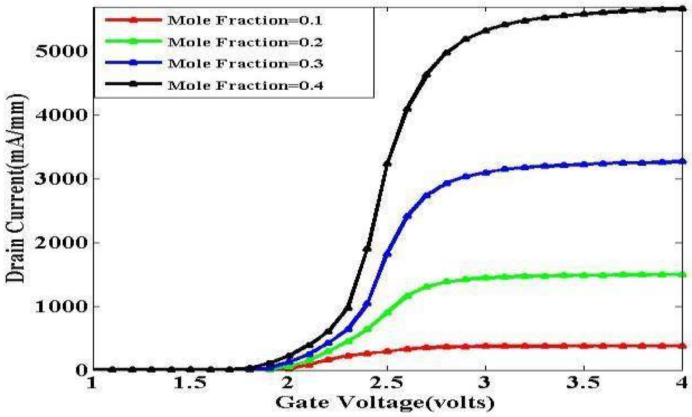

Fig 6: variation of Drain Current with variation in MoleFraction of Al in AlGaN barrier layer

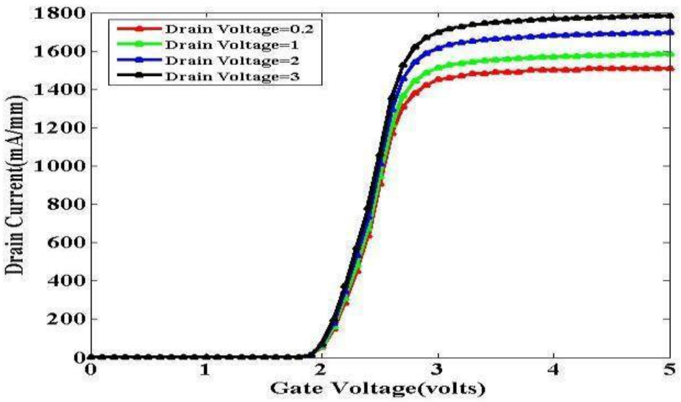

Fig 7: variation of Drain Current with variation in Drain voltage

Fig.6. shows the variation of Vth and drain current with different mole fractions of AlGaN barrier layer. High Al content in AlGaN barrier layer results in Poor transport properties. However, it increases 2-DEG density as well as breakdown field. We observe that as the mole fraction increases, Vth will decrease and drain current increases. The effect of different applied drain voltage on drain current is shown in Fig 7. When drain voltage increases, the maximum drain current also increases with respect to gate voltage but Vth is constant. Fig 9 shows the effect of Polarization in the AlGaN-GaN interface. When the polarization increases, then Vth decreases and current increases.

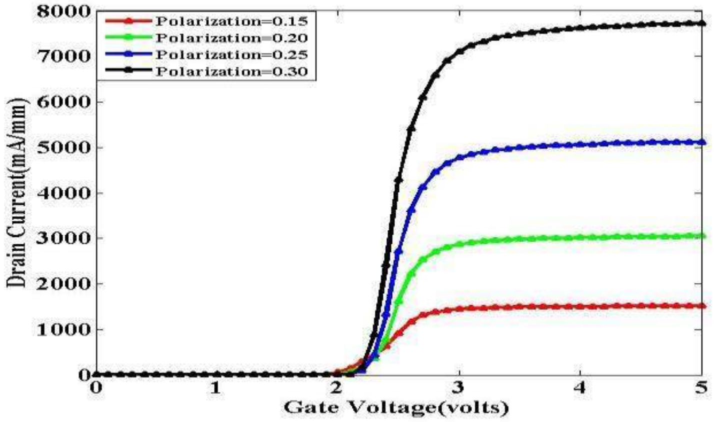

Fig 9: Variation of Drain Current with variation in polarization

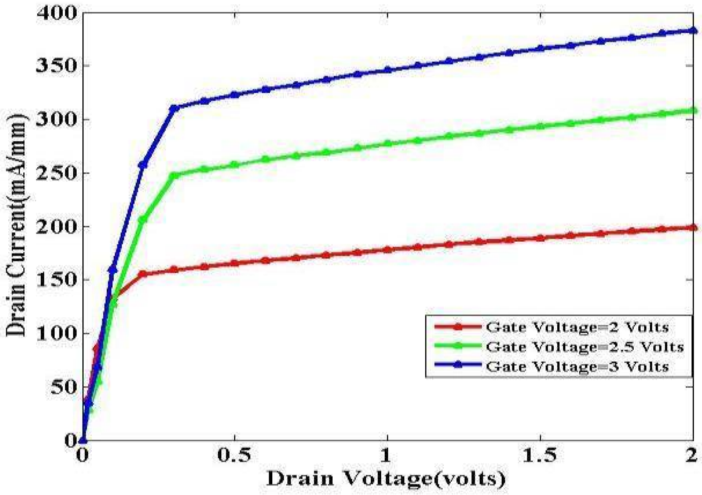

Fig 10: Variation of Drain Current with variation in gate voltage

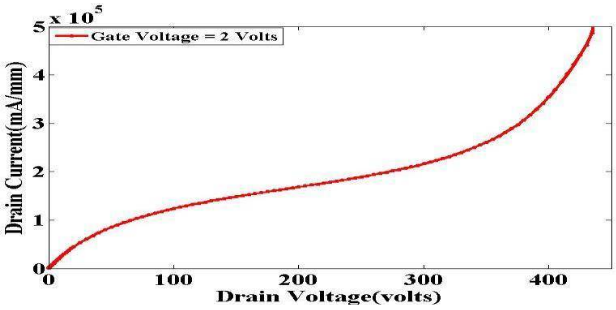

Fig 11: Conventional AlGaN/GaN HEMT breakdown curve

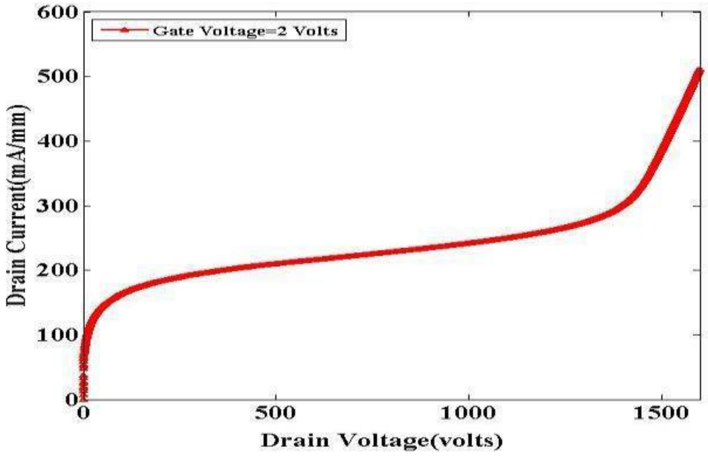

Fig 12: off state AlGaN/GaN/AlGaN HEMT breakdown curve

Fig10 shows the effect in drain current with different gate voltage applied. When gate voltage increases, the maximum drain current also increases with respect to gate voltage. Punch through voltage is very less because of buffer layer. Fig 12 shows the breakdown voltage of AlGaN/GaN double heterojunction HEMTs which is significantly improved as compared to conventional AlGaN/GaN HEMTs [12] it shows in the Fig 11

IV. CONCLUSION

We have presented the impact of gate metal work function on gate current of p-GaN gate HEMT with TCAD device simulation. A normally-off GaN transistor with high breakdown strength is suitable for power applications. The combination of a p-type GaN gate with an AlGaN back-barrier yield in a sufficiently high threshold voltage for power electronic applications by maintaining the low on-state resistances known from AlGaN/GaN HEMT devices. A breakdown voltage of 1400 V for 10 µm gate-drain spacing has been achieved.

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