



# High Performance Low Delay 10T Full Adder

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**ABSTRACT:** High Performance Low Power 10T Full Adder (FA) is presented in this paper. FA is an essential component for the design of all types of processors viz. microprocessors and digital signal processors (DSP) etc. Adders are the core element of complex arithmetic operations like addition, multiplication, division, exponentiation etc. In most of these systems adder lies in the critical path that affects the overall speed of the system. So improving the performance of the 1-bit FA circuit is a significant goal. The present work proposes an energy efficient FA circuit with faster switching of output that reduces the serious problem of carry propagation from one adder to another adder. Result shows 10.56% improvement in Sum delay, 91.46% improvement in Carry delay over the other types of adders with comparable performance of 8T and 9T FAs. The simulation has been carried out on Tanner EDA tool 14.1 at 45nm technologies.

**KEYWORDS:** Full adder; 10T adder; low power; low delay adder; Arithmetic operations; Fast carry propagation; lowest carry delay adder.

## I. INTRODUCTION

For the better performance of any processor, FA must be low powered and switch faster. FA is the combination of two half adders (EXOR and AND gate combination) and an OR gate which is shown in Fig. 1 with its truth table. Equations (1) and (2) shows sum and carry out equations of FA circuit. Adders are used in many arithmetic operations such as addition, subtraction, multiplication, division and numerical representations such as binary-coded decimal or excess-3 and one's and 2's compliments. It is being motivated by three basic design goals, viz. minimizing the transistor count, increasing the speed and minimizing the power consumption of adder circuit [1].

$$S = A \oplus B \oplus C_{in} \quad \dots\dots (1)$$

$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B)) \quad \dots\dots (2)$$

To meet the growing demand, we propose the new high speed, energy efficient adder circuit using 10 transistors that yielded very encouraging results, which are the best in speed, power, lowest delay in comparison to other adders using 8 and 9transistors [1] and [2]. Various FAs using static and dynamic logic are reported in [1]-[12].

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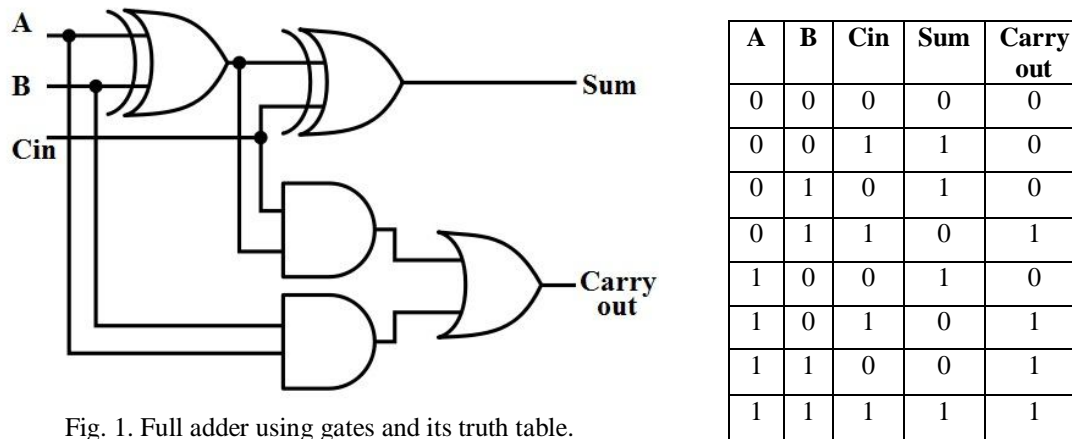


Fig. 1. Full adder using gates and its truth table.

## II. PREVIOUS CONVENTIONAL WORK

Here, we are going to describe 9T FAs which shows better results than other FAs developed till now.

- 9T 1 bit FA:

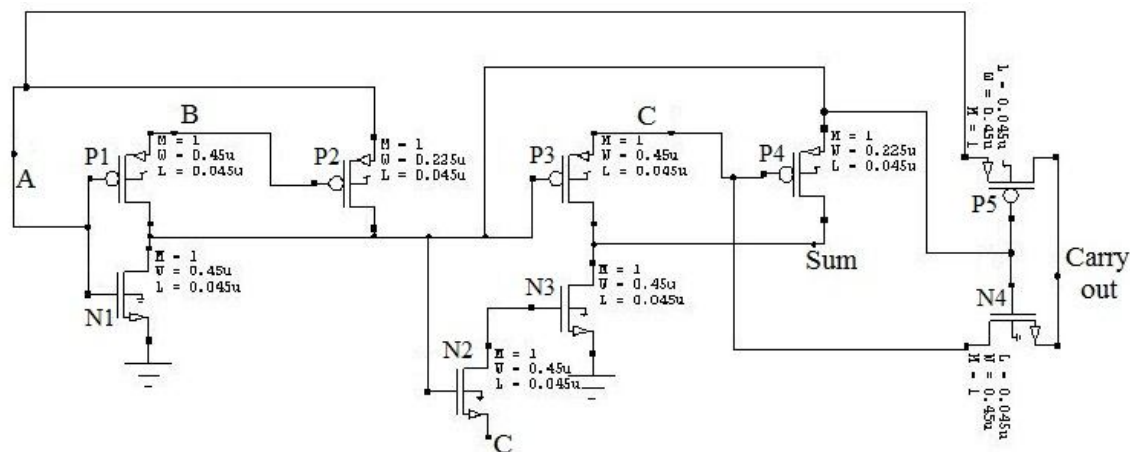


Fig. 3. Full adder using 9T

The circuit shown in Fig. 3 is the 9T FA which is the modified version of 8T FA using an extra transistor N2 that improves the performance of the FA circuit [1]. In 8T FA when inputs are ABC=000, 010 and 110 then problem persists as two transistors get ON simultaneously at the second stage of EXOR and results into the degradation of Sum output due to reduced device resistance as the ON transistors will have combined parallel effect on resistance. Extra transistor N2 gives solution for this problem. Now with inputs 010 and 100, the first stage XOR gate gives “1” which enables the extra added NMOS N2 giving complete “0”. This FA doesn’t give full swing output, so proposed FA removes this full swing problem and provides lower delay for the Sum and Carry out. 9T FA also dissipates more power which dissipates from the input sources.

## III. PROPOSED 10T FULL ADDER

Here, we are going to describe proposed 10T FA circuit which has lowest delay for sum and carry out generation when input is applied. Transistors N1, N2, P1 and P2 work as EXOR gate [4] means when both the input A and B are same, then

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its output is “0” and when both inputs are opposite, then its output is “1”. Intermediate node Z is simply the sum of input A and B. And transistors N3, N4, P3 and P4 are also act as EXOR gate for the input Z and C. So output Sum is the EXOR operation of A, B and C inputs. Carry out depends on the Z (A EXOR B) and inputs A & C. It is implemented using 2T multiplexer design. This design gives very low delay for the Sum output and Carry out. Carry out delay is reduced by using negative bias at the body terminal of the transistor P5 and N5 that makes these transistors so fast for the required operation. This negative bias lowers the threshold of transistors P5 and N5. Carry out delay should be lower for the more than 1-bit adder circuits. The proposed adder design is useful for the 1-bit, 2-bit, 4-bit, 8-bit and 16-bit adder circuits and gives lower power dissipation and fast speed performance. Here, we didn’t use power supply (vdd) but input sources supply the required power for the operation of adder. Carry out doesn’t have full swing for some combination which are shown in Fig. 5.

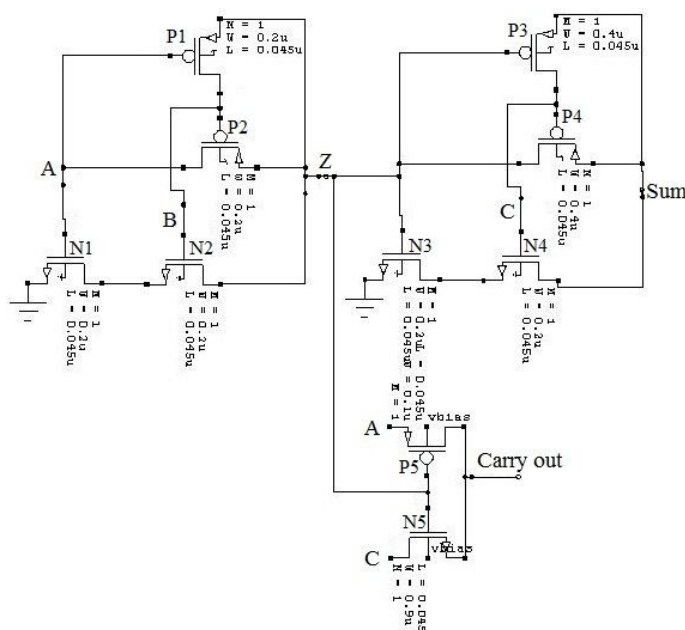


Fig. 4. Proposed 10T FA circuit

## IV. SIMULATION RESULTS

Simulations are performed at 45nm process technology using Tanner EDA tool 14.1 with the supply voltage 0.8V. All transistors are optimized for lower power dissipation and faster operation. Table I shows the delay comparison of different adders which are shown in shown in previous work and proposed work. Table II shows the power dissipation from the input sources A, B and C for 8T, 9T and 10T FA. From the all results, proposed 10T FA is the best according to the Sum & Carry out delay and also according to the power dissipation. It gives 10.56% lower delay than 9T FA circuit and 45.50% lower delay than 8T FA circuit.

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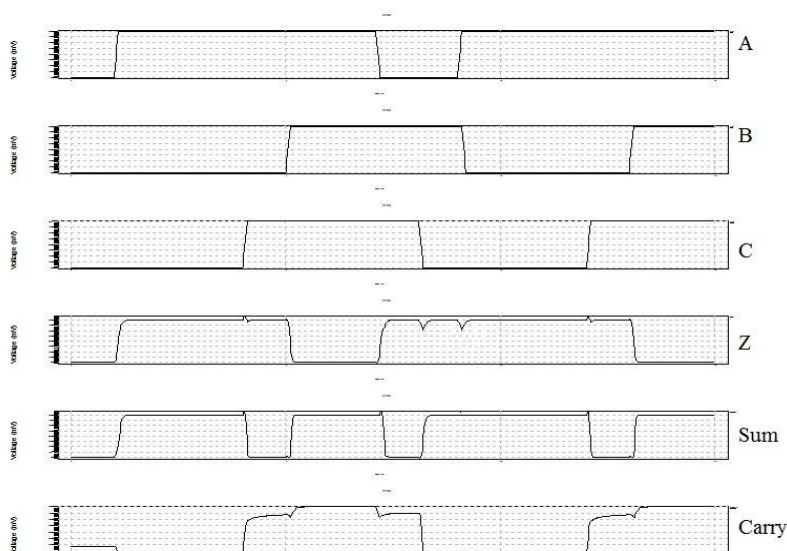
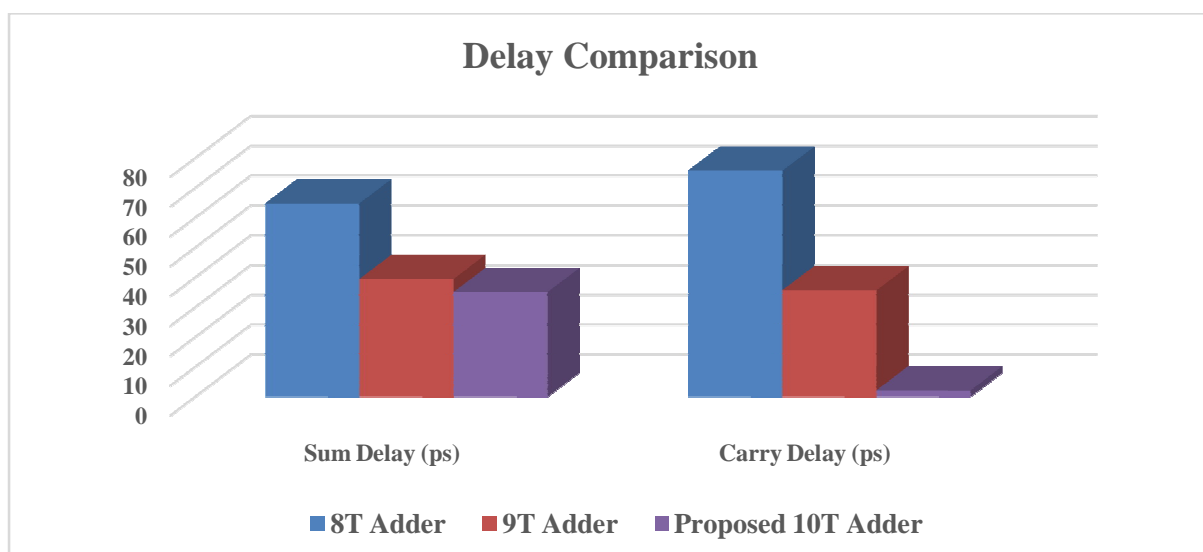


Fig. 5. Simulation waveform of proposed 10T FA circuit

Adders	Sum Delay (ps)	Carry Delay (ps)
8T Adder [1][2]	64.81	75.83
9T Adder [1]	39.49	35.74
Proposed 10T Adder	35.32	3.05

TABLE I. Delay Comparison of different Full Adders



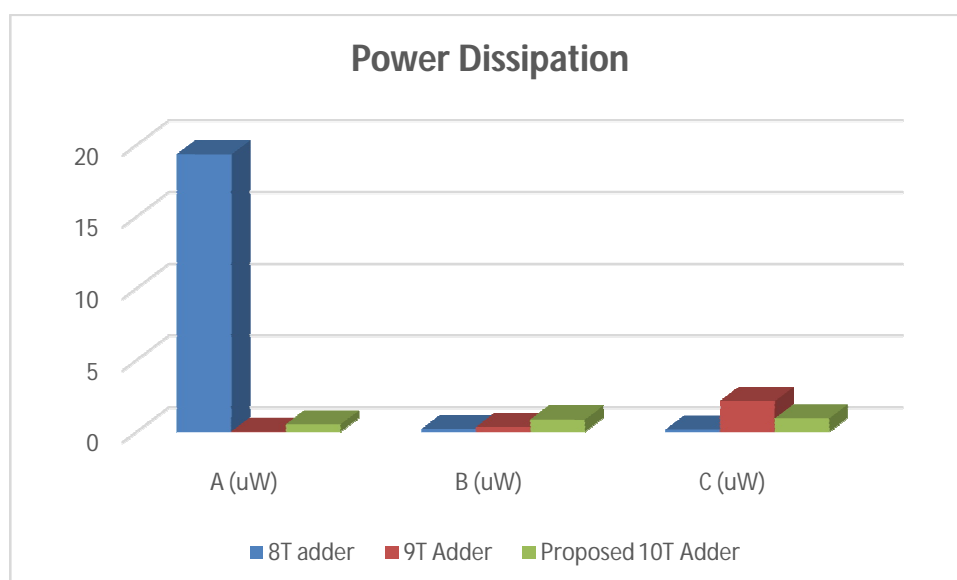
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TABLE 2. Power dissipation Comparison of different Full Adders

Adders	A (uW)	B (uW)	C (uW)
<b>8T adder</b>	19.355	0.192	0.166
<b>9T Adder</b>	0.023	0.327	2.154
<b>Proposed 10T Adder</b>	0.529	0.862	0.934



## V. CONCLUSION

In this paper, we have proposed a high performance low power 10T full adder which gives better performance than other FAs. It shows lowest delay and power dissipation. It gets almost full swing for Sum and Carry out (for particular combinations) during operations. 10T FA gives 10.93% lower delay than 9T FA circuit and 45.50% lower delay than 8T FA circuit. Proposed 10T FA is beneficial for the higher bit adders and it can be used for any arithmetic operations.

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