

e-ISSN: 2320-9801 | p-ISSN: 2320-9798

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

Volume 10, Issue 5, May 2022

ERNATIONAL К **STANDARD**

Impact Factor: 8.165

9940 572 462 □

6381 907 438 \odot

sijircce@gmail.com

www.ijircce.com ω

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

Implementation of Combinational Circuits with Quantum Gates

Munagala Yaswanth Madhu Kumar, Kollipaka Jaya Chandra Vardhan Babu,

Nukavarapu Venkata Sandeep

Student, Department of ECE, Vasireddy Venkatadri Institute of Technology, Guntur, Andhra Pradesh, India

ABSTRACT:Quantum Computing is an emerging field that depends on the basic properties of quantum physics and principles of classical systems. The quantum circuit model uses quantum gates to solve complex problems easily that a classical system takes years to complete. Digital circuits with reversible logic using quantum gates gives faster response, along with low power consumption thereby increasing the efficiency compared to the classical digital circuits. In this paper, we will implement the digital circuits Multiplexer and Demultiplexer using various combinations of Quantum gate named CSWAP. The whole analysis is done through VIVADO XILINX software and implemented using VHDL.

I. **INTRODUCTION**

Earlier quantum computing is developed in numerous ranges based on quantum mechanics that deals with the physical world that is probabilistic and unpredictable. Quantum mechanics being a more general model of physics than classical mechanics give rise to a more general model of computing- quantum computing that has more potential to solve problems that cannot be solved by classical ones. To store and manipulate the information, they use their quantum bits also called Qubits, unlike other classical computers which are based on classical computing that uses binary bits 0 and 1 individually. The computers using such type of computing are known as quantum computers.

Nevertheless, quantum computers are used to solve the complexity of problems within a seconds. This is a processor whose function is based on quantum mechanics thus, the number of inputs is equal to the number of outputs output must be unique.

Quantum computations are working on three conventional principles Superposition, Interface, and Entanglement. But by solving complex problems using the superposition principle.

A. *Superposition:*

In quantum computing, a qubit (short for "quantum bit") is a unit of quantum information—the quantum analog to a classical bit. Qubits have special properties that help them solve complex problems much faster than classical bits. One of these properties is superposition, which states that instead of holding one binary value ("0" or "1") like a classical bit, a qubit can hold a combination of "0" and "1" simultaneously.

$$
\begin{aligned}\n\vert 0 \rangle &= \begin{pmatrix} 1 \\ 0 \end{pmatrix} \\
\vert 1 \rangle &= \begin{pmatrix} 0 \\ 1 \end{pmatrix}\n\end{aligned}
$$

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

B. CSWAP Gate:

The CSWAP gate (also called Fredkin gate) is a computational circuit suitable for reversible computing, which means that any logical or arithmetic operation can be constructed entirely of Fredkin gates. The Fredkin gate is a circuit or device with three inputs and three outputs that transmits the first bit unchanged and swaps the last two bits if, and only if, the first bit is 1.

II. **CLASSICAL LOGIC CIRCUITS**

Logical gates are used for designing logic circuits. They are presently used in most electronic devices like smartphones and tablets. Based on the inputs obtained, logic gates will take the decision and it is based on Boolean algebra. So for a given combination of inputs, the output will always differ, thus the output for each gate is different. Here the input combinations are binary numbers so if the input is *0* it is called *false* and if it is *1* then it is called *true.* Classical logic gates include *NOT, OR, AND, XOR, XNOR, NAND* and *NOR* gates*.* These gates are used to design combinational and sequential circuits.

A. *Multiplexers:*

In electronics, multiplexer is also called as a data selector. This device receives several inputs, selects an input from them and forwards this input as a single output. This selection depends on a separate set of inputs called select lines. Suppose if we consider a multiplexer has $2ⁿ$ inputs then it will have n select lines which will select which input line to be sent as an output.

2:1 Mux:

Fig 1.1: RTL schematic of 2:1 mux

B. *Demultiplexers:*

A Demultiplexer also called as a line converter or data distributer, is a combinational circuit which takes data from one input and distributes it to several outputs. It has 2^n select lines. If $n=1$ then that demux has 2 select lines. Just like multiplexer the selection of output depend on separate set of lines called select lines.

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

1:2 Demux:

Fig 1.2 : RTL schematic of 1:2 demux

C. *Decoder:*

The combinational circuit that change the binary information into 2^N output lines is known as Decoders. The binary information is passed in the form of N input lines. The output lines define the 2^N -bit code for the binary information.

2:4 Decoder:

Fig 1.3 : RTL schematic of 2:4 decoder

III. **QUANTUM LOGIC CIRCUITS**

Quantum logic circuits are the logic circuits that are built by using quantum gates and qubits. Quantum gates play a crucial role in build a quantum circuit. These gates are divided into three types as unary, binary and ternary gate. One of the important quantum gates used in our work for the design of multiplexers and demultiplexers is CSWAP gate. It is observed that the output of CSWAP gate is the output of 2:1 multiplexer. We define 2:1 multiplexer, 1:2 demultiplexer and their cascading to realize high end structures i.e. 4:1, 8:1 multiplexers and 1:4, 1:8 demultiplexers, 2:4 decoder.

A. *Design of 2:1 Multiplexer:*

Quantum circuit of a 2:1 multiplexer requires only one quantum gate i.e, a cswap gate. As the first input is only required we consider it. This select of input depends on the control signal.

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

Fig 1.4 : Simulation Waveforms of 2:1 mux

From the above waveforms, We had taken input A as 1,B as 1 and C as 1 and here A is control input and B and C are target inputs.When control input A is 1 and target inputs B and C as 1 and 0,then B and C outputs Y1 and Y2 got swapped as 0 and 1.

B. *Design of 4:1 Multiplexer:*

Quantum circuit of a 4:1 multiplexer requires three quantum gate i.e. three cswap gates.

Fig 1.5 : Simulation Waveforms of 4:1 mux

From the above waveforms,We had taken inputs in vector form as I[0:3] and selection lines in vector form as S[1:0] and when inputs are taken as all 1's including selection lines then the output Y is obtained as 1 because the input at I[3] is 1 because of selection lines input is 1,1.

C. *Design of 8:1 Multiplexer:*

Quantum circuit of an8:1 multiplexer requires seven quantum gates i.e. seven cswap gates. As the first input is only required we consider it. This select of input depends on the control signal.

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

1.6 : Simulation Waveforms of 8:1 mux

From the above waveforms, When the selection lines input are taken as 1,1,1 and input I as 1 then the Y7 line will receive output as 1 because selection line selected Y7 output.

D. *Design of 1:2 Demultiplexer:*

Quantum circuit of a 1:2 demultiplexer requires only one quantum gate i.e.a cswap gate.

		1,256.833 ns
Name	Value	$1,200$ ns $1,300$ ns فتسلسب لمعالمها $1 + 1 + 1 +$ $\overline{}$
H s		
ii Ui	0	
iji YO	Ō	
II Y1		
끝 U0		

Fig 1.7 :Simulation Waveforms of 1:2 Demux

From the above waveforms,When the selection line input is taken as 1 and input as 1 then output will be received at Y1 because selection line selects Y1.

E. *Design of 1:4 Demultiplexer :*

Quantum circuit of a 1:4 demultiplexer requires three quantum gate i.e. three cswap gates. Cascading is applied on 1:2 demux for designing a 1:4 demux.

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

Fig 1.8 : Simulation Waveforms of 1:4 Demux

From the above waveforms,the inputs are taken for selection lines as 1 and 0 and input as,then the output Y2 is enabled and receives output as 1.

F. *Design of 1:8 Demultiplexer :*

Quantum circuit of a 1:8 demultiplexer requires seven quantum gates i.e. seven cswap gates. Cascading is applied on 1:2 demux and 1:4 demux for designing a 1:8 demux.

		$1,214.000$ ns
Name	Value	$1,000$ ns $1,100 \text{ ns}$ $1,200$ ns $1 + 1 + 1$. . $\mathbf{1}$ ٠ - 1 п п ٠
$\mathbf{\mu}$ so	1	
W S1	1	
$\mathbf{\mathsf{H}}$ S2		
레비	1	
<u> 제</u> Y0	0	
<u> 새 Y1</u>	0	
副 Y2	0	
<u>Ш</u> ҮЗ	0	
副 Y4	0	
温 Y5	0	
<u> 내</u> Y6	0	
<u> 내</u> Y7	1	

Fig 1.9 : Simulation Waveforms Of 1:8 Demux

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

From the above waveforms,the selection line inputs are taken as 1,1 and 1 and input as 1 and the output line Y7 is selected and receives output as 1.

G. *Design of 2:4 decoder:*

Quantum circuit of a 2:4 decoder requires three quantum gate i.e. three cswap gates. Cascading is applied on 1:2 demux for designing a 1:4 demux.

Fig 1.10 : Simulation Waveforms of 2:4 Decoder

From the above waveforms,the inputs are taken as 1 and 0 and enable input as 1,then output line Y1 is enabled.

IV.**CONCLUSION**

Quantum computing is now used widely in varying applications like health, E-commerce and even internet as they can solve complex problems in less time compared to classical computing. Advancement in chip designs demands high speed computations and accuracy.

Quantum Computing is now widely being used in all sectors.Quantum computing will solve complex problems in a faster way rather than a classical computer can solve using its methods.

REFERENCES

- 1. W.D. Pan, and M. Nalasani, "Reversible logic," IEEE Potentials, vol. 24, pp. 38-41, March 2005. J.M. Shalf, and R. Leland, "Computing beyond Moore's law," Computer, vol. 48, pp. 14-23, December2015.
- 2. T.M. Conte, E. Track, and E. DeBenedictis, "Rebooting computing: New strategies for technology scaling," Computer, vol. 48, pp. 10-13, December2015.
- 3. J.D. Hidary, Quantum Computing: An Applied Approach, Springer Nature, Switzerland AG, 2019, pp.3-10.
- 4. M. Soeken, H. Thomas, and R. Martin, "Programming quantum computers using design automation," proceedings of Design, Automation and Test in Europe, March2018.
- 5. M.S. Islam and M. Rafiqul Islam, "Minimization of reversible adder circuits," Asian Journal of Information Technology, vol. 4, pp. 1146-1151,2005.

6. C. Degen, F. Reinhard, and P. Cappellaro, "Quantum sensing: Reviews of modern physics," vol. 89, pp. 035002, July2017.

7. M. Krenn, M. Malik, T. Scheidl, R. Ursin, and A. Zeilinger, "Quantum communication with photons," Optics in Our Time, Springer, December2016.

8. Anand, B.K. Behera, and P.K. Panigrahi, "Solving diner's dilemma game, circuit implementation and verification on the IBM quantum simulator," Quantum Inf. Process. vol. 19, pp. 1-14, May2020.

9. VEDRAL, A. BARENCO, AND A. EKERT, "QUANTUM NETWORKS FOR ELEMENTARY ARITHMETIC OPERATIONS," *PHYSICAL REVIEW A*, VOL. 54, NO. 1, PP. 147–153, JULY1996.

10. S. A. Cuccaro, T. G. Draper, S. A. Kutin, and D. P. Moulton, "A new quantum ripple- carry addition circuit,"

IIJIRCCE

 | e-ISSN: 2320-9801, p-ISSN: 2320-9798| [www.ijircce.com |](http://www.ijircce.com/) |Impact Factor: 8.165 |

 || Volume 10, Issue 5, May 2022 ||

| DOI: 10.15680/IJIRCCE.2022.1005291 |

CoRR, vol. abs/quantph/0410184, November2004.

- 11. H. Thapliyal, "Mapping of subtractor and adder-subtractor circuits on reversible quantum gates," Trans. on Comput. Sci. XXVII, LNCS 9570, pp. 10–34, April2016.
- 12. M. Rahmati, M. Houshmand, and M.H. Kaffashian, "Novel designs of a carry/borrow look-ahead adder/subtractor using reversible gates," J. Comput. Electron., vol.16, pp. 856-866, July2017.
- 13. G. Oktay, K.T. Weng, B-F. Kent, and A. Brodutch, "Benchmarking quantum processors with a single qubit," Quantum Inf. Process. vol. 19, pp. 1-17, March2020.

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN COMPUTER & COMMUNICATION ENGINEERING

1 9940 572 462 **8** 6381 907 438 \approx ijircce@gmail.com

www.ijircce.com