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Efficient Error Detection Structure for Linear Feedback Shift Registers

K. Sowmya Sri[1], Ch. Naveen[2], J. T. Venkata Teja[3], Ch. Sravani Nag[4], N. S. Krishna Babu[5]

Assistant Professor, Department of ECE, Sri Vasavi Institute of Engineering & Technology, Nandamuru, A.P, India[1]

U.G. Student, Department of ECE, Sri Vasavi Institute of Engineering & Technology, Nandamuru, A.P, India [2]

U.G. Student, Department of ECE, Sri Vasavi Institute of Engineering & Technology, Nandamuru, A.P, India [3]

U.G. Student, Department of ECE, Sri Vasavi Institute of Engineering & Technology, Nandamuru, A.P, India [4]

U.G. Student, Department of ECE, Sri Vasavi Institute of Engineering & Technology, Nandamuru, A.P, India [5]

ABSTRACT: In many different applications, including Built-In-Self-Test circuits and Pseudo Random Number Generators, Linear Feedback Shift Registers (LFSR) are widely employed. So, for applications with faults, fault tolerant LFSR design is crucial. Strong dependability requirements Conventional fault-tolerant LFSRs have a lot of Single-Point- of-Failures (SPoFs), where one fault can bring the entire system down. In this study, a new fault tolerant architecture for LFSR (referred to as FT-LFSR) is suggested, with a substantially smaller number of SPoFs than the previous ones. To achieve this, a modified form of Triple Modular Redundancy (TMR) is employed, equipped with a few extra controlling units for locating the operative module is employed. In addition, a novel metric called Reliability-Area-Factor (RAF), a novel metric, is also proposed to assess the effectiveness of redundancy-based fault tolerant approaches (such FT-LFSR) in terms of the quantity of SPoFs and the area overhead. The FT-LFSR is resilient to all single transient and permanent faults, with the exception of its constrained SPoFs and numerous patterns of multiple faults, according to experimental results.

KEYWORDS: LFSR, Fault tolerance, FPGA, TMR, Test, Built in self-test.

I. INTRODUCTION

The primary element of embedded systems based on pseudorandom bit sequences includes rapid digital counters, built-in self-tests, pseudorandom number and noise sequence generators, and linear feedback shift registers (LFSR). Now and False functionality could have disastrous implications in safety-critical embedded applications, hence fault-tolerance is known as a traditional design requirement. Integrated Circuits (ICs) are becoming more susceptible to different hardware flaws in recent years due to the ongoing lowering of transistor size and supply voltage levels.

Redundancy, or the addition of additional capabilities to the original design that are not required for fault-free operation, is the fundamental idea of fault tolerance. Both spatial and temporal redundancy are possible. A well-known and widely used fault-tolerant method based on spatial redundancy is called Triple Modular Redundancy (TMR) [9]. To run a procedure in parallel, the design is duplicated three times in TMR. The result is then processed by a majority-voting method to produce a single output. Despite its effectiveness, the TMR approach has a significant flaw known as single- point-of-failure (SPoF). The SPoF is the design element that, if it fails, will cause the entire system to fail. In TMR, the majority-voting procedure is accounted for as its SPoF. Thus, in TMR-based fault tolerant systems, the number of SPoF is essential to be taken into account. In some earlier publications, fault-tolerant LFSR designs based on TMR methodology have been developed. Although they have offered fault tolerance for single faults, the number of SPoFs is dramatically raised by tripling the majority-voting method, which significantly reduces the design's reliability.

This work proposes a novel fault-tolerant LFSR (dubbed FTLFSR) in which the quantity of SPoFs is drastically decreased. To do this, a modified TMR that has additional controlling units for locating the operational module is used. In order to compare TMR-based fault tolerance strategies, we also present a novel comparison metric called Reliability-Area-Factor (RAF), which takes into account the number of SPoFs and area overhead of the TMR approach. Verilog is used to simulate and implement the suggested design on the Xilinx Spartan 6. The fault injection-based experimental

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results demonstrate that FT-LFSR tolerates numerous patterns of multiple faults in addition to all single transient and permanent faults (except from those that occur in its constrained SPoFs).

II. METHODOLOGY

A shift register with an input bit that is a linear function of its prior state makes up the LFSR state machine. The two primary LFSR configurations are the Galois and Fibonacci designs. The outputs from a few of the registers in the Fibonacci implementation are XORed together and supplied back to the shift register's input. The gates are positioned between the registers in the Galois implementation. The traditional Fibonacci and Galois LFSR implementations are displayed in Figure 1. n indicates the number of flip-flops, DF0,..., DFn, in the register, which represents the length of the LFSR. The binary coefficients for the n + 1 feedback terms are c0, c1,..., and cn. In contrast to the Fibonacci variation, the numbering of the feedback for the Galois implementation is reversed. The following is the form of the characteristic polynomial for the LFSR with n flip-flops:

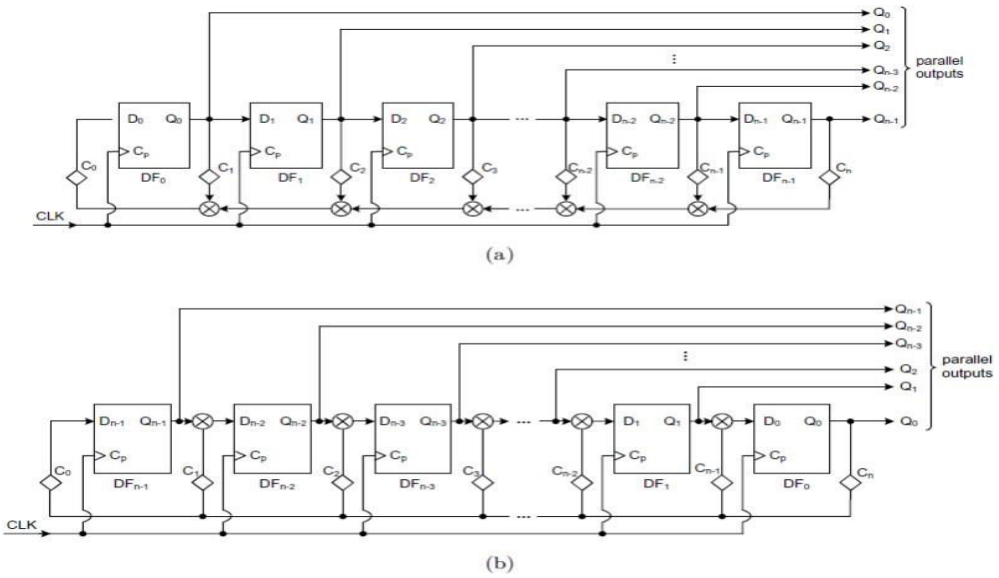

Fig. 1. LFSR structure. (a) Fibonacci implementation; (b) Galois implementation.

III. RELATED WORKS

In and, the fault tolerant architecture shown in Fig 2 is proposed for LFSRs (which we call it P-LFSR), the TMR technique is used in which the original design is triplicated and similar inputs are fed into the modules. The final output is obtained based on majority voting (which is not shown in Fig 2) on the outputs of the three voters (voter 1, voter 2, and voter 3). So, the last majority voter (which includes N onebit voters) is the SPoF of this architecture and any fault in the last voter leads to the system failure. Therefore, although this architecture tolerates the single faults in the intermediate points of the circuit, its reliability is threatened by N SPoFs.

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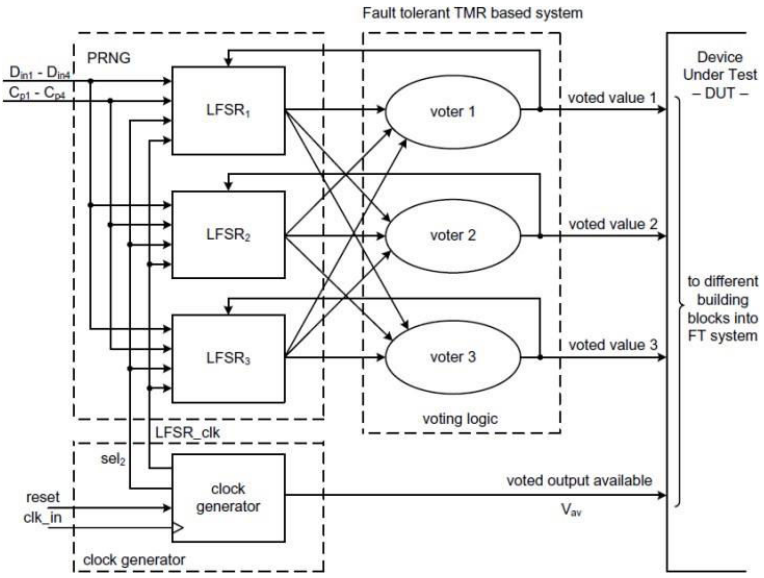

Fig. 2. P-LFSR structure

In this section, we describe the fault tolerant architecture proposed for LFSRs called FT-LFSR. The proposed architecture is shown in Fig 3. FT-LFSR has three PEs 1 and one voter based on TMR approach with Controller module which reduces the number of SPoFs. This architecture has two outputs 2 and one input 3 :

1. out sel. out sel comes from a module which controls the FTLFSR (e.g. BIST4) and determines which PE must be connected to FT LFSR out (selected PE).
2. FT LFSR out. FT LFSR out is the N bit output of selected PE which is the same as a conventional LFSR's output.
3. ready. ready shows that FT LFSR out is valid or not. if ready equals one, it means that FT LFSR out is valid and it means invalid.

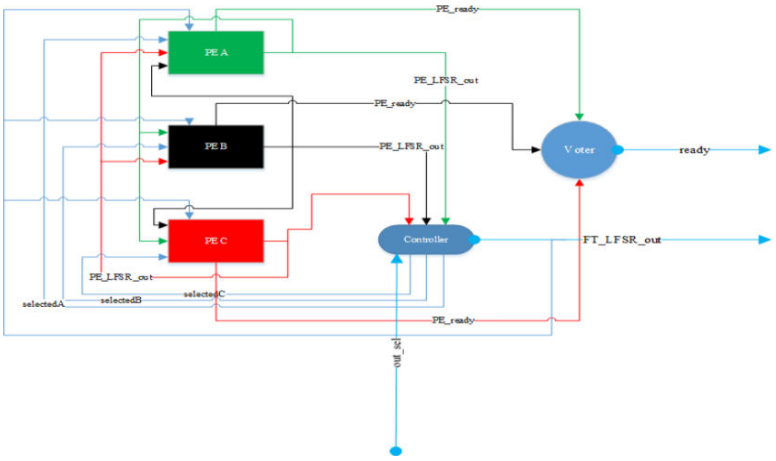

Fig. 3. The block diagram of the proposed FT-LFSR

IV. RESULT

This section investigates the efficacy of the proposed fault tolerant LFSR in various aspects based on the extensive fault injection analysis. The proposed method is implemented in Verliog language, simulated by ISE tool, and synthesized on Spartan 6 FPGA. Logic value upset is considered as the fault model for fault injection. In order to model transient faults, the logic upset is injected only for one clock cycle and then, becomes corrected in the next cycles while for

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permanent faults, the logic upset remains in the circuit for more than one clock cycle. Faults have been injected in outputs of main modules (PE, Controller and voter) and main inputs (sel out) in two forms wrong zero and wrong one. The used polynomial generators 6have been brought in table II.

TABLE I

POLYNOMIAL GENERATOR FOR DIFFERENT LFSR WIDTHS

LFSR width	Polynomial generator
16	$x^{16} + x^{14} + x^{13} + x^{11} + 1$
32	$x^{32} + x^{22} + x^{2} + x^{1} + 1$
64	$x^{64} + x^{63} + 1$

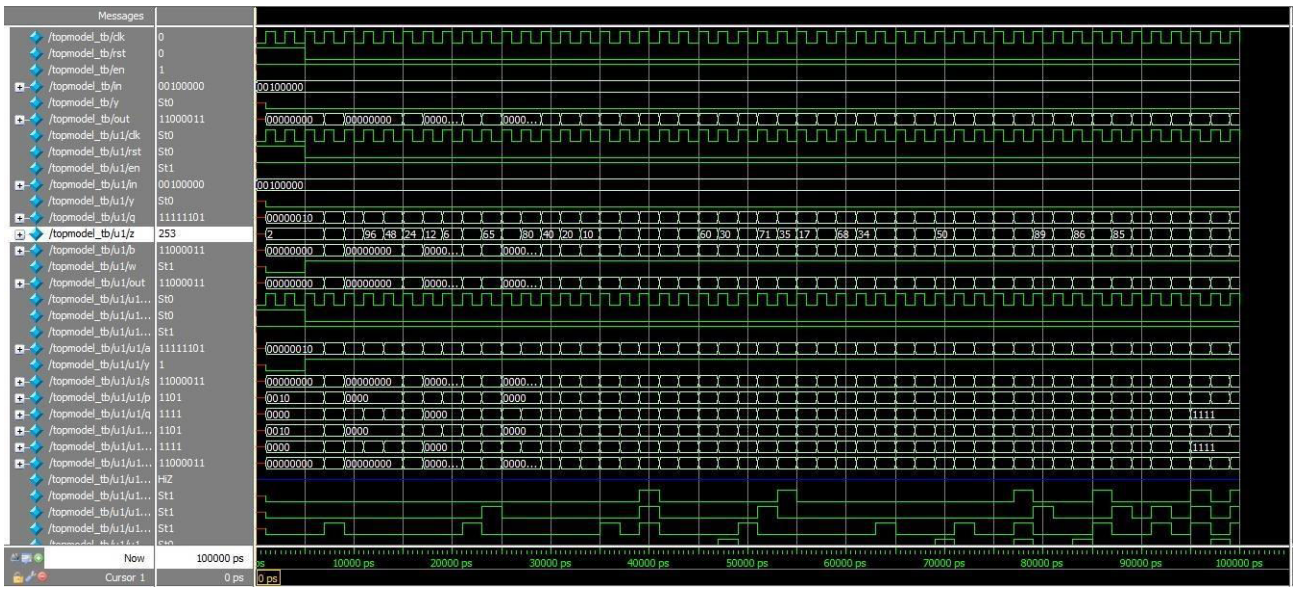

Fig 4: output waveforms

V. SYNTHESIS AND IMPLEMENTATION OF THE DESIGN

About Execution, click To use Synthesize-XST, doubleclick on the chosen existing file. If there are any errors, fix them. Click on the reports and the design overview. link if there are no errors.

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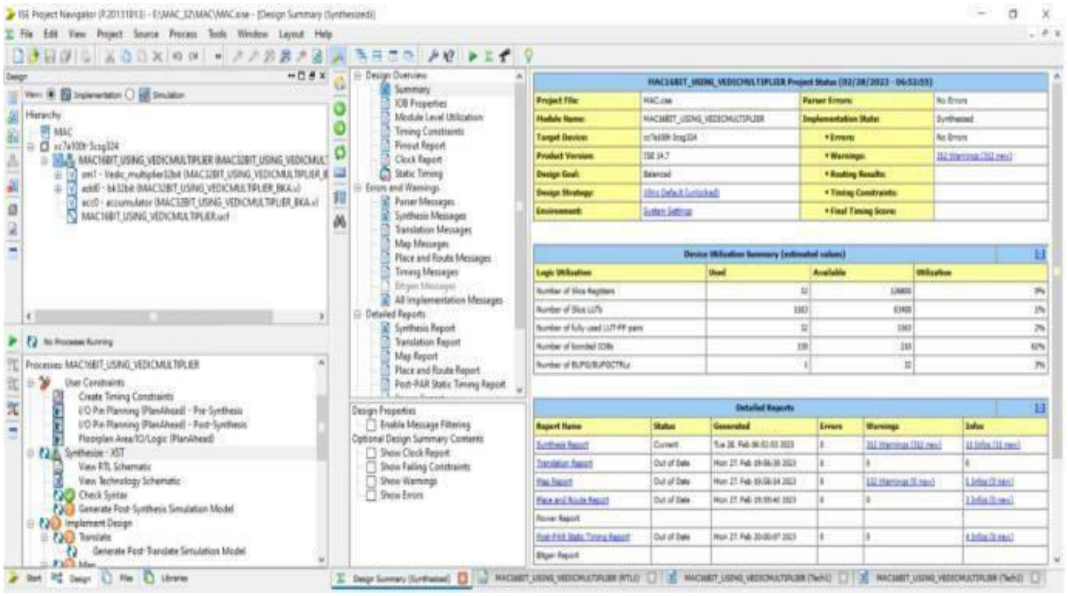

Fig 5. Design synthesis

VI. VIEW RTL SCHEMATIC

When Synthesize-XST is expanded, select See RTLSchematic and then click OK.

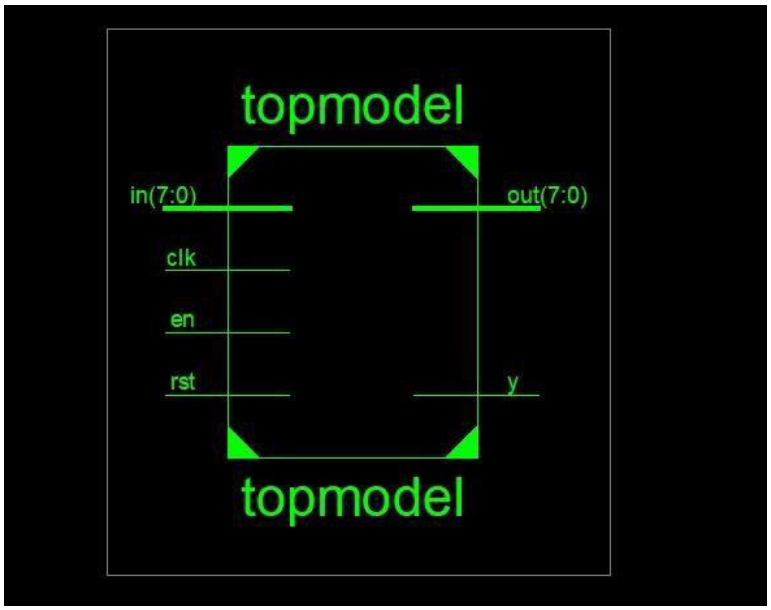

Fig 6: RTL schematic

Seeing the internal modules requires opening the window with the top module. simply choose the top module

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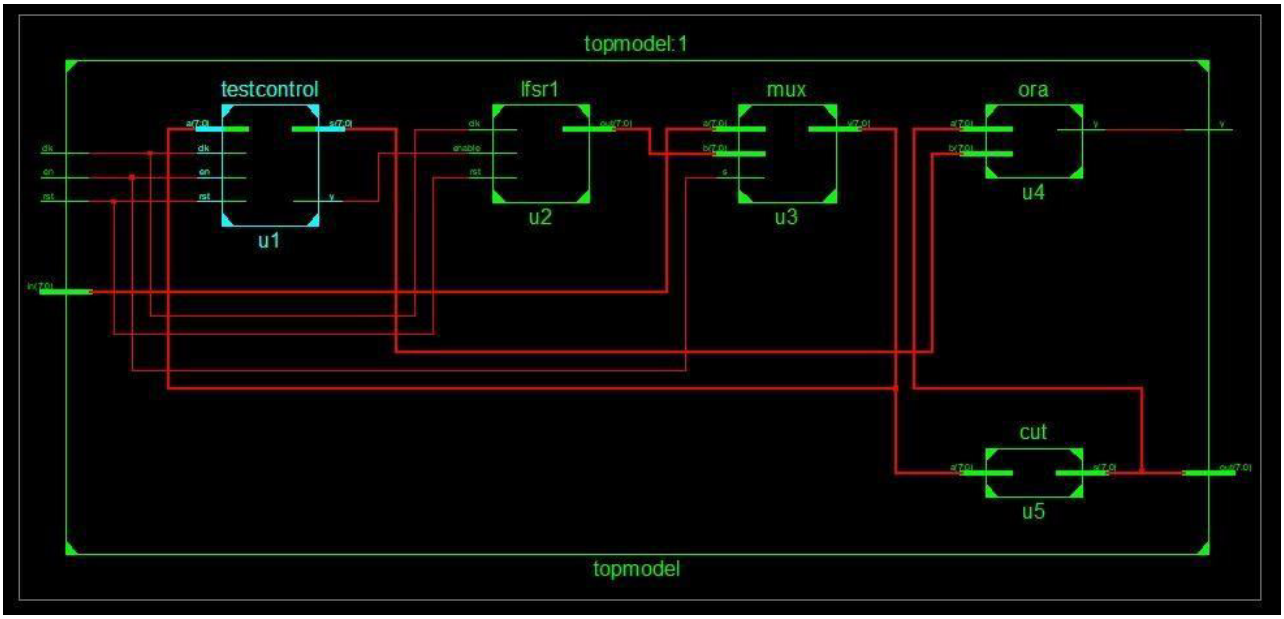

Fig 7: RTL Schematic internal modules

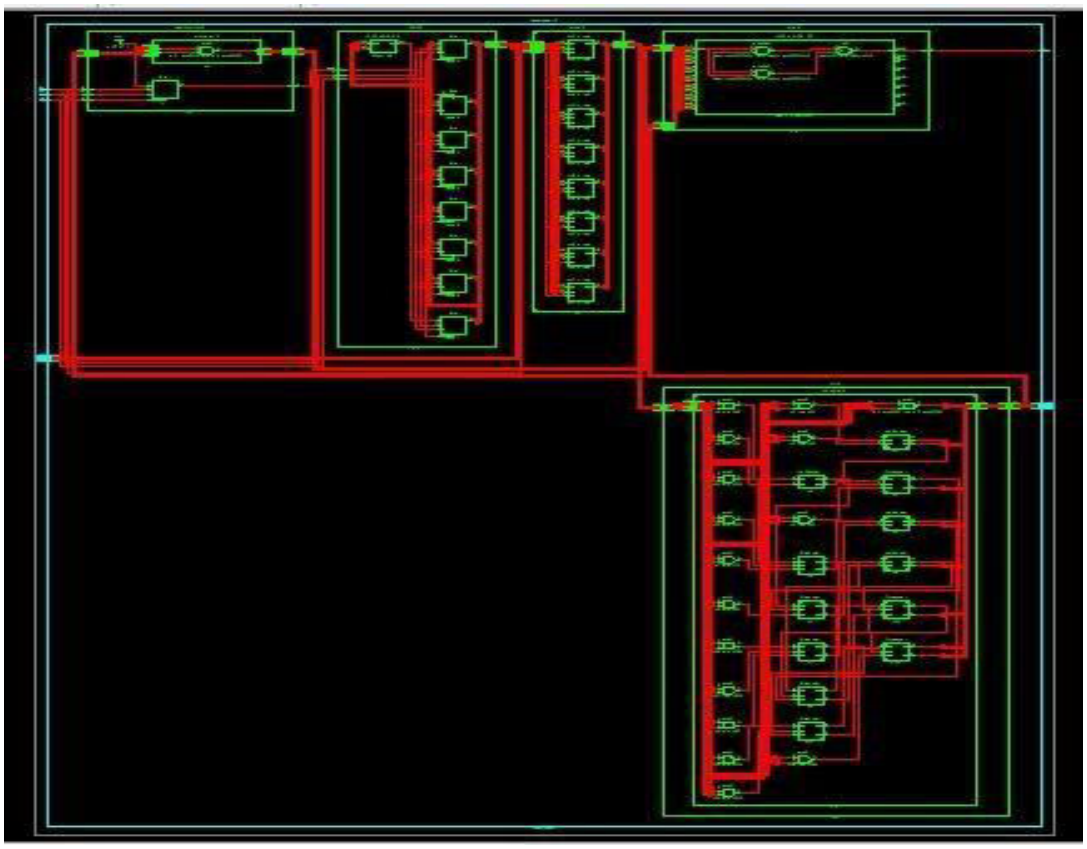

Fig 8: Technology schematic

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VII. CONCLUSION

In this paper, a new fault tolerant architecture for LFSRs called FT-LFSR is proposed which is applicable pseudorandom sequence generators such as BIST structures and pseudo random number generators. The main superiority of FT-LFSR over its counterparts is its less number of SPoFs. This leads to high resiliency to single (transient and permanent) faults and many patterns of multiple faults. We also introduce a novel metric called RAF which integrates the reliability improvement and area overhead of fault tolerant techniques in digital designs. The fault tolerance of FT- LFSR is investigated quantitatively and also through some experimental results on Spartan 6 FPGA. The results show the high fault tolerance of FT-LFSR against single and multiple faults in expense of reasonable area and delay overhead.

TABLE II

POWER CONSUMPTION OF DIFFERENT DESIGNS

Device	
Family	Spartan3e
Part	xc3s1600e
Package	fg320
Temp Grade	Commercial
Process	Typical
Speed Grade	-5

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0

Characterization	
PRODUCTION	v1.2,06-23-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	38	29504	0
Signals	0.000	56	---	---
IOs	0.000	20	250	8
Leakage	0.203			
Total	0.203			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	21.1	80.7	29.3

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.069	0.000	0.069
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.003	0.000	0.003

	Total	Dynamic	Quiescent
Supply Power (W)	0.203	0.000	0.203

REFERENCES

1. Leonard Colatitude and Dennis Silage, ”Efficient PGA LFSR Implementation Whitens Pseudorandom Numbers, 2009 International Conference on Reconfigurable Computing and FPGAs, 2009.
2. Thomas E. Tkacik, A Hardware Random Number Generator, 2003.
3. Nagaraj s vannal, saroja v siddamal, shruti v bidaralli, mahalaxmi s bhille, Design and testing of combinational Logic circuits using built in self Test scheme for fpgas, 2015 fifth international conference on communication systems and network technologies, 2015.
4. Jonathan M. Comer, Juan C. Cerda, Chris D. Martinez, and David H. K. Hoe, Random Number Generators using Cellular Automata Implemented on FPGAs, 44th IEEE Southeastern Symposium on System Theory, University of North Florida, Jacksonville, FL, March 2012.
5. R. Mita, G. Palumbo, S. Pennisi, M. Poli, A novel pseudo random bit generator for cryptography applications, Electronics, Circuits and Systems, 2002. 9th International Conference on, vol. 2, pp. 489 492, 2002.
6. Patooghy, A. Miremadi, S Ghassem. Javadtalab, A. Fazeli, M. Farazmand, Navid. (2006). A Solution to Single Point of Failure Using Voter Replication and Disagreement Detection. Proceedings - 2nd IEEE International Symposium on Dependable, Autonomic and Secure Computing, DASC 2006. 171-176. 10.1109/DASC.2006.15.
7. V. Petrovi, Z. Stamenkovi, M. Stojev, T. Nikoli, and G. Jovanovi, ”FaultTolerant Reconfigurable Low-Power Pseudorandom Number Generator,” IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Karlovy Vary Czech Republic, pp. 279-282, April 2013.
8. S. Nemanja, S. Mile, N. Tatjana, P. Vladimir and J. Goran. ”Reconfigurable low power architecture for fault tolerant pseudo-random number generation,” Journal of Circuits Systems and Computers, vol. 23, no. 1, pp. 1-21, February 2014.

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