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# Review Paper on Adaptive Filter based on Multi-rate Approach and Distributive Technique

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**ABSTRACT: -** Multi-rate systems are popular in DSP, which are used in audio, video processing and communication systems. Using Multi-rate system we can achieve the computation efficiency and improve the system performance. A Multi-rate systems operation involves decimation and interpolation. For a given signal, the method of decreasing the sampling rate is decimation and the process of increasing the sampling rate is interpolation. By cascading the process of decimation and interpolation results, savings in computation and great reduction in hardware complexity is achieved. For the application of Design a Narrow Band Filter for application for signal processing algorithm. To implement such a large order FIR filter in hardware involves large resources and sometime difficult to implement in resource constrained application. Keeping this in view, we have used Multi-rate approach to design the narrowband filter.

**KEYWORDS: -** Finite Impulse Response (FIR), Look Up Table (LUT), Adaptive Filter, Narrow Band Filter

## I. INTRODUCTION

The Digital Signal Processing (DSP) is one of the fastest growing technologies in digital communication systems over more than three decades. The digital filters are the main basic building blocks of DSP systems. The digital filter is used to remove unwanted noise in the incoming signals [1]. For achieving high speed computation in DSP Systems, FIR filters are used and it is implemented on dedicated hardware than software systems. There are many ways to design FIR filters, which can be realized in recursive and non-recursive techniques. In the Direct form, normal FIR filter gives the filter output by computing inner product which leads to long critical path. To avoid these problems, many solutions are designed which includes parallel and pipelined methods. The DA (Distributed Arithmetic) method is one best method to reduce hardware resources by replacing the convolution multipliers by LUT's to get high throughput.

DA based FIR filter that is designed in, is a memory based generation of up sampling along with interpolation method which can be modified or extended for filter design [2]. The up sampling is one of the methods that are used to insert zeros between the original input samples followed by FIR filters. They have used, in interpolation method to store the LUT values instead of Memory blocks. The interpolation values are output samples which are sequentially connected with the help of simple counter which eliminates the zeros in the design and improves the design area. They are using two dimensional shifts plus rotate registers which is used to shift the samples vertically and rotate horizontally to give better result. The raised-cosine filter is used in example design. It acts as a band – limited filter and impulse response for the roll-off factor of 0.3 and up sampling value of 5 is obtained. The performance is analyzed based on the parameter constraints like area, memory and mainly speed is considered to design the FIR filter using DA based approach [3, 4]. In FIR filter design, number of taps, plays a vital role for performance constraints. If the number of taps increases, the memory usage also increases exponentially, then the design operates at low speed. To solve these issues, two approaches are designed. One approach is to use Individual Scaling Accumulator for each DA based block and the other is to use only one Scaling Accumulator for all DA based blocks. With these approaches, reduction in memory usage is achieved along with improvement in the area and operating speed. In paper, FIR filter based on DA

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algorithm is designed and compared with traditional multiply-add method on FPGA. The computation of multiply-accumulate operation is realized using DA algorithm. They have designed 16-tap filter and it is analyzed in two tests with 5MHZ sampling frequency. They have used tree based shift-adder module to reduce the delay time. The architecture is based on FPGA with reliability of the system and design precision. The pipelined architecture of adaptive FIR filter is designed using DA method. Adaptive filter based on DA-technique is designed using LMS algorithm for higher orders. They are replacing MAC operators with bit serial nature of LUT shift-add unit. The architecture is same as with some changes in the design. The architecture is improved in terms of slices and there is reduction in delay [5].

## II. LITERATURE REVIEW

**Basant Kumar Mohanty et al.,** in this paper, we break down the substance of query tables (LUTs) of circulated math (DA)- based square slightest mean square (BLMS) versatile channel (ADF) and in light of that we propose intra-emphasis LUT sharing to decrease its equipment assets, vitality utilization, and emphasis period. The proposed LUT streamlining plan offers a sparing of 60% LUT content for square size 8 and still higher putting something aside for bigger square sizes over the ordinary outline approach. We too introduce here the outline of an enroll based LUT grid for maximal sharing of LUT substance and full-parallel LUT-refresh task. In light of the proposed configuration approach, we have determined a DA-based design for the BLMS ADF, which is versatile for bigger piece sizes and also higher channel lengths. We find that the equipment many-sided quality of the proposed structure increments not exactly proportionately with input piece measure and channel length.

**Azadeh Safari et al.,** discrete wavelet change (DWT) has demonstrated awesome execution in computerized picture pressure and denoising applications. It is the change utilized for source encoding as a part of JPEG2000 still picture pressure standard and FBI wavelet scalar quantization. DWT is fit for quick picture pressure at less region and low power utilization. This paper displays 4-tap orthogonal DWT in view of the buildup number framework. Equipment unpredictability lessening and configuration change are attained to by utilizing RNS for number-crunching operations and LUT offering between low pass and high pass channels. The RNS based DWT is reenacted and executed on the Xilinx FPGA to confirm the usefulness and effectiveness of the outline.

**Yajun Zhou *et al.*,** The present examination paper portray a system assessing the Field Programmable Gate Array (FPGA) assets usage for execution of computerized channels with distinctive requests. For a low pass Butterworth channel, barring its request, rest of the configuration parameters were kept steady. Channel outlining was done utilizing the numerical figuring environment programming, MATLAB. Its exceptional office producing Hardware Description Languages (HDLs) for a computerized channel item was conveyed. Diverse Very High Speed Integrated Circuit HDL (VHDL) source codes were created and executed in Xilinx FPGA gadget Spartan-3E by expanding channel request, until the gadget usage surpasses the accessible assets. Thusly, a most extreme 18th request channel was implementable in FPGA. The computerized channel reaction was shown on an Oscilloscope by method for a microcontroller, Advance RISC Machine (ARM) gadget LPC2148. The simple to advanced and computerized to simple transformation over advanced channel information was performed in a solitary ARM chip.

**V. Sudhakar et al.,** this paper displays completely parallel and completely serial architectures for Band pass channel. The exhibitions of completely parallel and completely serial architectures are investigated for distinctive quantized adaptations of representation. Channels produced utilizing 8 bit settled point execution requires littler zone utilization when contrasted with 16 bit altered point usage at the expense of imprecision. The proposed executions are orchestrated with Xilinx ISE 13.2 rendition. Group of gadget was Spartan 3E and target gadget was xa3s250e-4vqgl00. The key execution measurements, to be specific number of Slices, Slice Flip Flops, LUTs, Maximum recurrence are analyzed.

**Animesh Panda et al.,** a channel may be obliged to have a given recurrence reaction, or a particular reaction to a motivation, step, or incline, or recreate a simple framework. Contingent upon the reaction of the framework, computerized channels can be ordered into Finite Impulse Response (FIR) channels & Infinite Impulse Response (IIR)

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channels. FIR Filters can be composed utilizing recurrence examining or windowing routines. Yet these strategies have an issue in exact control of the basic frequencies. In the ideal outline system, the weighted estimate lapse between the real recurrence reaction and the sought channel reaction is spread over the pass-band and the stop-band and the greatest blunder is minimized, bringing about the pass-band and the stop-band having swells. The crest mistake can be processed utilizing a PC supported iterative methodology, known as the Remez Exchange Algorithm.

## III. DISTRIBUTIVE ARITHMETIC TECHNIQUE

Distributed Arithmetic (DA) is a widely-used technique for implementing sum-of-products computations without the use of multipliers. Designers frequently use DA to build efficient Multiply-Accumulate Circuitry (MAC) for filters and other DSP applications. The main advantage of DA is its high computational efficiency. DA distributes multiply and accumulates operations across shifters; lookup tables (LUTs) and adders in such a way that conventional multipliers are not required.

Distributed arithmetic is an important algorithm for DSP applications. It is based on a bit level rearrangement of the multiply and accumulate operation to replace it with set of addition and shifting operations. The basic operations required are a sequence of table lookups, additions, subtractions and shifts of the input data sequence. The Look Up Table (LUT) stores all possible partial products over the filter coefficient space.

Assuming coefficients c[n] is known constants, and then y[n] can be rewritten as follows:

$$y[n] = \Sigma\, c[n] \cdot x[n] \quad n = 0, 1, \ldots, N-1 \tag{1}$$

Variable x[n] can be represented by:

$$x[n] = \Sigma\, x_b[n] \cdot 2^b \qquad b=0, 1, \ldots, B-1$$
$$x_b[n] \in [0, 1] \tag{2}$$

Where $x_b[n]$ is the $b^{th}$ bit of x[n] and B is the input width. Finally, the inner product can be rewritten as follows:

$$y = \Sigma\, c[n] \Sigma\, x_b[k] \cdot 2^b \tag{3}$$

$$\begin{aligned} &= c[0]\,(x_{B-1}[0]2^{B-1} + x_{B-2}[0]\,2^{B-2} + \ldots + x_0[0]\,2^0) \\ &+ c[1]\,(x_{B-1}[1]\,2^{B-1} + x\,x_{B-2}[1]\,2^{B-2} + \ldots + x_0[1]\,2^0) + \ldots \\ &+ c[N-1]\,(x_{B-1}[N-1]\,2^{B-1} + x_{B-2}[0]\,2^{B-2} + \ldots + x_0[N-1]\,2^0) \end{aligned} \tag{4}$$

$$\begin{aligned} &= (c[0]\,x_{B-1}[0] + c[1]\,x_{B-1} + \ldots + c[N-1]\,x_{B-1}[N-1])\,2^{B-1} + (c[0]\,x_{B-2}[0] \\ &+ c[1]\,x_{B-2}[1] + \ldots + c[N-1]\,x_{B-2}[N-1])\,2^{B-2} + \ldots + (c[0]\,x_0[0] + \\ &c[1]\,x_0[1] + \ldots + c[N-1]\,x_0[N-1])\,2^0 \end{aligned} \tag{5}$$

$$= \Sigma\; 2^b\, \Sigma\, c[n] \cdot x_b[k]$$

Where n=0, 1… N-1 and b=0, 1… B-1

The coefficients in most of DSP applications for the multiply accumulate operation are constants.

## IV. MULTIRATE APPROACH

The process of converting a signal from a given rate to a different rate is called sampling rate conversion. The systems which employ multiple sampling rates in the processing of digital signal are called multi-rate signal processing [5].

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Decimation is the processes of lowering the word rate of a digitally encoded signal, which is sampled at high frequencies much above the nyquist rate. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma-delta ADC, oversampling the analog input signal by the modulator alone does not lower the quantization noise; the ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Figure 1.The decimator is a combination of a low pass filter and a down sampler. In Figure 1 the transfer function, H(z) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor M, where M is the oversampling ratio [6]. The function of low pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of the averaging circuit is given by equation (1.1). It establishes a relation between the input and output functions (1.1)

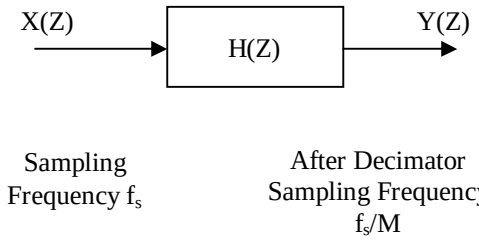


Figure 1: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M}\sum_{x=0}^{M-1} Z^{-x} \qquad (6)$$

**"Up sampling"** is the process of inserting zero-valued samples between original samples to increase the sampling rate. (This is called "zero-stuffing".) Up sampling adds to the original signal undesired spectral images which are centered on multiples [7] of the original sampling rate.
**"Interpolation",** in the DSP sense, is the process of up-sampling followed by filtering. (The filtering removes the undesired spectral images.) As a linear process, the DSP sense of interpolation is somewhat different from the "math" sense of interpolation, but the result is conceptually similar: to create "in-between" samples from the original samples.

## V. PROPOSED METHODOLOGY

It depends on the filter coefficients required to achieve the desired frequency response of the filter. The narrowband filter may be implemented directly or using the multi-rate method. Here we have estimated the required filter coefficients for both these methods to find the complexity of the narrow band filter.

- Specification of the narrowband filter:

Sampling frequency, $F_s = 250Hz$

Pass band ripple, $\delta_p = 0.08dB$

Stop band ripple, $\delta_s = 42dB$

Pass band frequency, $f_p = .825Hz$

Stop band frequency, $f_s = 4.15Hz$

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- Direct Approach

Block diagram for implementation of narrow band filter is shown in Figure 2.

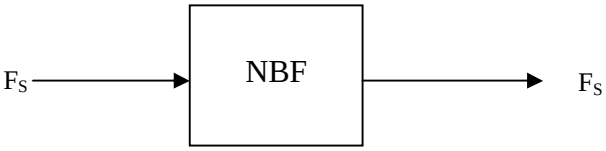


Figure 2: General diagram of narrow band filter

Transition width,

$$\Delta f\,(normalized)\ freq. = {f_s - f_p}/{F_S} \qquad (7)$$

Filter order N Filter order by Kaiser Formulation

$$N = -20\log\sqrt{\frac{\delta_s\delta_p - 13}{14.6\Delta f}} \qquad (8)$$

Filter order

$$N = 150$$

- **Multi-rate Approach**

The block diagram of multi-rate approach for implementation of narrowband filter is shown in Figure 3.

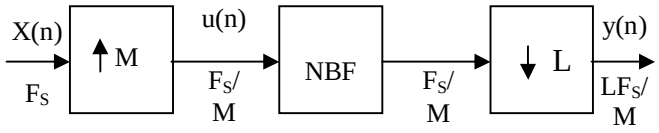


Figure 3: Diagram of the multistage for designing level

Suppose the sampling frequency of the narrowband filter is 125 Hz.

Down sampling factor M=2, Calculation of filter order of the decimator:

Specification of decimator:

$$\Delta f\,(normalized) = {(f_{s1} - f_p)}/{F_s}$$

$$f_{s1} = F_s - {F_s}/{2M}$$

$$\Delta f = .2467\,Hz$$

$$FilterOrder N1 = 9$$

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## VI. CONCLUSION

The narrowband filter is realized in FIR filter. Based on the direct approach, the filter requires 150 filter coefficients to meet the desired frequency response. To implement such a large order FIR filter in hardware involves large resources and sometime difficult to implement in resource constrained application. Keeping this in view, we have used Multi-rate approach to design the narrowband filter. We have used down sampling factor 2 and 4 for this purpose and found that, down sampling factor 4 requires significantly less filter constants than 2. To implement the narrowband filter, we therefore chosen down sampling factor 4 and designed the decimator, interpolator and narrowband filter.

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