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A Literature Review on Dynamic RAM

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ABSTRACT*:* The paper describes the thorough overview of DRAM . The review discusses basic introduction of DRAM , DRAM architecture and its support circuitry. The paper also focuses on the study of four transistor DRAM cell , two transistor DRAM cell and one transistor DRAM cell . Read and write operations of different types of DRAMs are explained with help of control signal waveform . The comparison between two basic types of memories i.e. SRAM and DRAM is also discussed in the paper. This paper also aims to study various fields of application where DRAM can be used.

KEYWORDS: DRAM ,SRAM , Precharge circuit , Sense amplifier.

I. INTRODUCTION

Performance of modern computer systems have seen dramatic improvements in the past thirty years due to advancements in silicon process technology. The advancements in silicon process technology have enabled the number of transistors on a single chip to roughly doubled every two years as suggested by Moore's Law. As a corollary to Moore's Law, processor performance has also double droughly every two years in the same time period due to a combination of the larger transistor budget and the increased switching speed of those transistors. However, increases in processor performance did not lead to comparable increases in performance of computer systems for all types of applications. The reason that increases in processor performance did not lead directly to comparable increases in computer system performance is that computer system performance is fundamentally constrained by the interaction between the processor and memory elements. Moreover, in contrast to the rapid improvements in processor performance, memory system performance has seen only relatively modest improvements in the past thirty years. The result of the imbalance in performance scaling trends between processor and memory is that modern computer systems are increasingly constrained by the performance of memory systems; in particular, the performance of DRAM based memory systems.

II. LITERATURE SURVEY ON DRAM

Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid operations on a memory device are reading the data stored in the device, writing (or storing) data in the device, and refreshing the data periodically. To improve efficiency and speed, a number of methods for reading and writing the memory have been developed. Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology.

III. DRAM ARCHITECTURE

DRAM chips are large, rectangular arrays of memory cells with support logic that is used for reading and writing data in the arrays, and refresh circuitry to maintain the integrity of stored data.

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Memory Arrays

Memory arrays are arranged in rows and columns of memory cells called word lines and bit lines, respectively. Each memory cell has a unique location or address defined by the intersection of a row and a column.

Memory Cells

A DRAM memory cell is a capacitor that is charged to produce a 1 or a 0. Over the years, several different structures have been used to create the memory cells on a chip. In today's technologies, trenches filled with dielectric material are used to create the capacitive storage element of the memory cell.

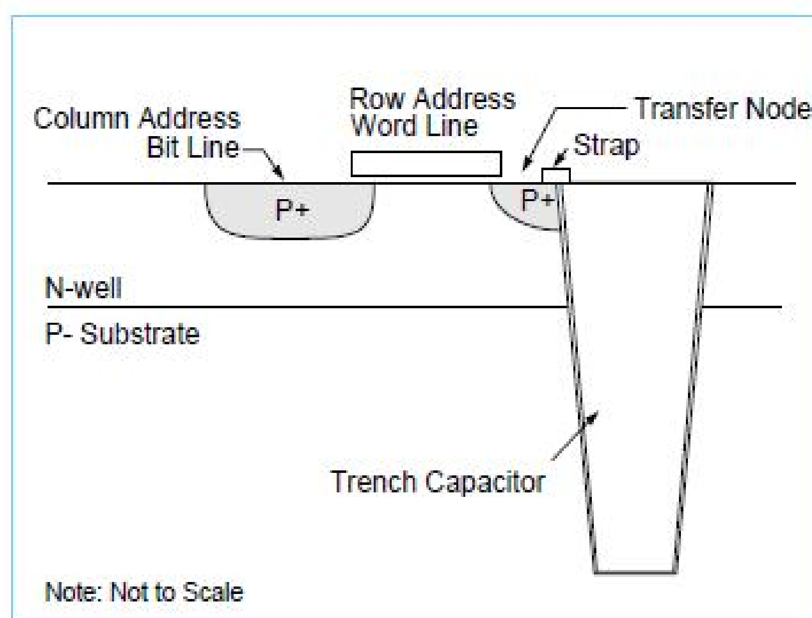

Fig. 1: IBM Trench Capacitor Memory Cell

Support Circuitry

The memory chip's support circuitry allows the user to read the data stored in the memory's cells, write to the memory cells, and refresh memory cells. This circuitry generally includes:

1. Sense amplifiers to amplify the signal or charge detected on a memory cell.
2. Address logic to select rows and columns.
3. Row Address Select (RAS) and Column
4. Address Select (CAS) logic to latch and resolve the row and column addresses and to initiate and terminate read and write operations.
5. Read and write circuitry to store information in the memory's cells or read that which is stored there.
6. Internal counters or registers to keep track of the refresh sequence, or to initiate refresh cycles as needed.
7. Output Enable logic to prevent data from appearing

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IV. DYNAMIC READ-WRITE MEMORY (DRAM) CIRCUITS

Various circuits of different types of DRAM cell are given in fig. 2.

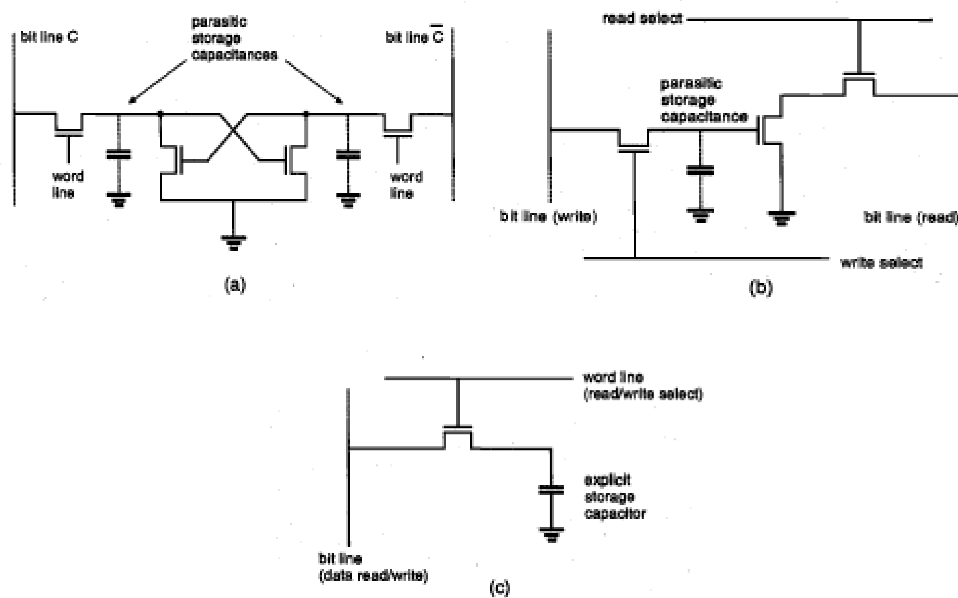

Fig. 2 Various configurations of the dynamic RAM cell.(a) Four-transistor DRAM cell with two storage nodes. (b) Three-transistor DRAM cell with two bit lines and two word lines. (c) One-transistor DRAM cell with one bit line and one word line.

A. Four-transistor cell

The four-transistor cell shown in Fig. 2(a) is the simplest and one of the earliest dynamic memory cells. This cell is derived from the six-transistor static RAM cell by removing the load devices. The cell has in fact two storage nodes, i.e., the parasitic oxide and diffusion capacitances of the nodes indicated in the circuit diagram. Since no current path is provided to the storage nodes for restoring the charge being lost to leakage, the cell must be refreshed periodically. It is obvious that the four-transistor dynamic RAM cell can have only a marginal area advantage over the six-transistor SRAM cell.

B. Three-Transistor DRAM Cell

The circuit diagram of a typical three-transistor dynamic RAM cell is shown in Fig. 3 as well as the column pull-up (precharge) transistors and the column read/write circuitry. Here, the binary information is stored in the form of charge in the parasitic node capacitance C_1. The storage transistor M2 is turned on or off depending on the charge stored in C_1, and the pass transistors Ml and M3 act as access switches for data read and write operations. The cell has two separate bit lines for "data read" and "data write," and two separate word lines to control the access transistors. The operation of the three-transistor DRAM cell and its peripheral circuitry is based on a two-phase non-overlapping clock scheme.

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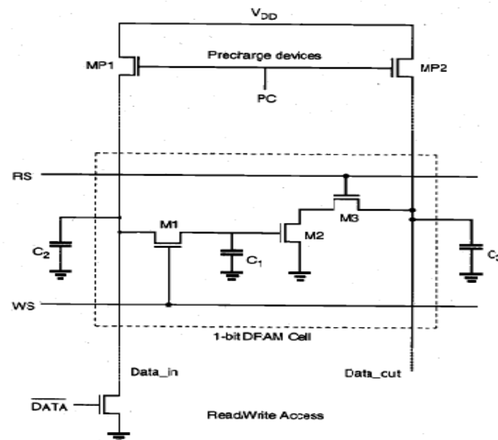

Fig. 3 Three-transistor DRAM cell with the pull-up and read/write circuitry.

The precharge events are driven by φ_1, whereas the "read" and "write" events are driven by φ_2. Every "data read" and "data write" operation is preceded by a precharge cycle, which is initiated with the precharge signal PC going high. During the precharge cycle, the column pull-up transistors are activated, and the corresponding column capacitances C_2 and $C_3$are charged up to logic-high level. With typical enhancement type nMOS pull-up transistors ($V_{TO=}$ 1.0 V) and a power supply voltage of 5 V, the voltage level of both columns after the precharge is approximately equal to 3.5 V.

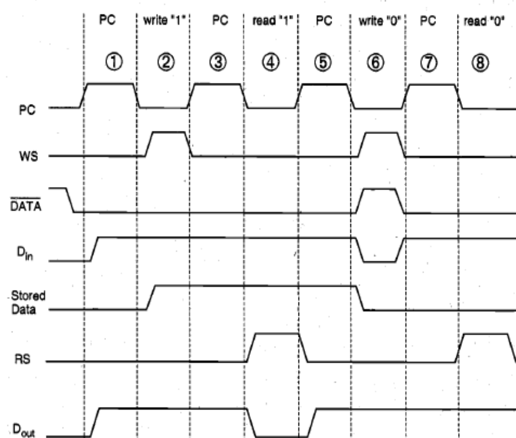

Fig.4 Typical voltage waveforms associated with the 3-T DRAM cell during four consecutive operations: write "1," read "1," write "0," and read "O."

All "data read" and "data write" operations are performed during the active ***2*** phase,i.e., when PC is low. Fig. 4 depicts the typical voltage waveforms associated with the 3-T DRAM cell during a sequence of four consecutive operations: write " 1," read "1," write "0," and read "0." The four precharge cycles shown in Fig. 4 are numbered 1, 3,5, and 7, respectively. The precharge cycle is effectively completed when both capacitance voltages reach their steady-state values. Note here that the two column capacitances C_2 and C_3 are at least one order of magnitude larger than the internal storage capacitance *C.*

C. One-Transistor DRAM Cell

The circuit diagram of the one-transistor (1-T) DRAM cell consisting of one explicit storage capacitor and one access transistor is shown in Fig.5. Here, C_1 represents the storage capacitor which typically has a value of 30 to 100 fF.

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Similar to the 3-T DRAM cell, binary data are stored as the presence or absence of charge in the storage capacitor. Capacitor C_2 represents the much larger parasitic column capacitance associated with the word line. Charge sharing between this large capacitance and the very small storage capacitance plays a very important role in the operation of the -T DRAM cell. The "data write" operation on the 1-T cell is quite straightforward. For the write "1" operation, the bit line (D) is raised to logic " 1 " by the write circuitry, while the selected word line is pulled high by the row address decoder. The access transistor Ml turns on, allowing the storage capacitor C_1 to charge up to a logic-high level. For the write "O" operation, the bit line (D) is pulled to logic "0" and the word line is pulled high by the row address decoder. In this case, the storage capacitor C_1 discharges through the' access transistor, resulting in a stored "0" bit.

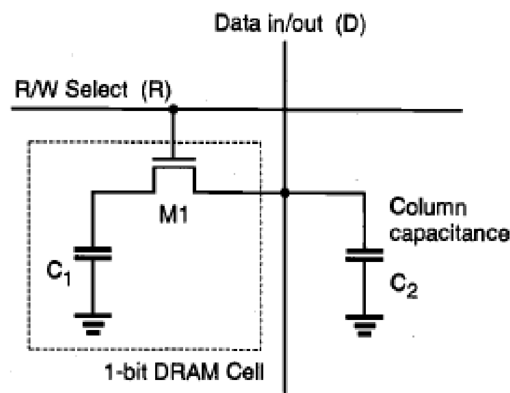

Fig. 5 Typical one-transistor (1-T) DRAM cell with its access lines

In order to read stored data out of a -T DRAM cell, on the other hand, we have to build a fairly elaborate read-refresh circuit. The reason for this is the fact that the "data read" operation on the one-transistor DRAM cell is by necessity a "destructive readout." This means that the stored data must be destroyed or lost during the read operation. Typically, the read operation starts with pre charging the column capacitance C_1. Then, 'the word line is pulled high in order to activate the access transistor Ml. Charge sharing between C_1 and C_2occurs and, depending on the amount of stored charge on C_1, the column voltage either increases or decreases slightly. Note that charge sharing inevitably destroys the stored charge on C_1. Hence, we also have to *refresh* data every time we perform a "data read" operation .An example of the 256-cells-per-column DRAM read circuitry is shown in Fig.6, along with typical control signal waveforms. A cross-coupled dynamic latch circuit is used to detect the small voltage differences and to restore the signal levels. The storage array is split in half so that equal capacitances are connected to each side of the cross-coupled latch. This means that half of the cells connected to one bit line (column) are arranged on one side of the latch, and the other half of the cells connected to the same column are arranged on the other side. As shown in Fig. 6, each half-column in the array also has a dummy cell which contains a capacitance half of the storage capacitance value. The capacitor C_D and C_D in Fig. 6 represent the relatively large parasitic column capacitances associated with the half-columns.

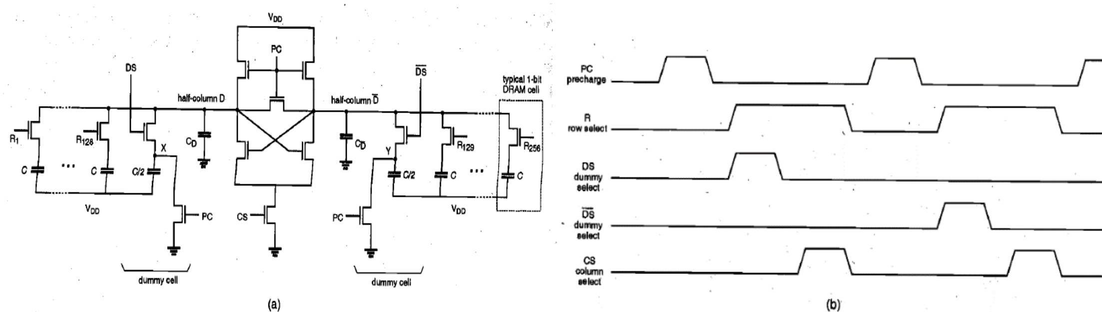

Fig. 6(a) Data read-restore circuit example for 256 -T DRAM cells per column. (b) Typical control signal waveforms for two consecutive data read operations, performed on alternate sides (half-columns) of the array.

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V. COMPARISON of DRAM W.r.t. SRAM

SRAM and DRAM are two basic types of RAM. The term SRAM stands for Static Random Access Memory and DRAM stands for Dynamic Random Access Memory. SRAM is made up of transistor and DRAM is made up of capacitor. Therefore a SRAM stores the binary bit inform of voltage; 5v represent 1 and 0v represents 0. DRAM stores binary bit in form of charge; presence of charge represent 1 and absence of charge (discharge) represent 0. The charge on the capacitor naturally leaks in few milliseconds. Therefore a DRAM need to be recharged (called refreshing a DRAM) periodically generally every 2 milliseconds. For this, a DRAM need a special refreshing circuit. DRAMs are cheaper than SRAMs and have high packing density. A DRAM consumes less power than a SRAM. They have lower speed than SRAMs. Cheaper DRAM is used in main memory while SRAM is commonly used in cache memory.

VI. CONCLUSION

The paper thoroughly explains the architecture of DRAM, circuitry of various cells of DRAM with their working operation. Comparison between SRAM and DRAM is also being made on the basis of their circuit, cost ,charge density, and applications. When SRAM because of its high cost can only be used as cache memory while low cost DRAM used as a main memory.

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