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A Novel High Speed Phase Acquainted Automatically Actuated Arbiter

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ABSTRACT: This paper proposes a novel approach to implement an arbiter for ML-AHB bus matrix to support three priority policies-fixed, round robin and dynamic and three data multiplexing modes-transfer, transaction and desired transfer length and also to sustain a clock frequency of more than 2GHz to produce 4 Giga data transfers per second. The proposed ML-AHB bus matrix uses slave side arbitration, since in this type, the master begins with a burst transaction of data and waits for the slaves response, this tailor under investigation is closely tied to increase the bandwidth. It is accomplished by integrating four 500 MHz synchronous memory, each of which exhibits 90 degree phase shift. A phase aware arbiter is designed for serving this purpose. As a result, we guarantee a maximum of one cycle communication latency to 32- 64 MHz processors connected to our infrastructure.

KEYWORDS: Multi Layer Advanced High Speed Bus (ML-AHB); internal arbiters (Phase Acquainted Arbiter and Automatically Actuated Arbiter); slave side arbitration; interconnect matrix; System on Chip (SoC)

I. INTRODUCTION

Although there are faster on chip shared buses of clock rates of the range of some hundreds of MHz, a good communication tailored material must also take care of increasing the performance of the bus (reducing interference), by choosing a favorable arbitration scheme. The Advanced Microcontroller Bus architecture described in this paper imparts significant improvements in speed along with reduced interference on a fully AHB infrastructure by providing data streaming via a shared memory. The former is achieved using an interconnect matrix that multiplexes several AHB masters interacting with a number of AHB slaves. Here special bridge architecture is designed so as to accomplish transferring between AHBs. When several slaves need to access the same resource, there is no bandwidth improvement when an interconnect matrix as depicted by ordinary ARM is used . However, when the proposed tailor consisting of several high speed bridges is used, an illusion that each clients' request was served with no apparent latency is being created. This is done using a phase aware arbiter, while the latter is achieved by selection of an arbitration scheme from the available number. In this venture, the ML-AHB uses slave side arbitration. The demerit of using master side arbitration is that, here only transfer based arbitration schemes are usable since it is a centralized arbiter. Moreover, the ML-AHB bus matrix of ARM uses only transfer based fixed priority and round robin arbitration schemes. This limitation on the arbitration scheme may lead to reduction in system performance, since, generally, the schemes are chosen according to the application. In slave side arbitration, both transfer and transaction based arbitration schemes can be dealt together. For the improvement of performance of the on chip bus, we thus propose a compatible arbiter which is self motivated. The slave mode arbitration scheme has the following merits.

i) Change in the priority policies during run time.

ii) Easy to turn the arbitration scheme according to the characteristics of the target application.

Therefore, our SM arbiter does not only deal with transfer based fixed priority, round robin and dynamic priority arbitration schemes but also comes up with transaction based fixed priority, round robin and dynamic priority schemes. Additionally, our SM arbiter also deals with choosing a scheme with desired transfer length based fixed priority, round robin and dynamic priority.

II. RELATED WORK

In [1] authors propose an interconnection architecture for a flexible on-chip high-performance communication medium that can provide variable bandwidth. It is based on the AHB AMBA bus. The proposed architecture has been

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implemented in the Seamless environment and laid out using a 0.18 μm CMOS with Cadence tools to validate the proposed concept. In [2] the author presents an on-chip interconnection infrastructure based on ARM's AHB standard to obtain a bus working beyond one gigahertz. In [3] the author proposed a multi-layer AHB bus matrix, a highly efficient on chip bus that allows parallel access paths between multiple masters and slaves in a system. However, the ML-AHB bus matrix of ARM offers only transfer-based fixed-priority and round-robin arbitration schemes. In [4] a stochastic approach for bus arbiter design which uses continuous-time Markov decision processes to get optimal arbitration policies and buffer space distribution. Data loss was reduced by 20% to 50% with redistribution of the buffer space. In [5] the multilayer advanced high-performance bus (ML-AHB) which employs slave-side arbitration is considered. Slave side arbitration is different from master-side arbitration in terms of request and grant signals since, in the former, the master merely starts a burst transaction and waits for the slave response to proceed to the next transfer that leads to the maximum performance, by 14%-62% compared to other schemes.

III. PROPOSED ALGORITHM

A. *Design and Description of Phase acquainted arbiter:*

For the study of operation of operation of bridges, it is important to understand the 2 GHz bus fabric. In this approach, we ensure only one cycle communication latency to all modules sharing the memory. For a high throughput of say, 2 GHz, as researched here, it is possible to achieve it by pipelining four 300 MHz synchronous memory with a 90 degree phase shift with respect to each other. A phase acquainted arbiter is used here to grant bus according to the memory phase required for the particular target address.

Here there are two types of bridges under consideration, one for the write operations and other for read operations. The illustration of 2GHz fabric architecture that sustains upto 4 Giga data transfers per second is shown in Fig. 1.

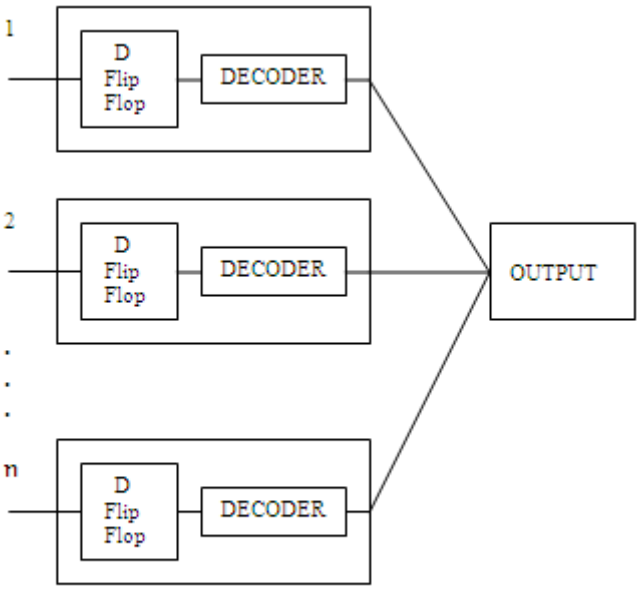

Fig.1. Structure of ML-AHB Bus matrix

IV. BRIDGE ARCHITECTURE

The bridge is the significant component in this matrix. As mentioned, it is of two types. The internal organization of the bridge is shown in Fig. 2. The bridge architecture shown in figure depicts the similarity of it with the conventional microprocessor containing a controller, a data path and the input-output interface.[6]

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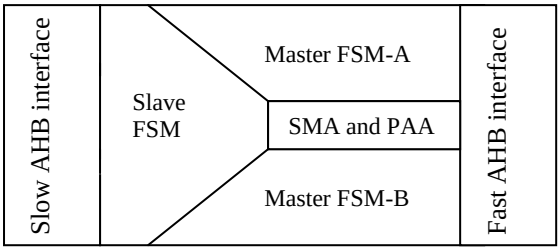

Fig.2 Internal organization of the bridge

It consists of 3 FSM and few internal arbiters. Slave FSM receives inputs from slow AHB interface. Now, it triggers one of the master FSMs through a synchronization register. Thus when a master FSM is launched, it initiates requests on 2 GHz AHB. Master FSMs A and B shall not be triggered at the same time. They work alternatively. But, it is also possible that one master FSM may stall upon the request of a positive grant signal. Here, when the other FSM is activated, a problem arises such that there are resource conflicts. This is overcome by our self- motivated arbiter which avoids first come first served basis and is capable of choosing the most suitable arbitration scheme for the problematic situation.

V. AUTOMATICALLY ACTUATED ARBITRATION SCHEMES

It is assumed that all the masters in the ML-AHB bus matrix system can change the priority level and the multiplexing modes and thereby can give a desired transfer length to the arbiters. Thus, the automatically actuated arbitration functions. This assumption should be valid because the system developer generally recognizes the features of the target applications [7]. For example, few masters in embedded system that are supposed to complete their job within the specified timing constraints are successful in satisfying the system-level timing constraints. In this venture, the process of predicting the computation time becomes easier but it is difficult to calculate the data transfer time since the on-chip bus is shared by several masters. Many works helped solving this problem by minimising the latencies of several latency-critical masters. There is another problem which arises here, i.e., these can increase the latencies of other masters; hence they may violate the given timing constraints . Unlike other works, in this issue, our scheme keeps the latency close to its given constraint by adjusting the priority level and transfer length of the masters.

In our system, we use a 32 bit address bus of the masters to inform the arbiters about the priority level and the desired transfer length of the masters. The Fig .3 depicts the internal structure of the arbiter for interference reduction part of our system. In the figure no-port signal indicates that none of the masters must be selected and the address and control signals to the shared slave must be driven to an inactive state. The master number gives the selected master (as generated by the controller for the automatically actuated arbitration scheme). The arbiter for the interface reduction consists of a RR block. A P block, two multiplexers, a counter, a controller and two flip-flops. The two multiplexers are used to select the arbitration scheme and the desired transfer length of a master. The counter calculates the transfer length, with two flip-flops being inserted to avoid attempts by critical path to arbitrate. The RR block (P block) performs the round robin or priority based arbitration scheme.

VI. CIRCUIT DESIGN

Generally, such high speed circuits are designed and implemented using full-custom design flow. In order to obtain clock rate of 2GHz with a low interference we use handcrafted designs. The various blocks are discussed below:

A. *Master Finite State Machine:*

For the purpose of reaching higher data rates with lesser interference, a larger circuit area is required. An FSM, firstly uses an one-hot encoding method [7]. Additionally, fast memory elements are required which are composed of the

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decision logic for allowing minimal logical depth. Fig.4 gives the operation of master FSM. There are three wait states resulting from the pipeline depth.

B. ***Synchronization register and internal arbitration:***

The AHB has two levels of pipelining; two transfers of different states are to be processed. For this, two master FSM machines are used in parallel for simplicity. The problem of which FSM should go first arises. The slave FSM thus is meant for triggering the two master FSMs. It continuously watches the incoming AHB's state changes and controls which master FSM is to be activated. The synchronization register is used to signal the master FSM, when to start.

To avoid the first come first served arbitration processes we go in for a self motivated arbiter which chooses one of the arbitration schemes from the available nine.

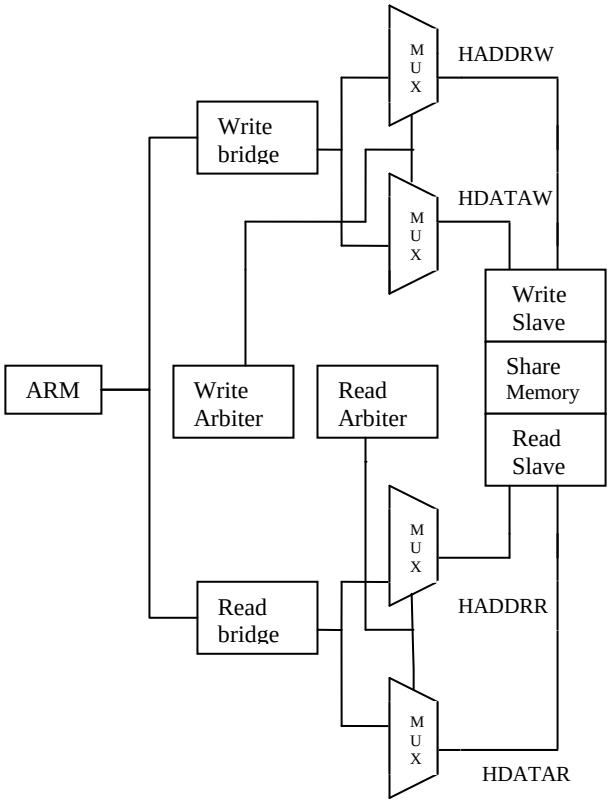

Fig.3. Communication Infra-Structure

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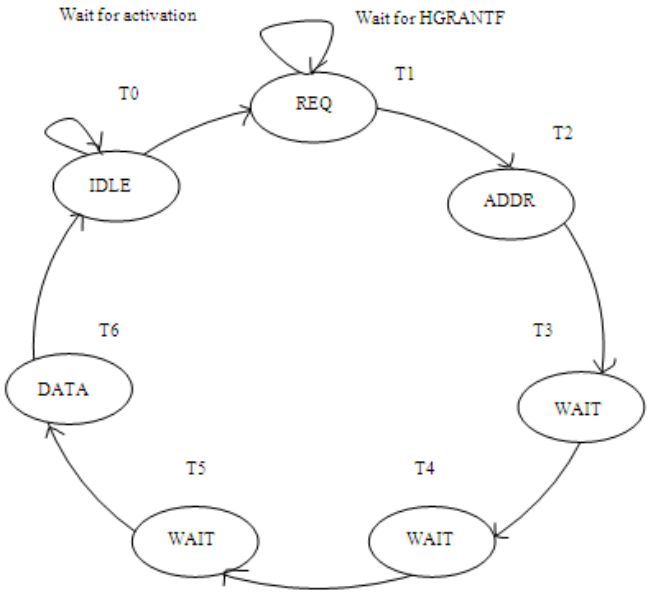

Fig.4. FSM operations

VII. CONCLUSION

In this paper, we presented a way to implement, a high performance (with increased clock rate and lower interference) system on chip platforms. The system uses a set of bridges to combine the multiple high frequency accesses. An automatically actuated arbiter was used to avoid the first come first served arbitration process which thereby, decreases the interference. A powerful, synchronization mechanism was designed to interconnect two buses of different clock rates. Finally, our objective is to obtain a clock frequency above 2GHz, can be implemented.

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BIOGRAPHY

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