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Performance Comparison of Different SRAM Cell Topologies and Design of NVLUT based on RRAM

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ABSTRACT: Static Random Access Memory (SRAM) is the most crucial part of memory that isimperative on simple and compound applications that implicate System on Chip (SoC) design. SRAM is a type of semiconductor memory and it has bistable latching circuitary which stores one bit of data either 0 or 1. SRAM is a volatile memory that retains data bits in its memory as long as the power is supplied.This work deals with simulation of five SRAM cell topologies i.e., 6T, 7T, 8T, 9T, 10T SRAM cells under 18nm technology. These SRAM cells actually stores one bit of data but for storing eight bits of data we have cascaded eight SRAM cells. The area of 6T and 7T SRAM cells is smaller i.e., $7nm^2$ and $8nm^2$ respectively and when we compare delay 8T SRAM cell and 9T SRAM is having less delay about 0.92ns and 0.87ns respectively. The 10T SRAM has more Read stability (RNM) when compared to other SRAM cells however the area and delay are more.Most of the FPGA's use SRAM cells to configure the Look up Tables but it is complex and volatile we designed Non Volatile Look Up Table (NVLUT) based on RRAM due to its simple structure, low switching voltage, fast switching speed, excellent scalability, great compatibility with the CMOS technology and area of RRAM is $51nm^2$, delay is 1.17nsec and power is 107.35pw.

KEYWORDS: SRAM, RRAM, NVLUT, 18nm technology,FPGA

I. INTRODUCTION

Static Random Access Memory (SRAM) stores data in the form of voltage. Static Random Access Memory (static RAM or SRAM) is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit either 0 or 1.The data in the SRAM is volatile i.e., the data is lost when the power is removed. They are made up of flip-flops. Static Random Access Memory is the faster form of RAM available because it doesn't need to refresh again and again. The stability and area of SRAM need to be concerned while a designing SRAM cell. SRAM cell must be able to write and read data and keep it as long as the power is applied. For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used.

II. RELATED WORK

In [1] authors characterised the performance of three SRAM cell topologies and their comparative analysis on the basis of Read NoiseMargin (RNM),Write Noise Margin (WNM) . They stated that the 6T SRAM provide very less RNM. To obtain higher RNM in 6T SRAM cell width of the pull down transistor has to be increased but this increases area of the SRAM which in turn increases the leakage currents. The 8T SRAM cell provide higher read noise margin. Due to asymmetric cell structure 8T SRAM cell may prone to failure during write operation. On the other hand 9T SRAM cell has higher RNM as well as WNM thus showing better stability performance as compare to 6T and 8T SRAM cell. In [2] authors characterised the performance of RRAM in which it has an advantage that it can be accessed randomly as well as it is a non volatile memory technology.They stated it is the most promising memory technologies in terms of

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storage density, non volatile behaviour and its property of resistance switching makes it more versatile in the field of data storehouse devices.

III.DESIGN OF SRAM CELL

6T SRAM cell: Each bit in an SRAM is stored on four transistors that form two cross- coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to a storage cell during read and write operation . A typical SRAM use six MOSFET to design a SRAM cell . In addition tosuch6TSRAM,otherkindsofSRAMchipsuse7T,8T,9T,10T,ormoretransistorsper bit. Access to the cell is enabled by the word line (WL in figure 1) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverseare typically provided in order to improve noise margins.

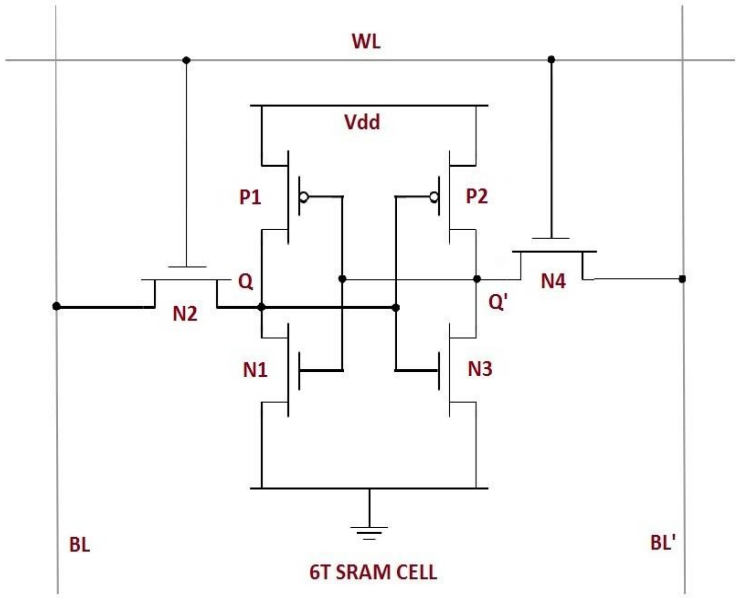

Fig 1: A 6T SRAM Circuit

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode should have "read stability".Due to high heat generation and high noise generation there is a chance of damaging the SRAM.

IV. DESIGN OF NVLUT BASED ON RRAM

Most of the current field-programmable gate arrays (FPGAs) use static random-access memory (SRAM) cells to configure the lookup tables (LUTs) and multiplexers (MUXs) in configurable logic blocks (CLBs) and routings. FPGAs in the core building block of logic-in- memory concept, but the inconsistency has been introduced based on the lookup table. Some proposals suggest using dynamic random-access memory (DRAM) cells instead, as it is not prone to soft errors, but SRAM cells are still widely used as they are faster than DRAM cells and require no refreshing. Due to reduce those drawbacks we have designed NVLUT based on RRAM and it is a non volatile memory even if the power is OFF the data will notlost.RRAM Slice constitutes of four ITIR RRAM cells at the left for configuration and a

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dummy RRAM cell at the right most as a reference resistor. The truth table is stored in the RRAM slice in the form of resistance state, ROFF or RON, which is different from the logic voltage in SRAM. The function of footer transistor mf is to allow current to flow during sensing and it is closed during pre charge to restrain leakage.

MRP(Matched Reference Path): It can be used to help to disabuse the parasitic resistance mismatch between the selected path in TMUX and reference path, their parasitic capacitance mismatch cannot be easily estimated and compensated. The MRP is devised to minimize the parasitic RC mismatch between the above-mentioned two paths. To illustrate this point, IN0 and IN1 are assumed to take the logic values of 0 and 1, respectively. As shown in Fig 2, the path marked by the green dash line in TMUX, P01,is selected to be compared with the reference path, Pref, For reliable sensing, the parasitic RCs of P01 and Pref should be equivalent.

TMUX (Terminal Multiplexer): TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding RRAM.

Single Stage Sense Voltage Amplifier: When there is any data read from memory it is used to sense low powersignals.

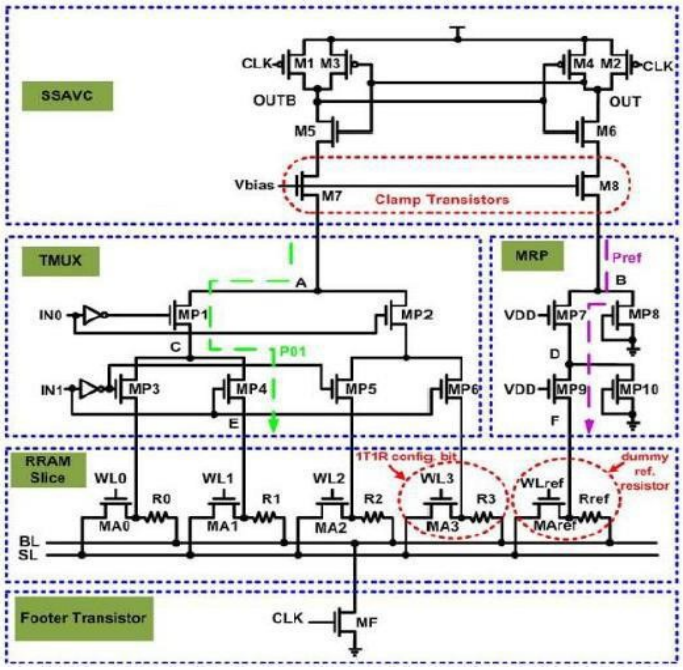

Fig 2:NVLUT based on RRAM

V.SIMULATION RESULTS

The Table. 1 shows the comparison of different SRAM cells. The 6T, 7T, 8T, 9T, 10T SRAM cells are simulated and compared the performance of these cells in terms of parameters like area, delay, power, read stability. The area of 6T and 7T SRAM cells is smaller i.e., $7nm^2$ and $8nm^2$ respectively and when we compare delay 8T SRAM cell and 9T SRAM is having less delay about 0.92ns and 0.87ns respectively whereas coming to Read Stability 10T SRAM cell has more stability. The 10T SRAM has more Read stability (RNM) when compared to other SRAM cells however the area and delay are more.

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Table 1: Comparison of SRAM cells

SRAM cell	Delay(ns)	RNM(v)	Area(nm^2)	Power(pw)
6T	1.31	0.9	7	39.81
7T	1.42	1.1	8	77.82
8T	0.92	1	10	39.56
9T	0.87	1	10	148.25
10T	1.81	1.5	14	154.527

The Fig 3 shows the Time Vs Voltage waveform for NVLUT based on RRAM. It has DC voltageoutput and two buffer inputs for transferring data and pulse inputs, two outputs (outA and outB) theseare clamping outputs which is either to lower or upper extreme. In non volatile Look Up Table we haveused twenty NMOS transistors and five PMOS transistors , two buffers as inputs and three pulse inputs, eightvoltage sources and print voltages for printing the inputs and outputs . The Area of NVLUT based on RRAM(Resistive Random Access Memory) is 51nm2 and delay of NVLUT based on RRAM is 1.17nsec

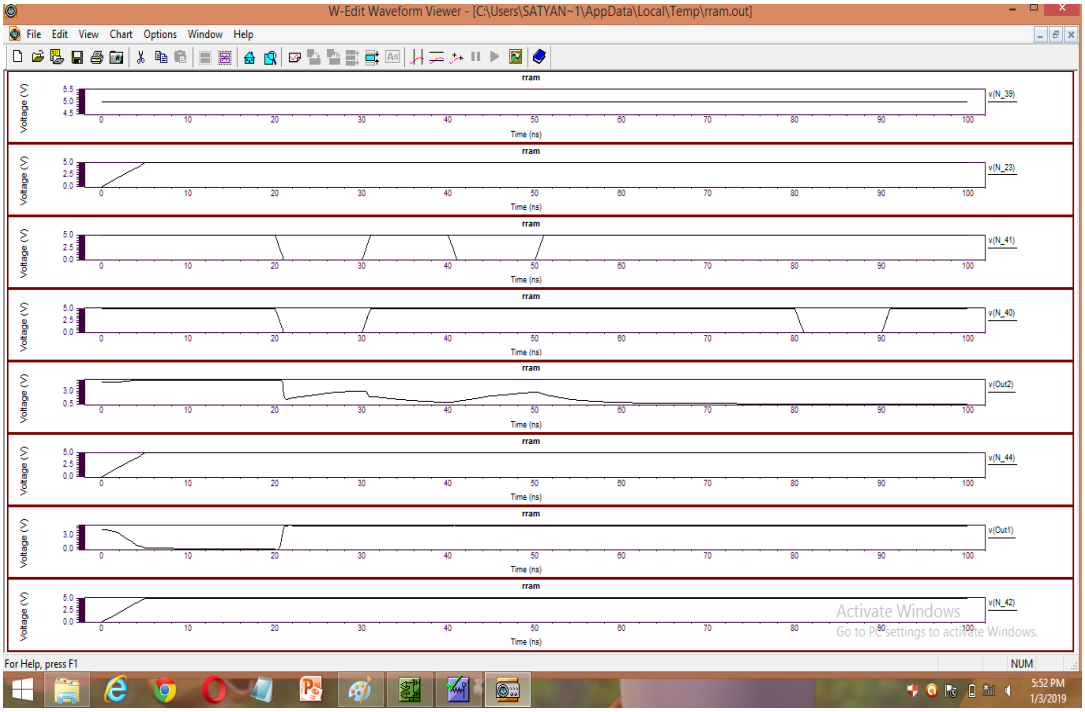

Fig 3: Time Vs Voltage waveform for NVLUT based on RRAM

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VI.CONCLUSIONS

This paper deals with the simulation of five SRAM cell topologies i.e., 6T, 7T, 8T, 9T, 10T SRAM cells which actually stores one bit of data and we have compared different parameters like area, delay, power, Read Noise Margin. For storing Eight bits of data we have cascaded eight SRAM cells. The area of 6T and 7T SRAM cells is smaller i.e., $7nm^2$ and $8nm^2$ and when we compare delay 8T SRAM cell and 9T SRAM is having less delay about 0.92ns and 0.87ns respectively whereas coming to Read Stability 10T SRAM cell has more stability. The 10T SRAM has more Read stability when compared to other SRAM cells however the area and delay are more. Most of the FPGA's use SRAM cells to configure the Look up Tables but it is complex and volatile we designed Non Volatile Look Up Table (NVLUT) based on RRAM due to its simple structure, low switching voltage, fast switching speed, excellent scalability, great compatibility with the CMOS technology.

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