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True Single Phase Clocked Flipflop with Low Power Consumption

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ABSTRACT:Energy-efficient retentive true single-phase-clocked (TSPC) FF is proposed in this work. The basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. With the employment of input-aware precharge scheme, the proposed TSPC FF precharge only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. Post layout simulations based on SMIC 45-nm CMOS technology show that at a supply voltage of different ranges 0.4V-1.5V Later, the flipflop is modified by adding SET, RESET, scan inputs and finally a soft error tolerant Flipflop is designed. The proposed designs are implemented in Tanner EDA using 45nm technology file. The existing method to implement this work, an energy-efficient retentive true single-phase-clocked (TSPC) FF is proposed.

KEYWORDS: Flip-flop (FF), low voltage operation, low-power, redundant-precharge-free, True-Single-Phase-Clocked (TSPC).

I. INTRODUCTION

The performance of digital systems is greatly improved with respect to the improvement in the process,power consumption has been the important limitation of digital systems. Secondly, with the rapid development of the Internet of Things (IoT), IoT devices are deployed on a large scale. As basic components, the power of flip-flops (FFs) accounts for a large part of the power of digital systems. As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area.

Power consumption is the most important limitation criteria of digital systems. As basic components, the power of FFs accounts for a large power of Digital systems. Thereby the power consumption in FF is reduced so that digital systems also reduce. Voltage scaling techniques proved to decrease the power consumption of Digital System. Inorder to design a FF of operating at both super threshold (vs) and near threshold supply voltage. Voltage scaling adjusting the supply voltage & the threshold voltage in CMOS logic circuits to control the total power dissipation in a block.

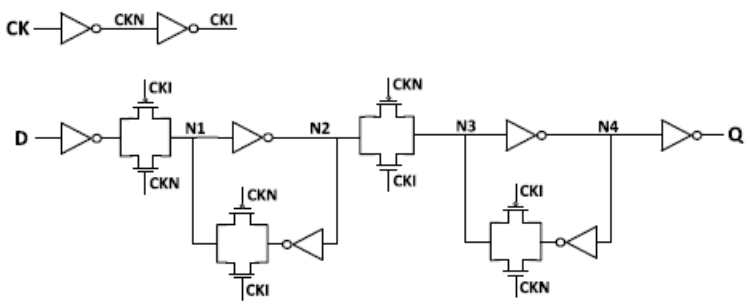

Fig 1: Schematic of TGFF

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TGFF: Transmission gate FF.
This is two phase clock (both CK and CKN are used). TGFF is the most widely used FF in current digital systems. TGFF is contention free FF which is suitable for sub threshold operation.
The main disadvantage of TGFF is the large clock network. Irrespective of what the input data is and those nodes drive a large no of transistor,the internal nodes Clock & clock bar toggle. Still with thesedisadvantages the Power Consumption of TGFF is large even if data activity is low. So, the usage of complementary clock signal should be optimised in order to reduce the power consumption of FF. After TGFF many low power single phase clocked FF's have been proposed in previous works. There are still some problems that affect the Power Consumption of FF's.

II. RELATED WORK

Forinstance, circuits of (13 - 18),(18) some of FF's failed at low supply voltage and some suffer at large Precharge power. In order to solve these problems, the proposed FF in the base paper should be suitable for wide range Supply Voltage Operation. In order to achieve this Redundant Precharge Operation is totally removed in the proposed FF and Power Consumption is further optimized compared with previous low power FF's.

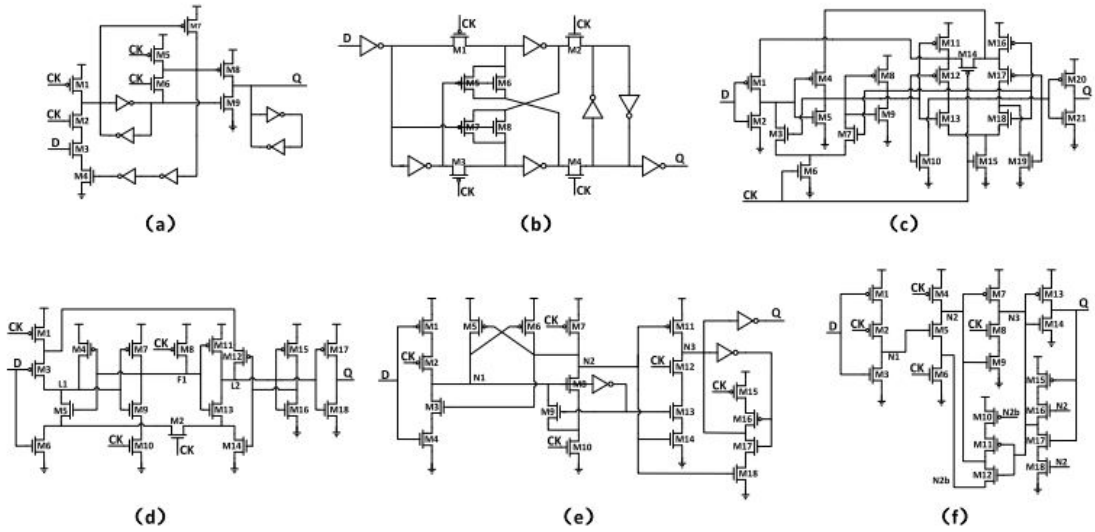

Fig 2. Schematic of various FF's (a) XCFF [13], (b) ACFF [14], (c) TCFF [15], (d) SPC-18 FF [16], (e) S^2CFF [17], (f) RTFF [18]

III. PROPOSED FLIPFLOP

Here, by minimizing the internal node transitions, the power consumption is minimized. Transitions of internal nodes should be removed in order to minimize the power consumption of FF+. We start with True Single Phase Clocked (TSPC) method and suitable for low voltage operations. To eliminate the redundant precharge and discharge operations, the FF is optimized by following steps. There are three steps involved in the structure of proposed FF. Initially, unnecessary precharge operation of the internal nodes is totally removed by the input-aware precharge scheme. Next, the floating node is under consideration to avoid short current which would greatly increase power consumption. In addition to this, unnecessary transistors are merged or removed to decrease the area.

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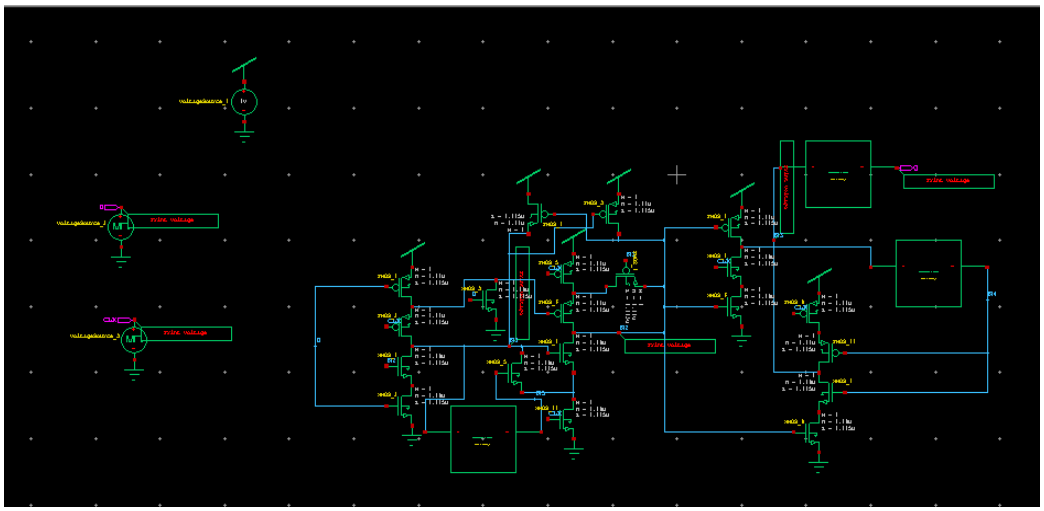

Fig 3. Schematic of the Proposed Flipflop

A. *Input Aware Precharge Scheme:*

When the Data is 0 the energy wasted operations i.e., the precharge path must be cut-off. A PMOS M1 is Controlled by inversion of input is inserted in to pre charge path. When Data is 1 PMOS M1 Will be ON. There by precharge operation works as usual. When Data is 0 PMOS M1 Will be OFF. There by precharge path is cut-off by the inserted transistor. As result the redundant precharge operation is totally removed.

B. *Floating Node Analysis:*

The voltage of floating nodes may after transition due to leakage current.so floating node analysis carefully analysed the floating nodes in order to avoid the generation of short circuit path. By the insertion of input aware precharge scheme, the voltage at N2 is no longer precharge from Vdd at the negative half of clock when the input is zero.

CASE 1: When the output Q=1 where N3=0.N3 is maintained by M9 and M10, Here M3 is in OFF state & M10 is ON state. For this N2 needs to be High-1. When the next data is zero, in order to avoid flotation of node N2. M2 is inserted to keep the voltage of N2. N2 transistor is controlled by N3 and provides a precharge path for N2.

CASE 2:When output =0 where N3=1, which is maintained by M7 & M8. When input is zero, then N2=0. It doesn't get charge to high. When clock is zero, then there is only effect is M3 is ON and its doesn't lead to any short circuit path. Now when N3=1, Clock =0, Data=0. At N3, N4, N5 are isolated. Therefore, N2 has no effect on N3. Similarly, at N1, M14, M13 are isolated. since Data=0 and therefore N2 has no effect on N1. Node N1 and N3 are independent of N2. The floating of the node N2 is negligible.

C. *Transistor level Optimization:*

Now the function Flipflop is in good condition so and precharge is removed after adopting the input aware precharge scheme and floating node analysis. But flipflops can be further removed. The PMOS 11_1 can be merged into M11, PMOS 11_1 is used to generate the inversion of data which can be done by M4 but M14 and M15 can't be merged because based on N2. Incase M14 and M4 are merged then the data of M11 and M14 are connected then it leads to the failures of flipflops, so M15 is reserved. And now in our true singled phased clock, M13 from before S^2CFF at which M4 and M5 in true singled phased clock is removed in S^2CFF M13 is used to prevent the glitches in two singled phased clock N2 doesn't need to precharge once data is zero because N2 is retentively low, the output will not have any glitches when transistor is removed.

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OPERATION:

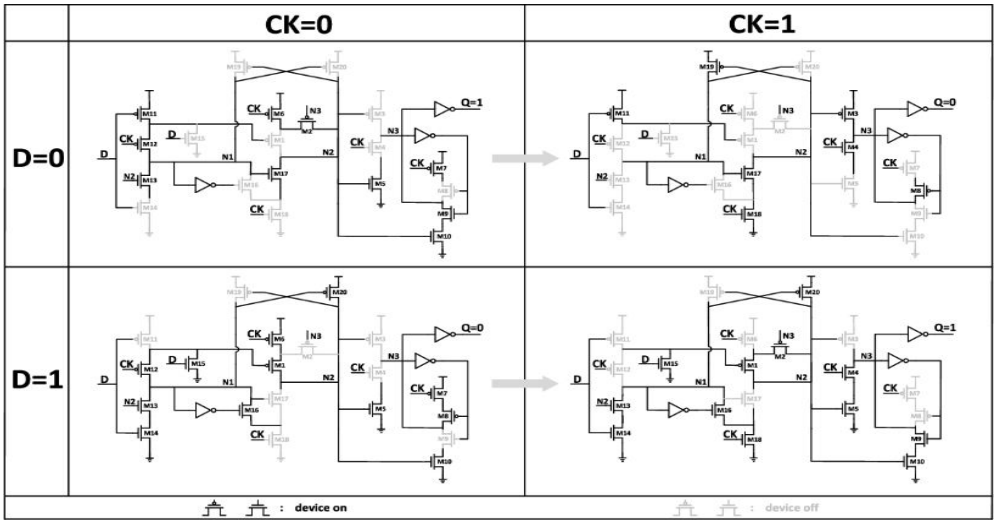

Fig 4. Operation Diagram of Proposed FF at different DATA (D) and CLOCK (CK)

CASE-1: HIGH TO LOW TRANSISTION (OUTPUT 1-0);
When ck=0; N1 is charged through M11 & M12. N2 is charged through VDD from M6 & M2.N3 will be low through ground M9 & M10, then Q=1; D=0. Now at rising edge of ck=1; N1 keeps high through M19. N2 is low through ground M17 & M18; and M13 is off because these isolate the Flip flop from changes in the input data. N3 is charged to VDD through M3, then N3=1 and then Q=0, D=0.
CASE-2: LOW TO HIGH TRANSITION (OUTPUT 0-1);
When ck=0; N1 is discharged through M13 & M14. N2 is charged through M6 & M1. N3 is high through M7 & M8; So, output Q=0. When ck=1; N1 keeps low through M16 & M18. N2 keeps high through M20 as the ½ cycle of ck. N3 is discharged; then Q=1.

ADDITIONAL FUNCTIONS OF THE PROPOSED FF:
The Functions are SET, RESET and SCAN are added to the main circuit so the three different circuits are implemented. Which can be easily added to the proposed FF.
SET:
It is an external triggered. When the signal is applied, the flip flop is triggered to high state at Q. It remains to be same value, hold until low input signal is given at reset pin. Set can also be called as PRESET. In general, it refers to forcing an output stage to a logical "1".
Case 1: When set is high.

- Q = high
- N1= low
- N2= high
- N3= low

Case 2:

- When set is low
- The flip flop acts as original flip flop.

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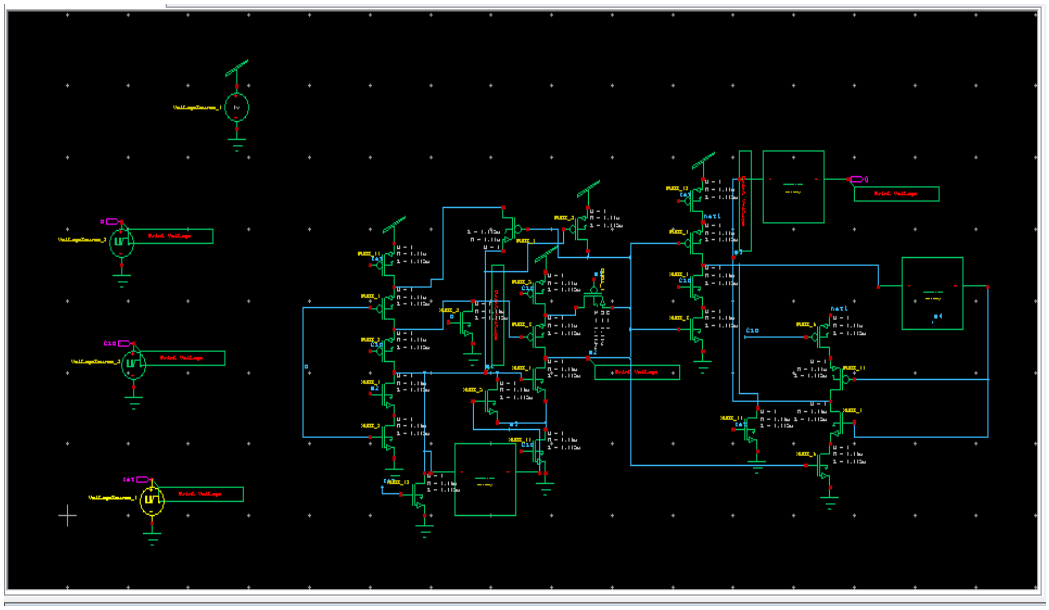

Fig 5. Schematic of the proposed FF with SET

RESET:It is an external triggered. RESET produces a change of state at Q. When reset signal is applied, the flip flop is triggered to low state at Q. It remained high in set, until reset function is applied to the circuit. In reset function, output is remained to be low i.e., 0.

RESET can be caller also as CLEAR. In general, it is referred to forcing an output stage to logic "1".

Case 1:

- When reset is high
- Q = low
- N1= high
- N2= low
- N3= high

Case 2:

- When reset is low
- The flip flop acts as original flip flop.

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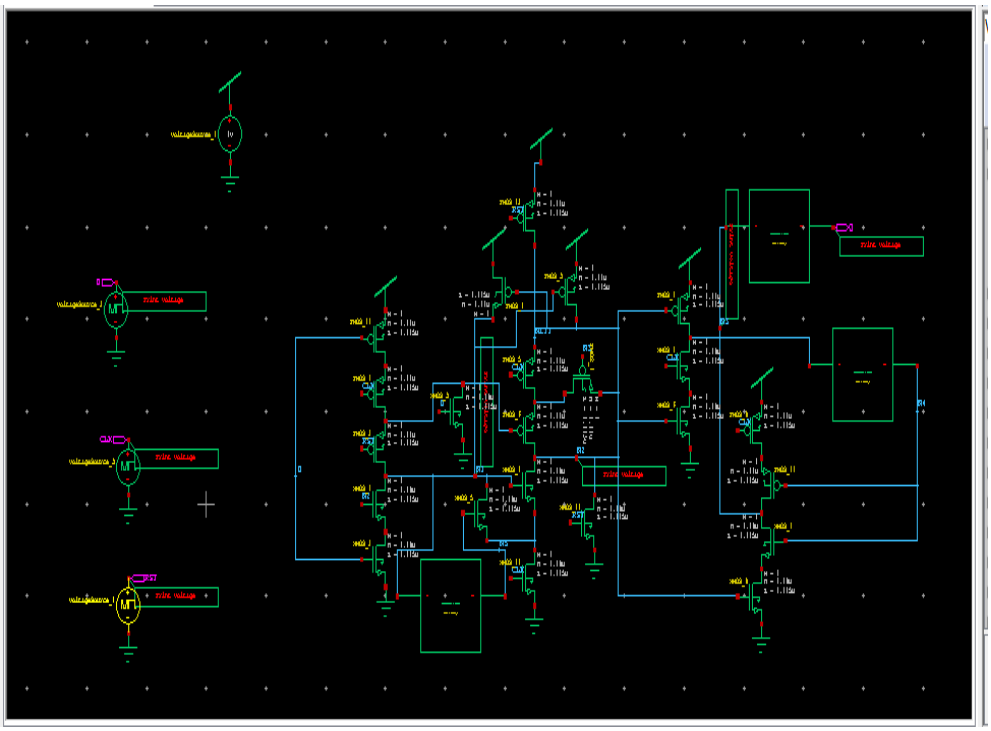

Fig 6. Schematic of the proposed FF with RESET

SCAN:The scan is an addition function which is used to control the flip flop.By using scan input we can obtain the output which can be modified by accordingly.

Case 1:

- When SE=0 and SEN=1.
- The flip flop acts as an original flip flop.

Case 2:

- When SI=1 and SEN =0.
- Then the output depends upon CLK and SI.

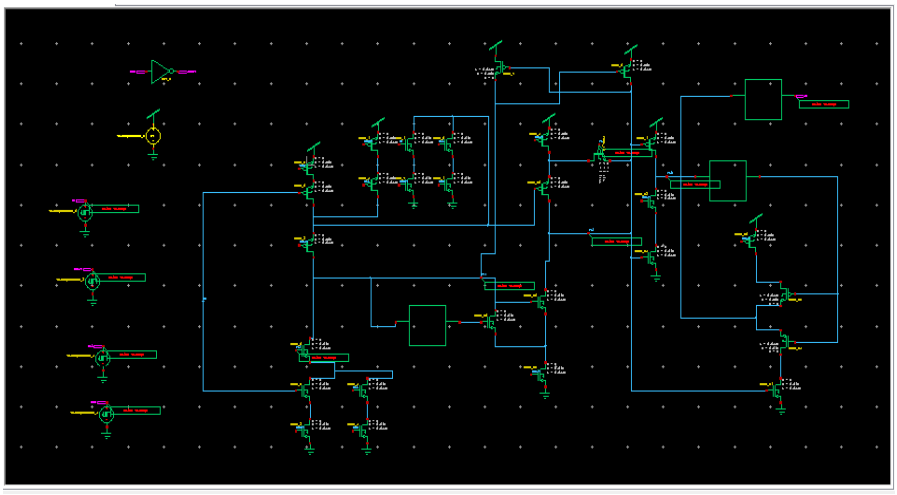

Fig 7. Schematic of the proposed FF with SCAN

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SOFT-ERROR TOLERANT OPTIMIZATION OF THE PROPOSED FF:

Soft-Error Tolerant Optimization of the Proposed FF Although scaling down the supply voltage can significantly decrease the power consumption of digital systems; aggressive voltage scaling will increase the soft error susceptibility of the systems. In order to improve the stability of low-voltage systems, the proposed FF can be hardened to resist the single event effect (SEE), which includes single event upset (SEU) and single event transient (SET). By using C-elementbased logic, the proposed FF can be insensitive to SEUs. The schematic of the proposed SEU-tolerant FF is shown in figure. The proposed SEU-tolerant FF achieves complete SEU masking. As for SETs at the input ports, the proposed FF can use the element-based temporal filter in to harden the input ports D and CK.

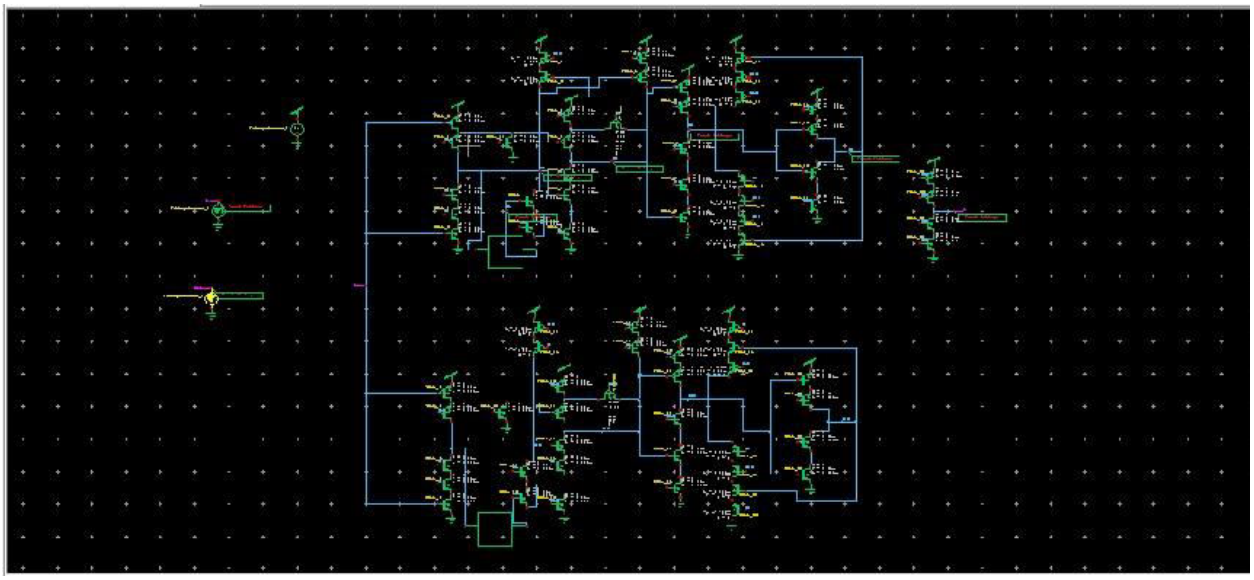

Fig 8. Schematic of the proposed SUE-tolerant FF.

To validate the benefit of the proposed FF in the real digital circuit, five 16-bit counters based on TGFF, S2CFF, ACFF, transmission-gate-pulsed latch (TGPL), and the proposed FF are designed for comparison. As shown in Table V, the counter based on the proposed FF has the lowest power consumption among these designs. However, since the complementary clock signals are still required in the latch, the power of the TGPL-based counter is still significantly larger than that of the counter based on the proposed FF. Since the maximum frequency is related to the D-to-Q delay of the sequencing element, the counter based on TGPL has the largest maximum frequency due to its negative setup time, but TGPL is not suitable for low voltage circuits due to the enlarged variability of the pulsed width at low supply voltage as described.Also, the TGPL-based circuit shares a pulse generator to reduce power consumption, and the pulsewidth will change during propagation, which will further increase the uncertainty of the pulsewidth. Since the D-to-Q delay of the proposed FF is slightly smaller than that of ACFF, the maximum frequency of the counter based on the proposed FF is a little larger than that of the ACFF-based counter. Since the area of the proposed FF is just 4.8% larger than that of TGFF, the area of the counter based on the proposed FF is just 5.2% larger than that of the TGFF-based counter.

IV. SIMULATION RESULTS

The simulation results of the proposed flipflop are obtained from the Tanner EDA tool using 45nm Technology. The timing waveforms of the Flipflop are obtained from the simulation of flipflop circuit varying its supply voltage from 0.4v-1.5v.

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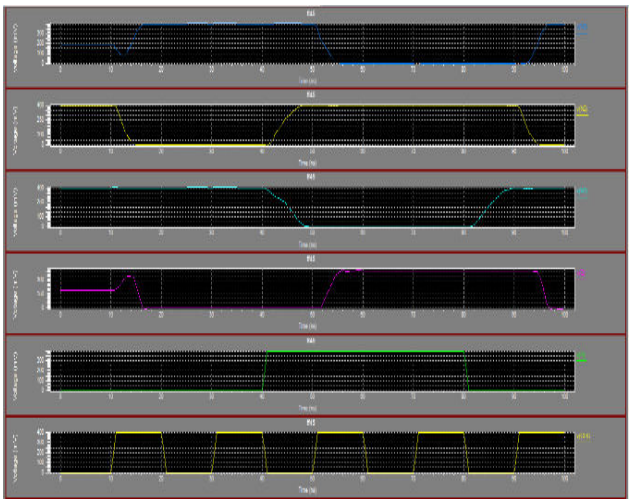

Fig 9. Timing Waveform of fig1 at 0.4 supply voltage

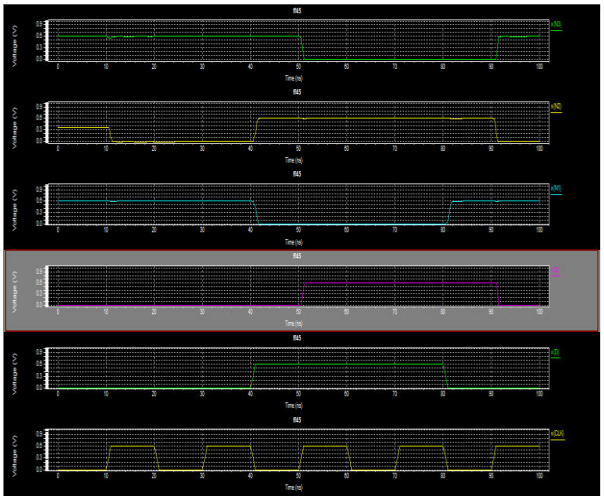

Fig 10. Timing Waveform of fig1 at 0.6 supply voltage

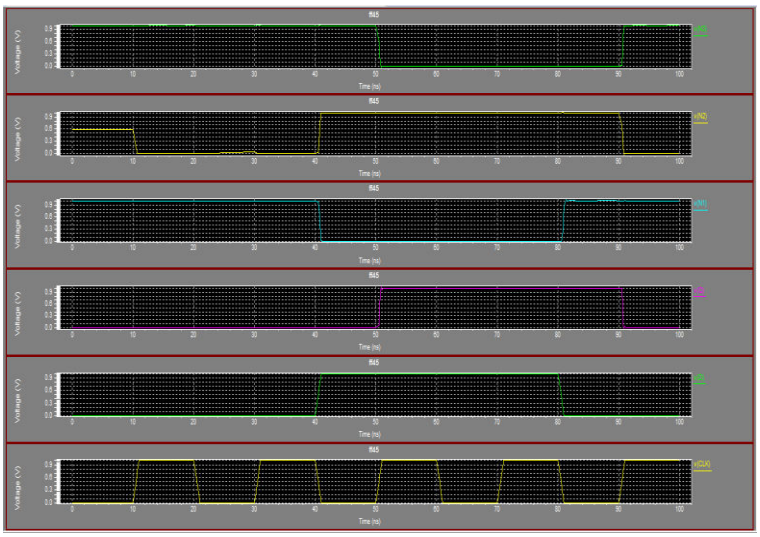

Fig 11. Timing Waveform of fig1 at 1.0 supply voltage

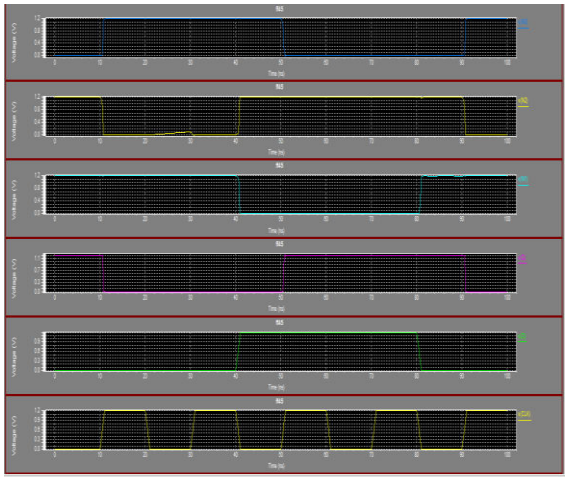

Fig 12. Timing Waveform of fig1 at 1.2 supply voltage

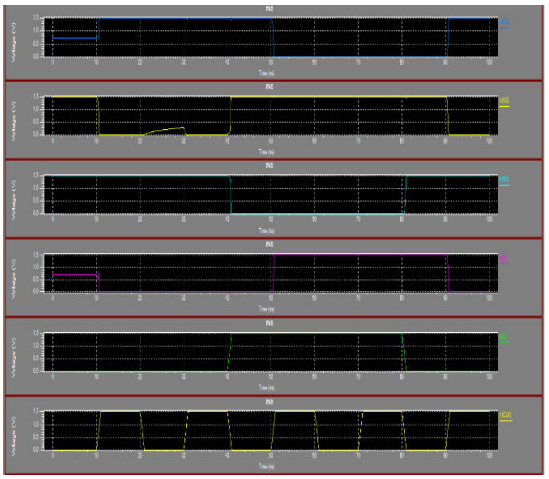

Fig 13. Timing Waveform of fig1 at 1.5 supply voltage

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The below simulated output waveform is the Transient Wavwforms of the proposed SEU-tolerant FF with several SEU's at the internal nodes.

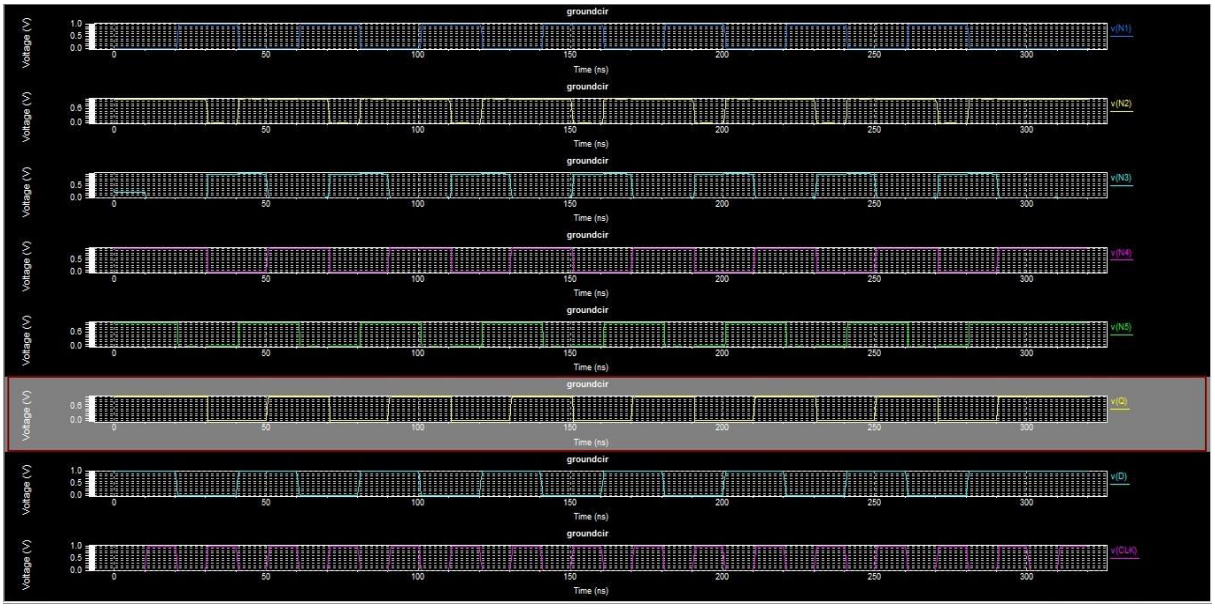

Fig 14. Timing Waveform of SEU-tolerant FF at different nodes

V. FUTURE SCOPE OF WORK

The glitches are observed at the output's waveforms of the proposed FF at 0.4v Supply voltage. This Effect is also called as the GROUND BOUNCE EFFECT as to avoid the bouncing of the simulation outputs at lower supply voltages. So, to increase the wide range voltages with low power consumption the threshold voltage of the models is varied to obtain the glitch free outputs of the flipflop.

The threshold voltage in the used model of 45nm technology is 0.466v and it is decreased till 0.300 to obtain the error and bounces free output for a very low voltage od 0.4V supply voltage.

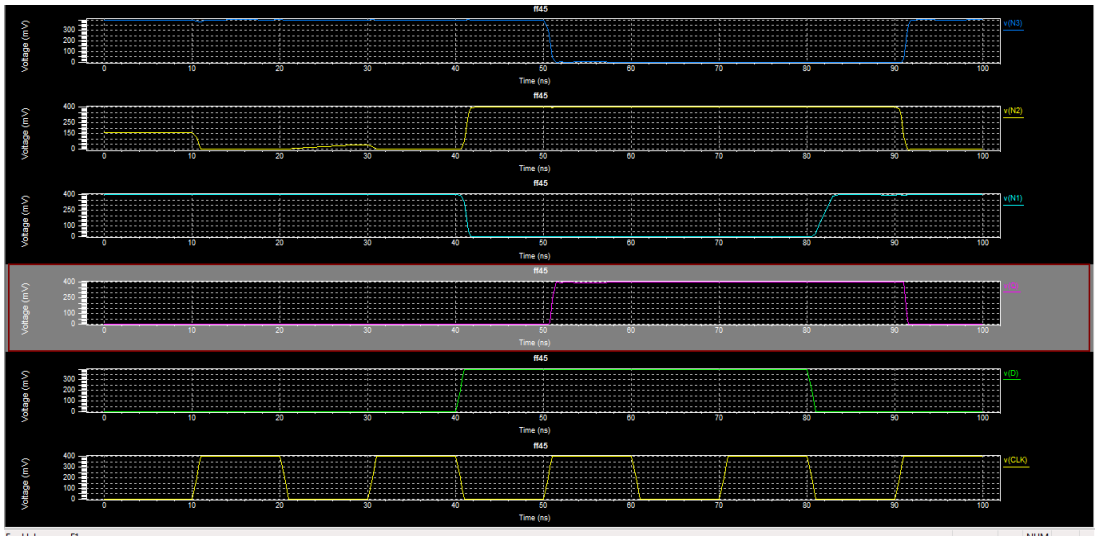

Fig 15. Timing Waveform of proposed FF at 0.4V supply voltage after changing Threshold Voltage

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VI. CONCLUSION

An energy-efficient retentive TSPC FF is proposed in the paper. The input-aware precharge approach considerably reduces the power of the proposed FF by eliminating superfluous precharge and discharge procedures. The proposed structure is also subjected to floating node analysis to prevent the formation of short-circuit routes. The circuit is then optimized at the transistor level to further reduce its size and power usage. According to post layout simulation results, the suggested FF consumes less power than TGFF with less than 10% data activity Since Flip flops are one of the most complex and power consuming component among the various building blocks in digital designs and Clocking network and flip flops consume about 30 to 70 % of total power in the system out of which 90 % is consumed by flip flop. In some circuits it is the main aim to reduce the area and reduce the delay, at that time the 5T Flip Flop is preferred. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. As True Single-Phase Clocking (TSPC) flip-flop design has small area and low power consumption. And it can be used in various applications like digital VLSI clocking system, microprocessors, buffers etc. The analysis for various flip-flops for power dissipation and propagation delay has been carried out at different foundries.

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