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A Low-Power Parallel Architecture for Linear Feedback Shift Registers

A. Dhanunjaya Rao[1], G. Mallikarjuna Rao[2], D. Saikumar[3], G. Vkias Roy[4], K. Sandhya Rani[5]

U.G Students, Dept. of Electronics and Communications Engineering, Vasireddy Venkatadri Institute of Technology, Nambur, Guntur, Andhra Pradesh, India [1-4]

Assistant Professor, Dept. of Electronics and Communications Engineering, Vasireddy Venkatadri Institute of Technology, Nambur, Guntur, Andhra Pradesh, India [5]

ABSTRACT: Linear Feedback Shift Registerhave wider applications in communication at transmitting and receiving ends. In the VLSI design technology, the power consumption by the chip or the most important thing to consider. The Designs which consume less power will have higher demand and have high advantages than the other. We propose alternative transformation matrix construction which will be active for each and every clock cycle. The power consumption of the design also depends upon the total number of gate count. If the gate count increases then the total power consumption by the design is also increases. The gate count in the design has been reduced by the substructure sharing. The proposed design of linear feedback shift register consumes less power and gate count is also reduced.

KEYWORDS: Linear Feedback Shift Register(LFSR), Transformation matrix, Substructure Sharing(SS), Cyclic Redundancy Check(CRC).

I. INTRODUCTION

Linear feedback shift registers are the random test pattern generators these are used in Built in self-test method used for testing the integrated circuits in VLSI. Linear Feedback Shift Registers has many applications in communications field also where the Cyclic redundancy check is similar to Linear Feedback Shift Register. The Cyclic Redundancy Check performs the error detection at the receiving end. The Architecture of the Linear Feedback Shift Register Involves the basics components of digital electronics like D-Flip Flops and XOR gates as feedback network.

II. LINEAR FEEDBACK SHIFT REGISTER (LFSR)

A linear feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state. The bits in the LFSR state which influence the input are called taps.A maximum-length LFSR produces an m-sequence (i.e., it cycles through all possible 2^{n-1} states within the shift register except the state where all bits are zero), unless it contains all zeros, in which case it will never change. As an alternative to the XOR based feedback in a standard LFSR, one can also use XNOR.For XOR gate used in the feedback path all the zeroes are avoided and for XNOR gate as feedback path all ones are to be avoided because they are “locked up” state.

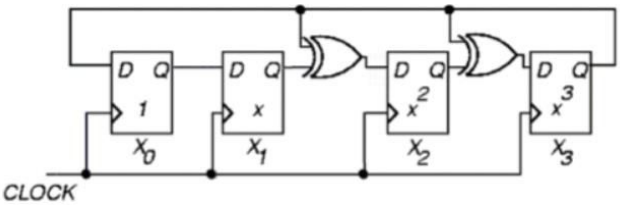

Figure 1: Linear Feedback Shift register

The total patterns generated by the linear feedback shift register are shown except the locked-up states

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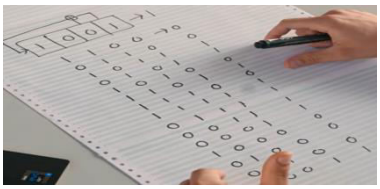

Figure 2: Bit Linear Feedback Shift Register Random Patterns

III. P-PARALLEL LFSR ARCHITECTURE

Let us consider the serial Linear Feedback Shift Register architecture as shown below

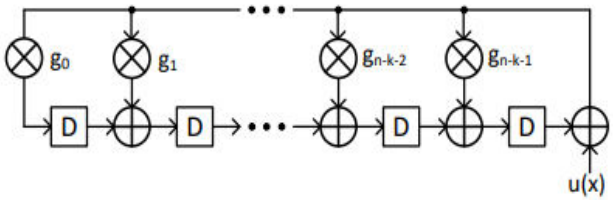

Figure 3: Serial Linear Feedback Shift Register

The serial LFSR shown in Fig. 3 is configured using a generator polynomial $g(x) = x^{n-k} + g_{n-k-1}\ x^{n-k-1} + \cdots + g_1\ x+g0$. For binary BCH codes and CRC, the coefficients are binary. When the input u(x) is added to the most significant tap, this LFSR implements the division of u(x)x n−k by g(x). Only the remainder r(x) is of interest to BCH encoding and CRC. The coefficients of u(x) are input serially starting with the most significant one, and r(x) is located in the registers after the last coefficient of u(x) is sent in.

Denote the register states at clock cycle t by $r(t) = [r_{n-k-1}(t), r_{n-k-2}(t), \cdots, r_0(t)]`$ , where ‘ ` ’ represents transpose. Let u(t) be the input at clock cycle t. Then $r(t + 1) = A \times r(t) + b \times u(t)$.

where **A** is a companion matrix

$$\mathbf{A} = \begin{bmatrix} g_{n-k-1} & 1 & 0 & \cdots & 0 \\ g_{n-k-2} & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ g_1 & 0 & 0 & \cdots & 1 \\ g_0 & 0 & 0 & \cdots & 0 \end{bmatrix}$$

Figure 4: Companion Matrix

$b = [g_{n-k-1}, \cdots, g_1, g_0]`$ After ‘p’ times =>$r(t + p) = A_p \times r(t) + B_p \times u_p(t)$.A p-parallel LFSR that processes p bits in each clock cycle can be implemented according to the above. But the transformed state vector as $r(t) = T \times rT(t)$and transformed equation for the p-parallel architecture is

$$r_T(t + p) = A_{pT} \times r_T(t) + B_{pT} \times u_p(t),$$

where $A_{pT} = T^{-1} \times A_p \times T$, $B_{pT} = T^{-1} \times B_p$

BpT and ApT are also referred to as the pre-processing and feedback matrices, respectively.A block diagram for implementing such a transformed p-parallel LFSR is shown in Fig. 5

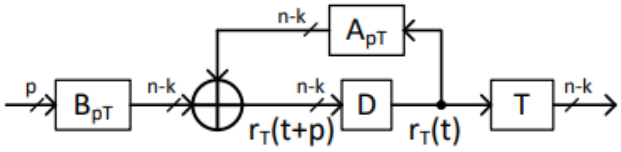

Figure 5: Transformed P-Parallel Architecture

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IV. POWER OPTIMIZATION IN COMPUTATION

This design spends a higher portion of the gates on the pre-processing (B_{pT}) and feedback matrix (A_{pT}) multiplications. These multiplications are active in every clock cycle, while the T matrix multiplication is only done for one clock cycle at the end. The dynamic power consumption can be compared by the number of logic gates switching in each clock cycle. One effective way to lower the power consumption is to reduce the gate counts of B_{pT} and A_{pT} , even though T ends up having more gates. Exhaustive search can be carried out to find T^{-1} that minimizes the gate count of B_{pt}. T is determined from T^{-1} . Although the gate count of A_{pT} may not be minimized, having the lowest gate count in the $T^{-1}\times A_p$ part also helps to reduce the complexity of A_{pT} multiplication. To define a valid transformation, the only requirement on T^{-1} or T is that it must be invertible. The search is reduced to the first column or row, and the other columns or rows are derived by shifting and modulo reduction. Our search is done on T^{-1} instead. Also the later rows of T^{-1} are not derived from the first row just in order to reduce the search complexity. Instead, the goal is to minimize the weight of each row in B_{pT}. The number of XOR gates needed to implement a matrix multiplication can be reduced by SS, which means common intermediate results among multiple outputs are computed once and shared. Nevertheless, comparing the row weights often gives a good indication of which matrix multiplication requires less logic gates. Our proposed T^{-1} is in the following format.

$$\mathbf{T}^{-1} = \begin{bmatrix} 0 & 0 & \cdots & 0 & 0 & 1 \\ 0 & 0 & \cdots & 0 & 1 & t_{1,0} \\ 0 & 0 & \cdots & 1 & t_{2,1} & t_{2,0} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 1 & \cdots & t_{n-k-2,2} & t_{n-k-2,1} & t_{n-k-2,0} \\ 1 & t_{n-k-1,n-k-2} \cdots & & t_{n-k-1,2} & t_{n-k-1,1} & t_{n-k-1,0} \end{bmatrix}$$

Figure 6: Inverse Transformation matrix

Such a lower anti-triangular matrix with the anti-diagonal set to all '1's guarantees that T^{-1} is invertible. It is also possible to use a lower triangular, upper triangular, or upper anti-triangular format for T^{-1}.

V. SUB STRUCTURE SHARING

Substructure, also called a common term, appears in multiple output formulas, then this substructure only needs to be computed once and it can be shared in the computations of multiple outputs. The complexity of constant matrix multiplications is more accurately estimated by applying SS. The SS for achieving optimal gate count reduction is an NP-complete problem. Also, different SS schemes lead to trade-offs on the gate count and CPD. To achieve high clock frequency in parallel LFSRs, SS needs to be applied with constraints on the CPD. Although many SS schemes targeting at gate count reduction have been proposed, only a few of them address the critical path issue associated with sharing substructures.

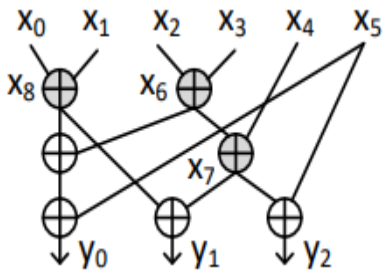

Figure 7: Example for Substructure Sharing

Consider an example that computes $y_0 = x_0 + x_1 + x_2 + x_3 + x_5$, $y_1 = x_0 + x_1 + x_2 + x_3 + x_4$, and $y_2 = x_2 + x_3 + x_4 + x_5$. The substructures identified for sharing in iteration 1, 2, and 3 are $x_6 = x_2 + x_3$, $x_7 = x_6 + x_4$ and $x_8 = x_0 + x_1$, respectively. The SS can be expressed by a graph as shown in Fig. 6.

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VI. TOOLS

The tool used for the implementation of the design is Xilinx 14.7 ISE DESIGN SUITE which contains various standard IEEE libraries. The hardware description language used is VHDL for the proposed design. The simulation analysis and synthesis analysis can be done. The total power consumption by the design can be analyzed in the Analyze power distribution option in the software.

Figure 8: Xilinx ISE design suite

VII. EXPERIMENTAL RESULTS

The Simulation results of the proposed design for some inputs has been shown in the below figures

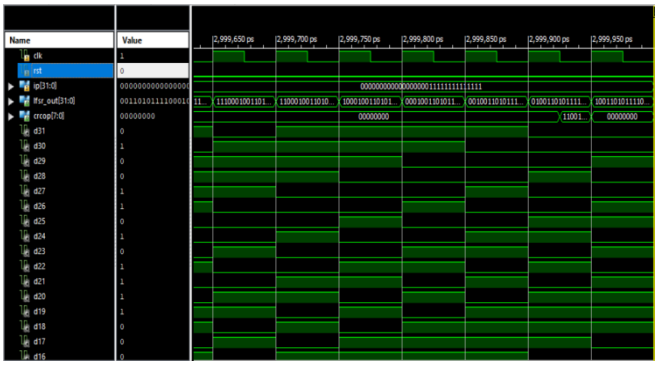

Figure 9: Simulation Result for input 11111111111111

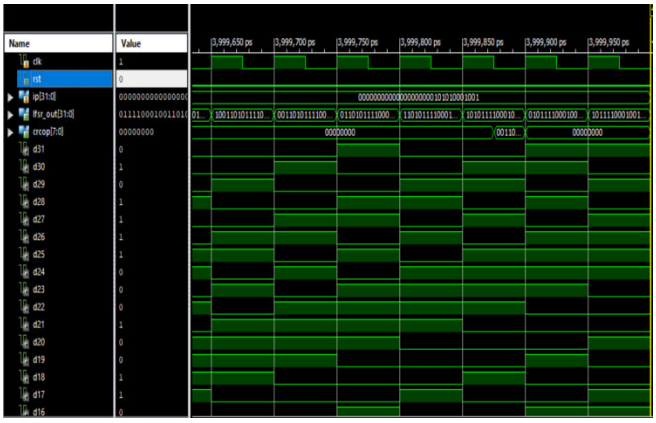

Figure 10:Simulation Result for input 101010001001

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The Synthesis results of the proposed design for some inputs has been shown in the below figures. Synthesis results provides the equivalent hardware architecture functionalities of the design about the number of gates used and timing analysis as shown in the below figure

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 2.476ns (Maximum Frequency: 403.918MHz)
   Minimum input arrival time before clock: 3.048ns
   Maximum output required time after clock: 2.055ns
   Maximum combinational path delay: 2.627ns
```

Figure 11: Timing Summary

```
Device utilization summary:
---------------------------

Selected Device : xa7a100tcsg324-2i


Slice Logic Utilization:
 Number of Slice Registers:                44  out of  126800     0%
 Number of Slice LUTs:                     40  out of  63400      0%
    Number used as Logic:                  40  out of  63400      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:       62
   Number with an unused Flip Flop:        18  out of     62     29%
   Number with an unused LUT:              22  out of     62     35%
   Number of fully used LUT-FF pairs:      22  out of     62     35%
   Number of unique control sets:           2

IO Utilization:
 Number of IOs:                            74
 Number of bonded IOBs:                    74  out of    210     35%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                  1  out of     32      3%
```

Figure 12: Device Utilization Summary

The proposed design consumes less power than the existing designs and the power distribution analysis has been shown in the below figure 12. From the above Design Summary, the space consumption of the design is also better than the existing design. The design total power consumption is 80milliwatts which is very less when compared to the other designs. The actual power consumption of the existing designs is at the levels of twice the proposed design power consumption levels which is a very far level from our design power consumption. So, the design proposed is the efficient design than the existing designs. The power analysis of the design can be obtained from the Xilinx power design tools which gives the total power consumption summary as shown in the below figure.

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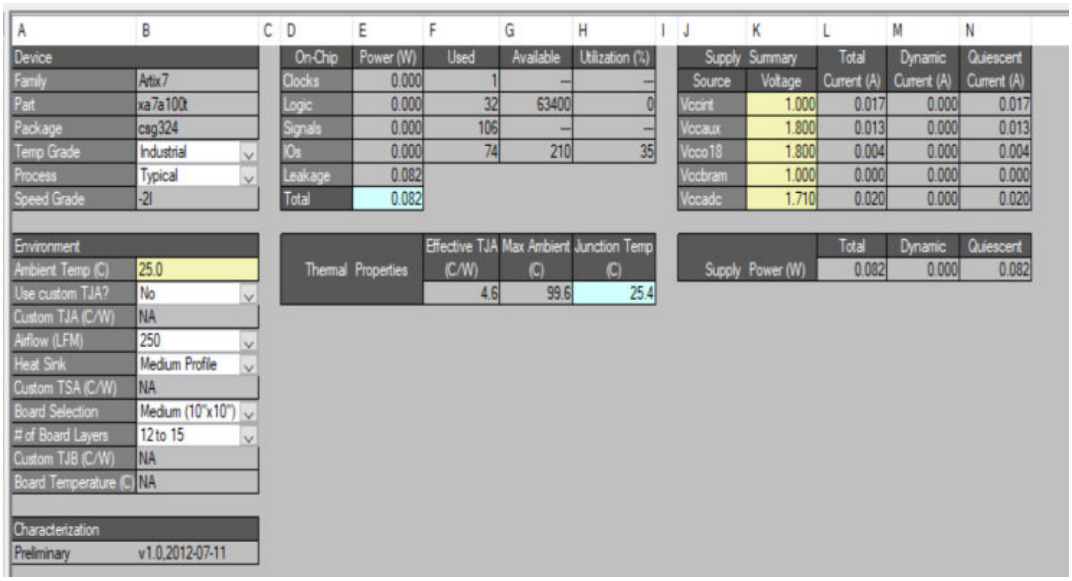

Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Artix7	Clocks	0.000	1	--	--
Part	xa7a100t	Logic	0.000	32	63400	0
Package	csg324	Signals	0.000	106	--	--
Temp Grade	Industrial	IOs	0.000	74	210	35
Process	Typical	Leakage	0.082			
Speed Grade	-2I	Total	0.082			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco18	1.800	0.004	0.000	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	99.6	25.4

	Total	Dynamic	Quiescent
Supply Power (W)	0.082	0.000	0.082

Characterization	
Preliminary	v1.0,2012-07-11

Figure 13: Power Distribution Analysis

VIII. FUTURE SCOPE

The development of designs in VLSI technology has been advancing to higher levels in these days and every organization shifts its works towards less power consumption circuits. This design methodology can be used in BCH encoders, CRC 's and some other electronics. Future work will address efficient design of long lfsr's with less complexity.

IX. CONCLUSION

The proposed design effectively shifts the complexity to the transformation matrix multiplication, which is only active in the last clock cycle. As a result, the proposed design achieves substantial reduction on the power consumption without increasing the CPD or total gate count compared to other transformed designs. In addition, a simplified method for computing the CPD of systems adopting SS is developed to better evaluate the complexity of matrix multiplications with CPD constraints.

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