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Review Paper on Distributed Arithmetic-Based Narrow Band Adaptive Filter

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ABSTRACT: Adaptive filters have proven to be an instrumental system component in the modern signal processing applications. Innumerable systems that we presently depend on in our daily life would not exist without the use of adaptive filters. There are two conflicting algorithms that are commonly used for implementation of adaptive filters; namely the narrow band based on multi rate approach. In addition, a computationally efficient distributed arithmetic (DA) approach may be used to implement the narrow band algorithm which may further reduce computational complexity. DA scheme employs bit-serial operations and look-up tables (LUTs) sharing and weight increment terms of multi-rate approach to implement high throughput filters. Therefore, a shared-LUT design is proposed to realize the DA computation. Instead of using separate registers to store the possible results of partial inner products for DA processing of different bit positions, registers are shared by the DA units for bit slices of different weightage.

KEYWORDS: - Finite Impulse Response (FIR), Look Up Table (LUT), Adaptive Filter, Narrow Band Filter

I. INTRODUCTION

The performance of digital signal processing and communication systems is generally limited by the precision of the digital input signal which is achieved at the interface between analog and digital information. Sigma-Delta modulation based analog-to digital (A/D) conversion technology is a cost effective alternative for high resolution converters which can be ultimately integrated on digital signal processor ICs. The sigma-delta modulator was first introduced in 1962; but it gained the importance in recent times after the development in digital VLSI technologies. The sigma delta A/D converters are based on digital filtering techniques; almost 90% of the die is implemented in digital circuitry which enhances the prospect of compatibility [1-3].

Conventional converters are often difficult to implement in fine line very large scale integration (VLSI) technology. By keeping these things in mind the people are going for over sampling converters, these converters make extensive use of digital signal processing. The main advantages of the sigma delta A/D converters are mentioned below.

- Higher reliability.
- Increased functionality.
- Reduced chip cost.

Those characteristics are commonly required in the digital signal processing environment of today. Consequently, the development of digital signal processing technology in general has been an important force in the development of high precision A/D converters which can be integrated on the same die as the digital signal processor itself. Conventional high-resolution A/D converters, such as successive approximation and flash type inverters, operating at the Nyquist rate (sampling frequency approximately equal to twice the maximum frequency in the input signal); often do not make use of exceptionally high speeds achieved with a scaled VLSI technology. These Nyquist samplers require a complicated analog low pass filter (often called an anti-aliasing filter) to limit the maximum frequency input to the A/D, and sample-and hold circuitry. The high resolution can be achieved by the decimation process. Moreover, since precise component matching or laser trimming is not needed for the high-resolution sigma delta A/D converters, they are very

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attractive for the implementation of complex monolithic Systems that must incorporate both digital and analog functions [4].

II. LITERATURE REVIEW

Basant Kumar Mohanty et al., in this paper, we break down the substance of query tables (LUTs) of circulated math (DA)- based square slightest mean square (BLMS) versatile channel (ADF) and in light of that we propose intra-emphasis LUT sharing to decrease its equipment assets, vitality utilization, and emphasis period. The proposed LUT streamlining plan offers a sparing of 60% LUT content for square size 8 and still higher putting something aside for bigger square sizes over the ordinary outline approach. We too introduce here the outline of an enroll based LUT grid for maximal sharing of LUT substance and full-parallel LUT-refresh task. In light of the proposed configuration approach, we have determined a DA-based design for the BLMS ADF, which is versatile for bigger piece sizes and also higher channel lengths. We find that the equipment many-sided quality of the proposed structure increments not exactly proportionately with input piece measure and channel length.

Azadeh Safari et al., discrete wavelet change (DWT) has demonstrated awesome execution in computerized picture pressure and denoising applications. It is the change utilized for source encoding as a part of JPEG2000 still picture pressure standard and FBI wavelet scalar quantization. DWT is fit for quick picture pressure at less region and low power utilization. This paper displays 4-tap orthogonal DWT in view of the buildup number framework. Equipment unpredictability lessening and configuration change are attained to by utilizing RNS for number-crunching operations and LUT offering between low pass and high pass channels. The RNS based DWT is reenacted and executed on the Xilinx FPGA to confirm the usefulness and effectiveness of the outline.

Yajun Zhou *et al.*, The present examination paper portrays a system assessing the Field Programmable Gate Array (FPGA) assets usage for execution of computerized channels with distinctive requests. For a low pass Butterworth channel, barring its request, rest of the configuration parameters were kept steady. Channel outlining was done utilizing the numerical figuring environment programming, MATLAB. Its exceptional office producing Hardware Description Languages (HDLs) for a computerized channel item was conveyed. Diverse Very High Speed Integrated Circuit HDL (VHDL) source codes were created and executed in Xilinx FPGA gadget Spartan-3E by expanding channel request, until the gadget usage surpasses the accessible assets. Thusly, a most extreme 18th request channel was implementable in FPGA. The computerized channel reaction was shown on an Oscilloscope by method for a microcontroller, Advance RISC Machine (ARM) gadget LPC2148. The simple to advanced and computerized to simple transformation over advanced channel information was performed in a solitary ARM chip.

V. Sudhakar et al., this paper displays completely parallel and completely serial architectures for Band pass channel. The exhibitions of completely parallel and completely serial architectures are investigated for distinctive quantized adaptations of representation. Channels produced utilizing 8 bit settled point execution requires littler zone utilization when contrasted with 16 bit altered point usage at the expense of imprecision. The proposed executions are orchestrated with Xilinx ISE 13.2 rendition. Group of gadget was Spartan 3E and target gadget was xa3s250e-4vqgl00. The key execution measurements, to be specific number of Slices, Slice Flip Flops, LUTs, Maximum recurrence are analyzed.

Animesh Panda et al., a channel may be obliged to have a given recurrence reaction, or a particular reaction to a motivation, step, or incline, or recreate a simple framework. Contingent upon the reaction of the framework, computerized channels can be ordered into Finite Impulse Response (FIR) channels & Infinite Impulse Response (IIR) channels. FIR Filters can be composed utilizing recurrence examining or windowing routines. Yet these strategies have an issue in exact control of the basic frequencies. In the ideal outline system, the weighted estimate lapse between the real recurrence reaction and the sought channel reaction is spread over the pass-band and the stop-band and the greatest blunder is minimized, bringing about the pass-band and the stop-band having swells. The crest mistake can be processed utilizing a PC supported iterative methodology, known as the Remez Exchange Algorithm.

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III. DISTRIBUTIVE ARITHMETIC TECHNIQUE

Distributed Arithmetic (DA) is a widely-used technique for implementing sum-of-products computations without the use of multipliers. Designers frequently use DA to build efficient Multiply-Accumulate Circuitry (MAC) for filters and other DSP applications. The main advantage of DA is its high computational efficiency. DA distributes multiply and accumulates operations across shifters; lookup tables (LUTs) and adders in such a way that conventional multipliers are not required.

Distributed arithmetic is an important algorithm for DSP applications. It is based on a bit level rearrangement of the multiply and accumulate operation to replace it with set of addition and shifting operations. The basic operations required are a sequence of table lookups, additions, subtractions and shifts of the input data sequence. The Look Up Table (LUT) stores all possible partial products over the filter coefficient space.

Assuming coefficients c[n] is known constants, and then y[n] can be rewritten as follows:

$$y[n] = \Sigma\, c[n] \cdot x[n] \quad n = 0, 1, \ldots, N\text{-}1 \tag{1}$$

Variable x[n] can be represented by:

$$x[n] = \Sigma\, x_b\,[n] \cdot 2^b \qquad b = 0, 1, \ldots, B\text{-}1$$
$$x_b[n] \in [0, 1] \tag{2}$$

Where x_b [n] is the b^{th} bit of x[n] and B is the input width. Finally, the inner product can be rewritten as follows:

$$y = \Sigma\, c[n]\, \Sigma\, x_b\,[k] \cdot 2^b \tag{3}$$

$$\begin{aligned} &= c[0]\,(x_{B-1}\,[0]2^{B-1} + x_{B-2}\,[0]\,2^{B-2} + \ldots + x_0\,[0]\,2^0) \\ &+ c[1]\,(x_{B-1}\,[1]\,2^{B-1} + x\, x_{B-2}\,[1]\,2^{B-2} + \ldots + x_0\,[1]\,2^0) + \ldots \\ &+ c[N\text{-}1]\,(x_{B-1}[N\text{-}1]\,2^{B-1} + x_{B-2}\,[0]\,2^{B-2} + \ldots + x_0\,[N\text{-}1]\,2^0) \end{aligned} \tag{4}$$

$$\begin{aligned} &= (c[0]\,x_{B-1}\,[0] + c[1]\,x_{B-1} + \ldots + c[N\text{-}1]\,x_{B-1}[N\text{-}1])\,2^{B-1} + (c[0]\,x_{B-2}[0] \\ &+ c[1]\,x_{B-2}[1] + \ldots + c[N\text{-}1]\,x_{B-2}[N\text{-}1])\,2^{B-2} + \ldots + (c[0]\,x_0[0] + \\ &c[1]\,x_0\,[1] + \ldots + c[N\text{-}1]\,x_0[N\text{-}1])\,2^0 \end{aligned} \tag{5}$$

$$= \Sigma\; 2^b\, \Sigma\, c[n] \cdot x_b\,[k]$$

Where n=0, 1… N-1 and b=0, 1… B-1

The coefficients in most of DSP applications for the multiply accumulate operation are constants.

IV. MULTIRATE APPROACH

The process of converting a signal from a given rate to a different rate is called sampling rate conversion. The systems which employ multiple sampling rates in the processing of digital signal are called multi-rate signal processing [5].

Decimation is the processes of lowering the word rate of a digitally encoded signal, which is sampled at high frequencies much above the nyquist rate. It is usually carried out to increase the resolution of an oversampled signal and to remove the out-of-band noise. In a sigma-delta ADC, oversampling the analog input signal by the modulator alone does not lower the quantization noise; the ADC should employ an averaging filter, which works as a decimator to remove the noise and to achieve higher resolutions. A basic block diagrammatic representation of the decimator is shown in Figure 1.The decimator is a combination of a low pass filter and a down sampler. In Figure 1 the transfer

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function, H(z) is representative of performing both the operations. The output word rate of the decimator is down sampled by the factor M, where M is the oversampling ratio [6]. The function of low pass filtering and down sampling can be carried out using an averaging circuit. The transfer function of the averaging circuit is given by equation (1.1). It establishes a relation between the input and output functions (1.1)

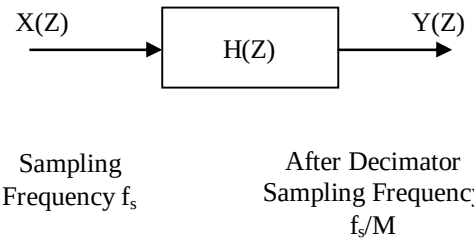

Figure 1: Block Diagram of Decimator

$$H(Z) = \frac{X(Z)}{Y(Z)} = \frac{1}{M}\sum_{x=0}^{M-1} Z^{-x} \qquad (6)$$

"Up sampling" is the process of inserting zero-valued samples between original samples to increase the sampling rate. (This is called "zero-stuffing".) Up sampling adds to the original signal undesired spectral images which are centered on multiples [7] of the original sampling rate.
"Interpolation", in the DSP sense, is the process of up-sampling followed by filtering. (The filtering removes the undesired spectral images.) As a linear process, the DSP sense of interpolation is somewhat different from the "math" sense of interpolation, but the result is conceptually similar: to create "in-between" samples from the original samples.

V. PROPOSED METHODOLOGY

It depends on the filter coefficients required to achieve the desired frequency response of the filter. The narrowband filter may be implemented directly or using the multi-rate method. Here we have estimated the required filter coefficients for both these methods to find the complexity of the narrow band filter.

- Specification of the narrowband filter:

Sampling frequency, $F_s = 250Hz$

Pass band ripple, $\delta_p = 0.08dB$

Stop band ripple, $\delta_s = 42dB$

Pass band frequency, $f_p = .825Hz$

Stop band frequency, $f_s = 4.15Hz$

- Direct Approach

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Block diagram for implementation of narrow band filter is shown in Figure 2.

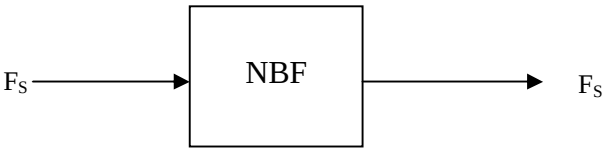

Figure 2: General diagram of narrow band filter

Transition width,

$$\Delta f\,(normalized)\ freq. = {f_s - f_p}/{F_S} \qquad (7)$$

Filter order N Filter order by Kaiser Formulation

$$N = -20\log\sqrt{\frac{\delta_s\delta_p - 13}{14.6\Delta f}} \qquad (8)$$

Filter order

$$N = 150$$

- **Multi-rate Approach**

The block diagram of multi-rate approach for implementation of narrowband filter is shown in Figure 3.

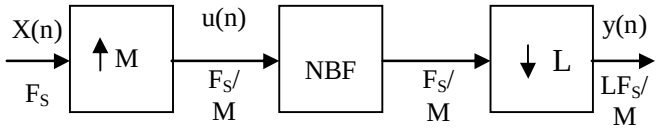

Figure 3: Diagram of the multistage for designing level

Suppose the sampling frequency of the narrowband filter is 125 Hz.

Down sampling factor M=2, Calculation of filter order of the decimator:

Specification of decimator:

$$\Delta f\,(normalized) = {(f_{s1} - f_p)}/{F_s}$$

$$f_{s1} = F_s - {F_s}/{2M}$$

$$\Delta f = .2467\,Hz$$

$$FilterOrder N1 = 9$$

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VI. CONCLUSION

The narrowband filter is realized in FIR filter. Based on the direct approach, the filter requires 150 filter coefficients to meet the desired frequency response. To implement such a large order FIR filter in hardware involves large resources and sometime difficult to implement in resource constrained application. Keeping this in view, we have used Multirate approach to design the narrowband filter. We have used down sampling factor 2 and 4 for this purpose and found that, down sampling factor 4 requires significantly less filter constants than 2. To implement the narrowband filter, we therefore chosen down sampling factor 4 and designed the decimator, interpolator and narrowband filter.

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