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Analysis of Various Low-Voltage High Impedance Gate Driven CMOS Current Mirrors

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ABSTRACT: Current mirror (CM) circuit has served as the basic building block in analog circuit design since the introduction of integrated circuit. In this paper, various low-voltage, high impedance gate-driven current mirror circuits have been discussed. The circuits are implemented in GDPK 180nm CMOS process and the simulation is done using Cadence Spectre. Various parameters of the circuits such as current linearity, output impedance, dc transmission error, power consumption, leakage power etc. have been analyzed and discussed. Analysis of these circuits shows that different circuits can be used in different applications depending upon their characteristics. The total power consumption is reduced by 110% in the improved gate-driven current mirror (CM) design and hence can be used for power efficient applications where as the cascode configuration is best suited for high current swing applications due to its high current linearity range.

KEYWORDS: Low-Voltage, Super Wilson, High Output Impedance, Current Mirror, Gate-Driven, Cascode.

I. INTRODUCTION

In the early 1980s many experts predicted the demise of analog circuits. Many functions that had been traditionally realized in analog form were now easily implemented in the digital domain, suggesting that with enough capability in IC fabrication, all processing of signals would eventually occur digitally. But still analog designers are of great demand today. This is because there are many areas where it is not feasible or even impossible to replace analog blocks with their digital counterparts regardless of the technology advancements. Digitization often requires analog blocks before digitizing. A major component in these analog circuits is the current mirror CM), especially a high impedance CM in the case of biomedical applications.

With the advancements in the CMOS technologies, it is possible to integrate baseband signal processing units, sensors and radio-frequency (RF) circuits on a single chip. Ultra-low power consumption and low voltage supply of 1V or less are an important aspect to ensure that the batteries can work for a long duration. The new deep sub-micron CMOS technologies are very apt to fulfil this need, since deep sub-micron CMOS transistors can operate in weak inversion region (up to the GHz region) with reasonable gain, and have low threshold voltage which makes it feasible to design analog circuits that can operate at low voltages (around 1V). However, the scaling of the supply voltage along with the low output resistance of transistors in these deep sub-micron CMOS processes make it very difficult to implement CM and current sources or sinks that give very-high output impedance over a large output voltage range [1]. Various current mirror designs are hence analysed for different parameters and their suitable applications are mentioned.

The performance of the gate-driven current mirrors and their basic operation is described in section II. The simulation results are shown in section III and the conclusions are drawn in section IV.

II. LITERATURE REVIEW

Several current mirror designs have been proposed in the past. One of the very fundamental designs of current mirror is a high-swing super-Wilson (HSSWCM) [2], which offers high output impedance using negative feedback and

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shown in Fig. 1. The transistors M1 and M4 forms a CM which samples the output current I_{out} and makes its comparison with the input current I_{in}. The gate voltage of the M5 is adjusted by the difference between I_{out} and I_{in} which in turn assures that the output current I_{out} is equal with input current I_{in}.

The output impedance is directly proportional to the gain of the loop which is given as the combination of current source load and Common Source amplifiers M1. The output impedance r_{out} of the HSSWCM can be approximated as:

$$r_{out} = g_{m1}r_{01}r_{05} \quad (1)$$

Where g_{m1} and r_{01} are respectively the transconductance and the output resistance of transistors M1 and r05 is the output resistance of transistors M5. The low voltage current mirror [3] circuit shown in Fig. 2 is the modified super–Wilson structure. In this structure, a diode connected transistor is attached at the input current arm in the cascoded configuration, such that the gain is improved to $g_m r_{out}$. In both cases the auxiliary current source is used to make the drain symmetry for the CM transistor pair.

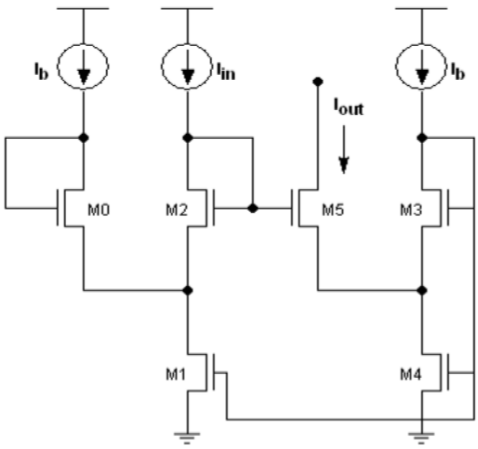

Fig. 1 HSSWCM Circuit

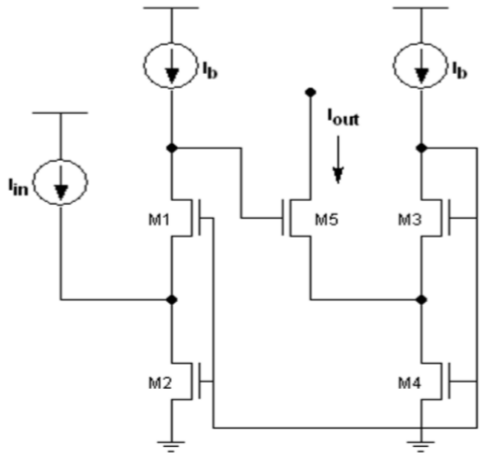

Fig. 2 LVSWCM Circuit

III. CIRCUIT OPERATION

The above circuit acts as a basis for a new circuit low voltage high swing Super Wilson Current Mirror circuit (LVHSSWCM) [4]. In this circuit, no auxiliary current source is required to achieve the drain symmetry for the transistors M2 and M4. Rather, the auxiliary current source is replaced by the diode-connected PMOS to achieve the drain symmetry. The M2 and M4 transistors formed as part of the CM have a purpose of giving high output impedance.M1, which is a diode connected transistor, is modified as a cascoded one. The transistors M2 and M4 samples the output current I_{out} which is then compared with the input current I_{in} which in turn changes the conduction of the transistor M5 and finally, the output current I_{out} is made equal to the input current I_{in}. M6 and M7, which are also the diode connected transistors, acts as an active load and increase the output impedance as well as the output current. The increased output impedance can be expressed as:

$$r_{out} \approx (g_{m1}||g_{m6})g_{m2}r_{01}r_{02}r_{05} \quad (2)$$

where g_{m1}, g_{m2}, g_{m6} and g_{o1}, g_{o2}, g_{o5} are respectively the transconductance of the transistors M1, M2, and M6.

The performance of the earlier proposed circuits is good in the input current range of 30 to 40μA. However, at lower input currents, a negative leakage current exists in these circuits due to which these circuits fail to produce the exact mirroring. As a diode connected PMOS is present in LVHSWCM circuit, this performs well in the lower input range from 5μA to 40μA range as well and provides very less transfer error compared to the earlier mentioned structures..

But the circuit has a major drawback. In the PMOS the source and gate are shorted and as a result V_{gs} is always zero.

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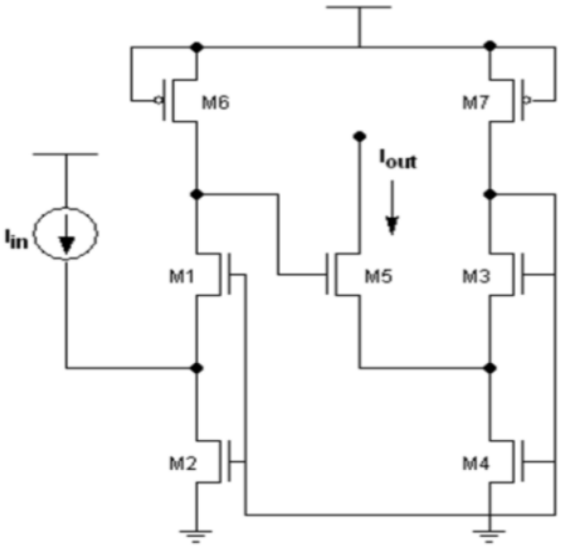

Fig. 3 LVHSWCM circuit

For the PMOS to act as constant current source, it should be in saturation. i.e.

$V_{gs} - V_t \geq V_{ds,sat}$ (3)

In this circuit Vgs is zero and hence the equation reduces to

$-V_t \geq V_{ds,sat}$ (4)

This limits the value of overdrive voltage, V_{ov} depending on the value of V_t to make the transistor operate in the saturation region.

In order to overcome this limitation, LVHSWCM circuit is modified so that the circuit can be designed for various overdrive voltages [5]. The modification is made by removing the short circuit between gate and source of the PMOS transistors and the transistors are biased by applying a biasing voltage at the gate of the PMOS transistors in Fig 4. This helps in designing the circuit for different overdrive voltages. The new current mirror circuit has a biasing voltage V_{b1} at the gates of transistors M6 and M7. This voltage is selected such that the transistors obey the condition for saturation, i.e.

$V_{gs} - V_t \geq V_{ds,sat}$ (5)

Where, $V_{gs} = V_g - V_s = V_{b1} - V_{dd}$ (6)

i.e. the biasing voltage is greater than supply voltage plus minimum overdrive or minimum saturation voltage.

Another type of low-voltage, high-swing current mirror is cascode current mirror [6]. The circuit is shown in Fig. 5. Cascode current mirror (CCM) is used to obtain better input/output characteristics. It also helps to achieve high output impedance. In this configuration, the output resistance of the circuit is increased by a factor given by $g_m r_0$, (where gm is transconductance and r0 is output resistance of the MOSFET) [7]. Thus CCM is highly suitable for applications such as high performance second generation current conveyers, variable gain low noise amplifier, voltage to current converter, telescopic opamps, etc, as compared to simple current mirror. [8]. However, CCM has reduced voltage swing. Let, V_{out} be the minimum output voltage needed to maintain the MOSFET's of the CM in saturation region be. Lower the value of V_{out}, higher is the voltage swing of the mirror.

The output impedance of this circuit is given by:

$r_{out} = r_{01} + r_{02} + g_{m2} r_{01} r_{02}$ (7)

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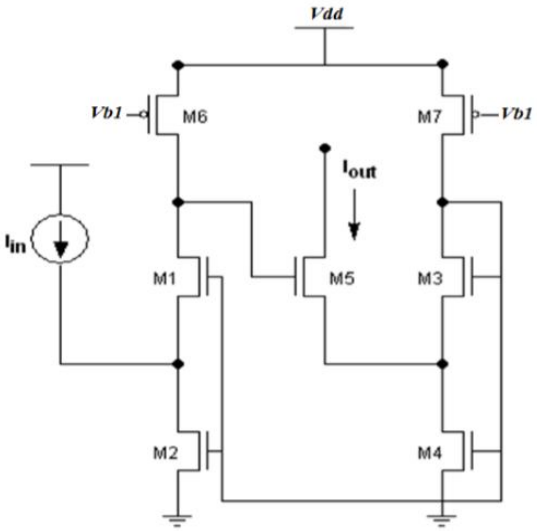

Fig. 4 Improved LVHSSWCM Mirror

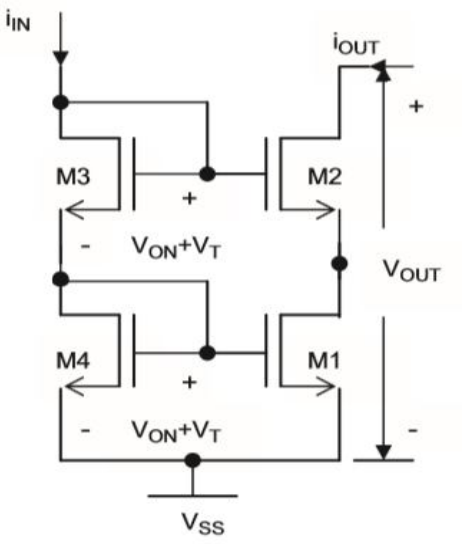

Fig. 5 Gate Driven CCM circuit

IV. SIMULATION RESULTS

The circuits shown in this paper are simulated using Cadence spectre of 180nm CMOS technology. The design specifications are shown in Table I. All the gate driven current mirrors operates at 1.8V.

The output characteristics i.e., output current vs. output voltage is shown in Fig. 6. It can be seen that the circuit starts conducting at a value quite below the threshold value thus reducing the input/output voltage drop.

The Design specifications for LVHSSWCM and improved LVHSSWCM are mentioned in Table I and Table II respectively.

Cascode current mirror has all NMOS of dimension W/L=1µ/180n.

Table I. Design Specifications of LVHSSWCM

V_{DD}= 1.8V, V_{SS}=0V	
Transistor	**Aspect Ratio, W(µm)/L(µm)**
PMOS (M6/7)	1/0.18
NMOS (M1-M5)	0.4/0.18

Table II. Design Specifications of Improved LVHSSWCM

V_{DD}=1.8V, V_{SS}=0V	
Transistor	**Aspect Ratio, W(nm)/L(nm)**
PMOS (M6/7) & NMOS (M1/3/5)	405/360
NMOS (M2/M4)	570/360

Fig. 6 shows the output characteristics of the circuits. LVHSSWCM and improved LVHSSWCM have almost same output characteristics where the circuit starts conducting when the input voltage becomes greater than the threshold voltage. Whereas CCM has better response as there is no threshold lag for this circuit and the circuits starts conducting as soon as the input is applied. This is attributed due to the cascode topology of the circuit.

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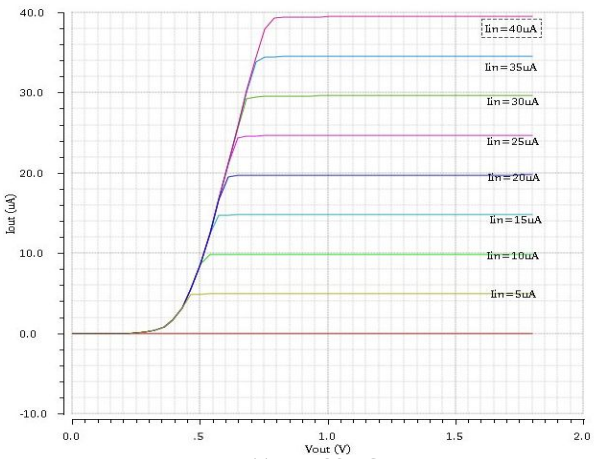
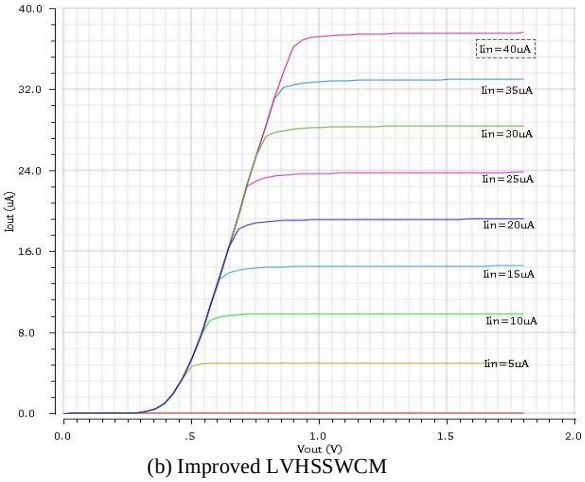
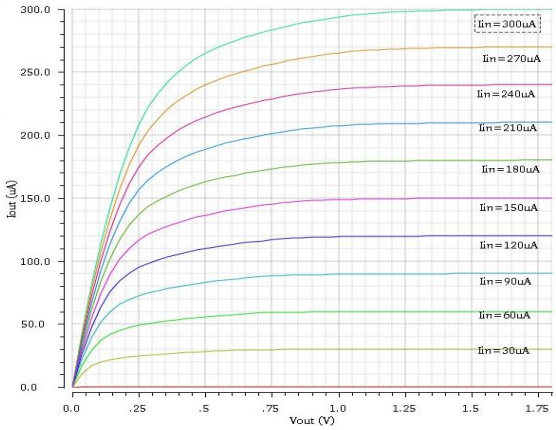


(a) LVHSSWCM

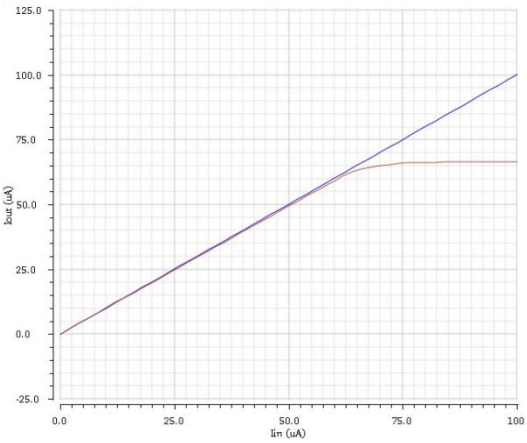


(b) Improved LVHSSWCM

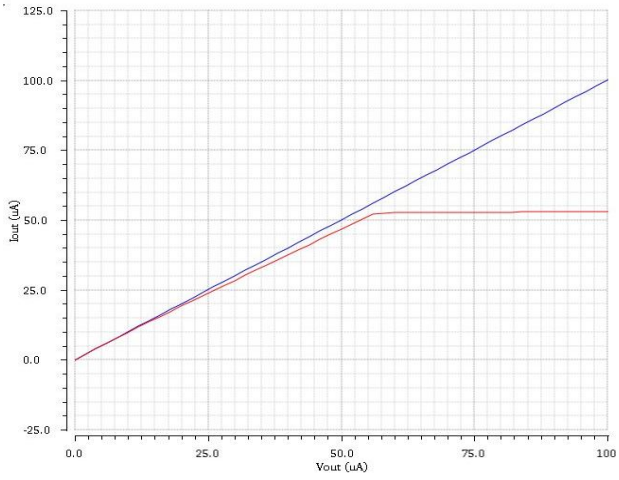


(c) Cascode Current Mirror

Fig. 6 Output current vs. Output Voltage characteristics



(a) LVHSSWCM



(b) Improved LVHSSWCM

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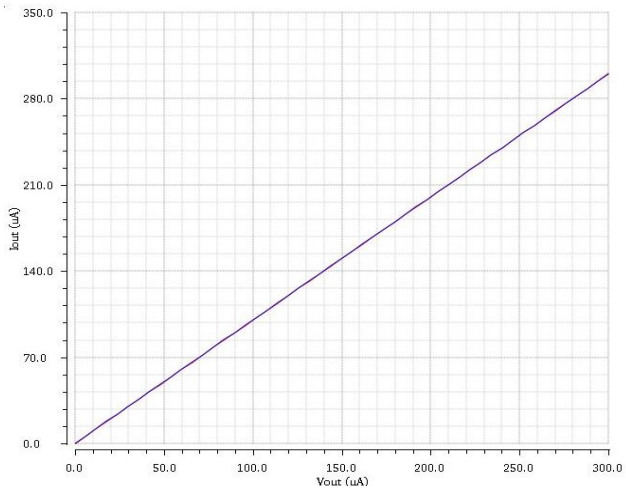


(c) Cascode current Mirror

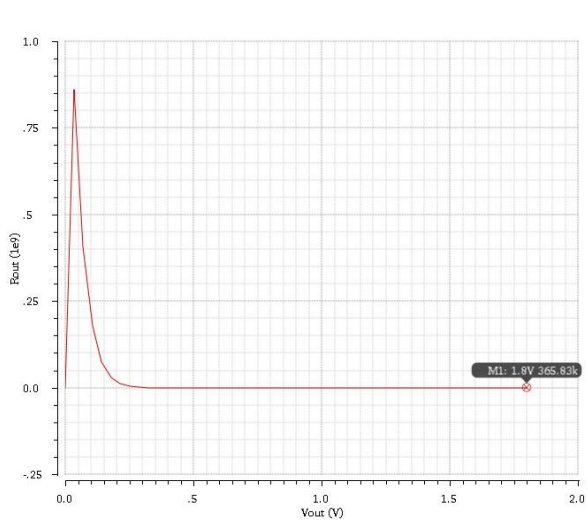
Fig. 7 Iout vs. Iin characteristics

Fig. 7 shows that the linearity of LVHSSWCM is upto 60µA, Improved LVHSSWCM is upto 55µA where as it is upto 100µA for the cascode current mirror.

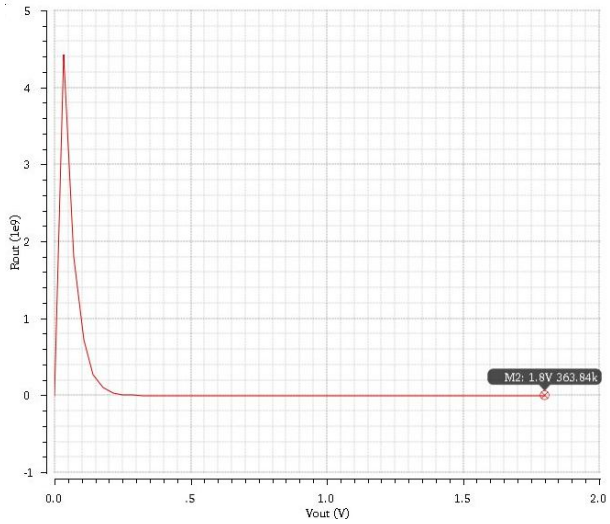
The output resistance graphs for 5µA input current are shown in Fig. 8. It can be seen that the output resistance shoots abruptly to a very high value at very lower voltages for Fig. 8 a) and b) as the circuits are not conducting at this region but beyond this region the output resistance is constant at a considerably high value. In cascode CM, output resistance increases with increase in voltage and attains maximum value at 1.8V.

Fig. 9 shows the total power consumption of the circuit at 5µA input current. The improved LVHSSWCM has less power consumption (in µW) than LVHSSWCM (in mW) where as for cascode CM, power consumption is increasing with the increase in the output voltage.

Fig 10 shows that the leakage power is slightly reduced in improved LVHSSWCM than that of LVHSSWCM. The improved LVHSSWCM has the lowest leakage power consumption which is nearly same as cascode CM and followed by LVHSSWCM. Thus improved LVHSSWCM can be used in power efficient applications.



(a) LVHSSWCM



(b) Improved LVHSSWCM

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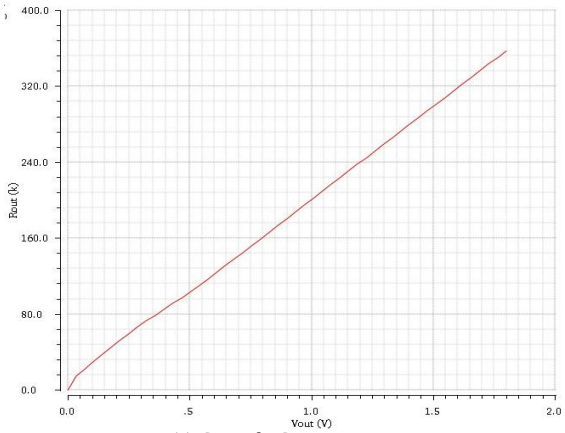
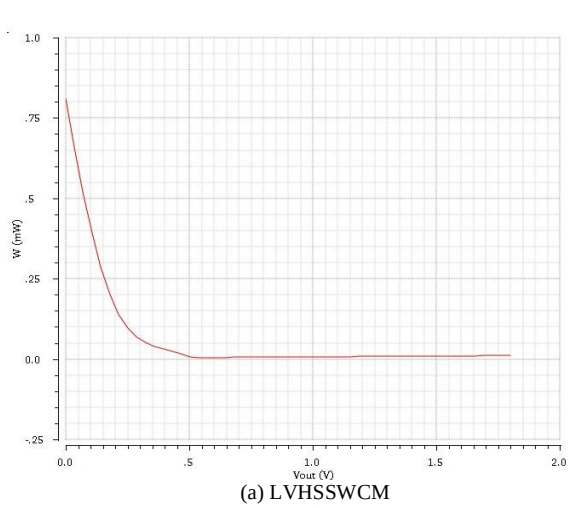
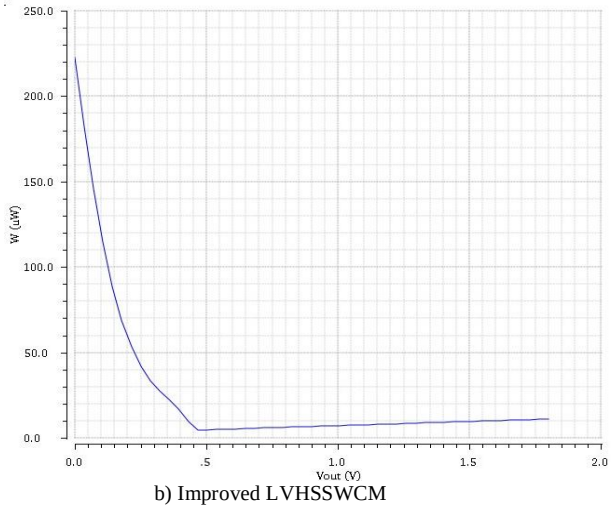


(c) Cascode Current Mirror

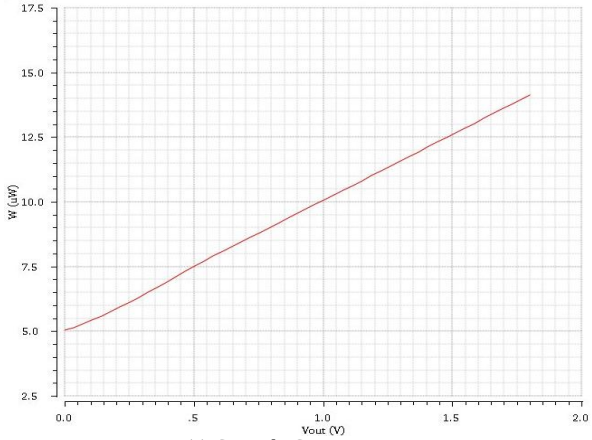
Fig. 8 Output resistance vs. Output Voltage at 5µA Input Current



(a) LVHSSWCM



b) Improved LVHSSWCM



(c) Cascode Current Mirror

Fig. 9 Power Analysis at 5uA Input Current

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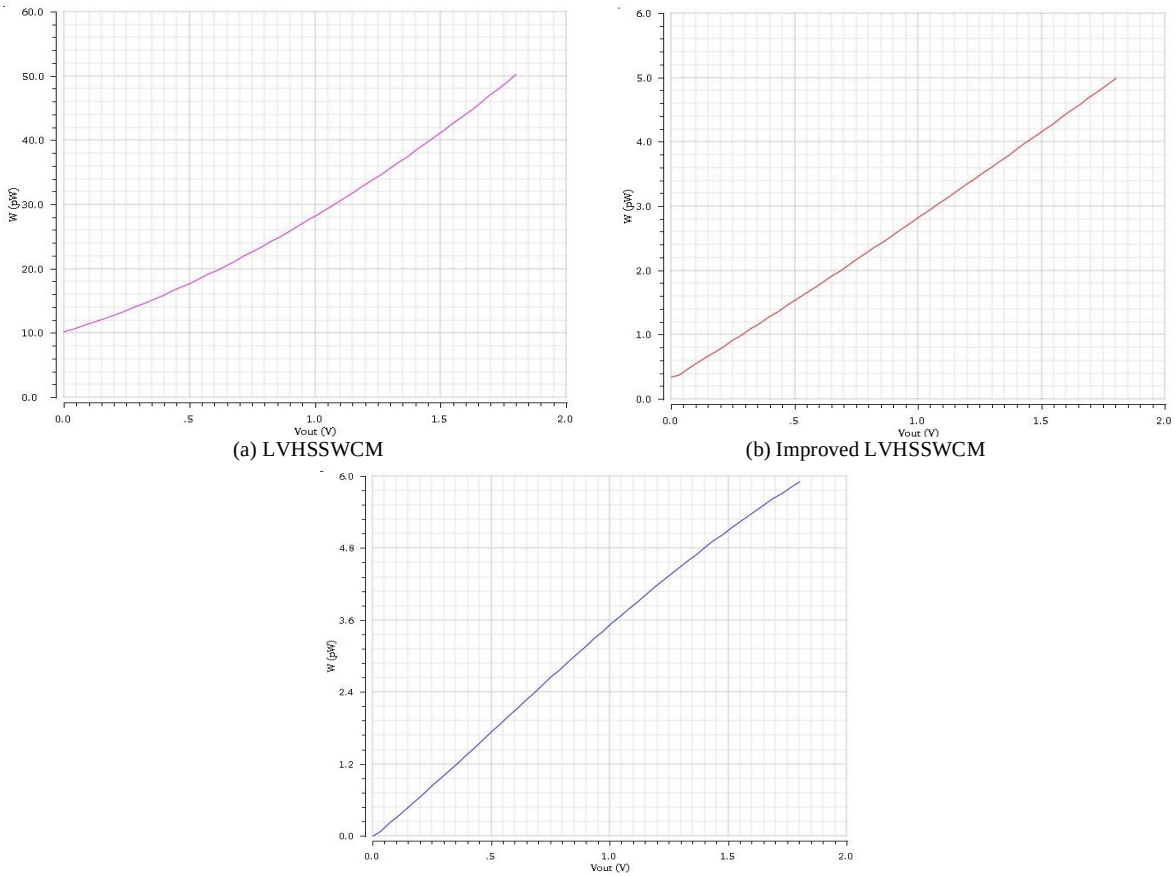

(a) LVHSSWCM (b) Improved LVHSSWCM

(c) Cascode Current Mirror

Fig. 10 Leakage Power Analysis

V. CONCLUSION

The simulation results show that the cascode CM can be used in low supply voltage applications as it reduces the limitation caused by the threshold voltage. Also cascode CM has the highest current linearity (100uA) and can be used in high current swing applications. Improved LVHSSWCM dissipates around 110% less power than LVHSSWCM. Also the leakage power consumption is also reduced by 9 times in Improved LVHSSWCM from LVHSSWCM. Thus the Improved LVHSSWCM is suitable for power efficient or low power applications.

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