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Design and Implementation of Power Efficient Linear Feedback Shift Register for BIST using Verilog

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ABSTRACT: Testing is an essential part in VLSI from designers to the users. More importance is given in achieving low power designs in the design level but it is equally important to achieve low power test techniques since more power will be consumed during testing than in normal functional mode. This paper proposes a low power test pattern generator based on 8 bit linear feedback shift register (LFSR) which consumes 65.62% less power and 70.08% less area as compared to bitswap LFSR. This reduction in power and area is observed solely for LFSR, it might vary when observed with respect to Circuit Under Test (CUT).

KEYWORDS: LBIST (LOGIC Built In Self Test), LFSR, CUT, ATPG (automatic test pattern generator), ATE (Automatic Test Equipment)

I. INTRODUCTION

Production of low power design is increasing since in many application areas such as communication and computing power dissipation is one of the major objectives in design. Not only in design, power optimisation is becoming an important factor in testing as well since, during testing the power consumption is more than the functional mode of operation. Since test throughput and manufacturing yield are often affected by test power, dedicated test methodologies have emerged over the past decade. Based on the switching activity, there can be tremendous variation in consumption of Dynamic power. This leads to significant variation in functional power and testing power. Due to this, there exists a gap between functional power and test power which might cause some serious problems during testing as per [1].

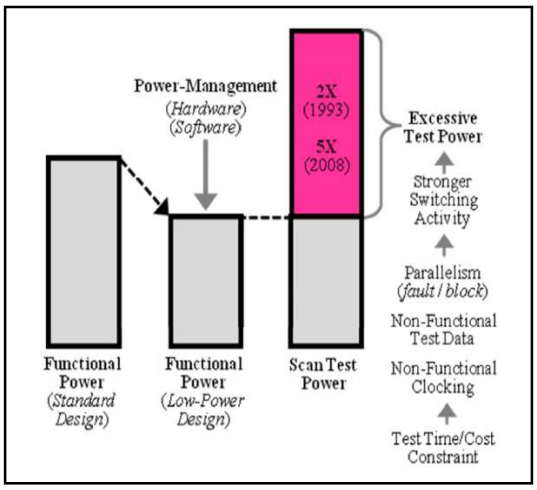

Figure 1: Functional Power and Test Power gap [1]

Consider a functional block implemented using standard design techniques and another functional block implemented by making use of low power design techniques. It is been observed that the latter one has better power management techniques and is found to be more efficient and consumes less functional power all because of the use of power management techniques. Though there is reduction in functional power, it is been observed that there is increase in the test power due to more switching activity and the increase is 2 times in 1993 and 5 times in 2008 as depicted in Figure 1. This makes it important to develop low power test techniques in order overcome this drawback and also improve the efficiency of testing.

Any VLSI system consists of logic block. The major working of any design solely depends on the logic. And as per the power consumption observed, it is very important to achieve low power technique for design for testability. This led to the development of Logic built-in self-test (BIST).

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II. LITERATURE SURVEY

According to Chethan J et.al [6], it was observed that various researchers have tried to optimize test pattern generation design, in order to reduce the power consumption by design under test while testing for stuck at faults. Sakthivel et.al, Pradhan, D.K et.al [2],[5] have presented Low Transition Galois Linear Feedback Shift Register(LT-GLFSR) made of modified GLFSR in order to reduce transitions in Circuit Under Test(CUT) when compared with standard LFSR and GLFSR. S. Kundu [4] have come up with a low power test pattern generator which combines gray counter and read only memory (ROM) in order to produce low power patterns for CUT which yields 52% reduction in dynamic power consumption. Sabir Hussain et.al [3] talks about bit swapping technique which is used for LFSR to be used in BIST, a low power technique and reduces transitions in CUT and 27.48% reduction in dynamic power consumption as opposed to standard LFSR. The simulation was performed using Cadence Electronic Design Automation (EDA) Tool in 180nm technology. Emina Milovanovic et.al [7] gives the explanation of standard LFSR generators Fibonacci and Galois. Implementation of LFSR based parallel test pattern generator having multiple outputs which are used as building block in BIST is discussed. Praveen Kasunde et.al [8] have proposed low power test pattern generator which has modified low power LFSR that reduces the power consumption during testing mode which is possible because of less number of switching activities. This is achieved by EXORing the sequence generated by LPLFSR with output of gray code generator as per [8].

Based on the knowledge of varieties of techniques available to design test pattern generator and achieving low power techniques for the same, Consider the explanation of basic LBIST and the blocks present in them. LBIST is a DFT technique where a portion of Design under Test (DUT) is used to test itself. One of the major objectives of LBIST is to achieve high fault coverage but the major issue is the power consumption during testing which exceeds the power rating of the chip or package. This increased power consumption can lead to heating of the chip, noise related failures.

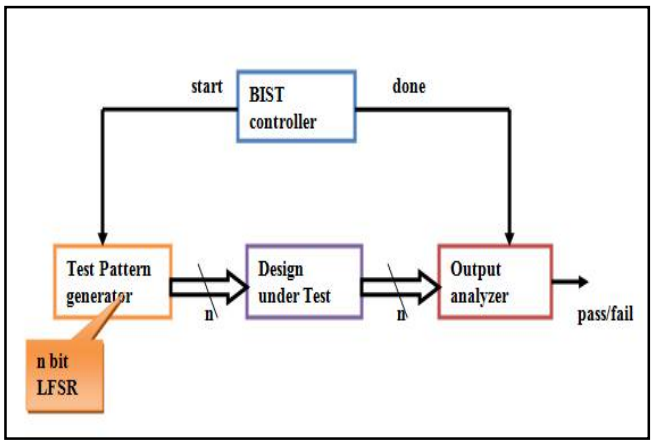

Figure 2 General block diagram of LBIST [10]

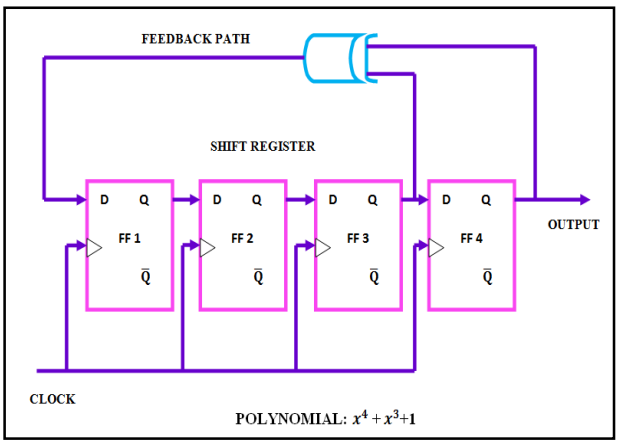

Figure 3: General block of a 4 bit LFSR [12]

Figure 2 shows the block diagram of a LBIST in which the BIST controller provides the data for the DUT as test patterns or externally applied ones based on the control signal applied to it. During the testing mode, the DUT will receive the data from the test pattern generator else it considers the externally applied data. The output of the DUT is applied to output response analyzer, which compares the output of the DUT called actual signature with what is known as golden signature. The signatures which are generated by them are basically the compact version of the output of DUT.

LBIST uses pseudo random patterns enabling it to generate patterns on the die, saving tester memory to a larger extent. At the same time it poses challenges to enable fail data correction for later debug as the LBIST test iterations are usually large. It operates by exercising the circuit logic and detects if the logic behaved as intended using on chip test generator and test response comparator.

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In LBIST architecture, LFSR is used to generate stimuli for CUT. LFSR is a clocked synchronous shift register augmented with clock signal as input to generate random test patterns at every clock cycles. The random patterns generated are used to detect the physical faults in the IC. The operation of the shift register is deterministic therefore the values generated by the shift registers are determined by its previous states. Seed is the value given to the LFSR initially.

The same is shown in Figure 3 which represents a four bit LFSR. It can be observed that, simple D flip flop has been used for shift register and modulo two adder implemented using XOR gates provides for the feedback network. The lines from which input of XOR gates are to be tapped will be determined by the polynomial equation.

Section III explains the proposed method, IV depicts of simulation results and comparisons of power and area readings, V provides the conclusion and future work, and finally information about the references used and biography.

III. PROPOSED ALGORITHM

A. *Design Considerations: Algorithm of state based LFSR*

The conventional LFSR would give only (2^n-1) states. Since some applications require all the states of the random pattern generator more importance is given to that. As per the design proposed in [8] all the 256 states can be achieved and considering that as reference LFSR named as bitswap. According to [8] the LFSR that is used would give low power when used along with BIST. The LP-LFSR block in [8] is considered as single tap LFSR for bitswap, Fibonacci LFSR for bitswap_f and Galois for bitswap_g. Considering the LFSR itself as a sole block and comparison is made with various different types of LFSR. The conventional Galois or Fibonacci LFSR is modified to produce all the 256 states, that is by using the basic polynomial equation for an 8 bit LFSR and making slight changes, this was possible to be achieved.

B. *Description of the state based LFSR-Proposed Algorithm:*

The traditional Fibonacci LFSR is considered, having reset signal in synchronous with clock. In the traditional Fibonacci LFSR, a condition is maintained to bypass the stuck at zero state. It is explained in the flowchart shown in Figure 5 as follows.

The state prior to zero state is found by running classical Fibonacci LFSR that is without any modification. This method ensures that all the 256 states are achieved without leading to stuck at 0 states. The same is explained in algorithm followed by Pseudo code, flowchart is depicted in Figure 5 and the state diagram is as shown in Figure 4. The same technique has been tried with Galois LFSR as well.

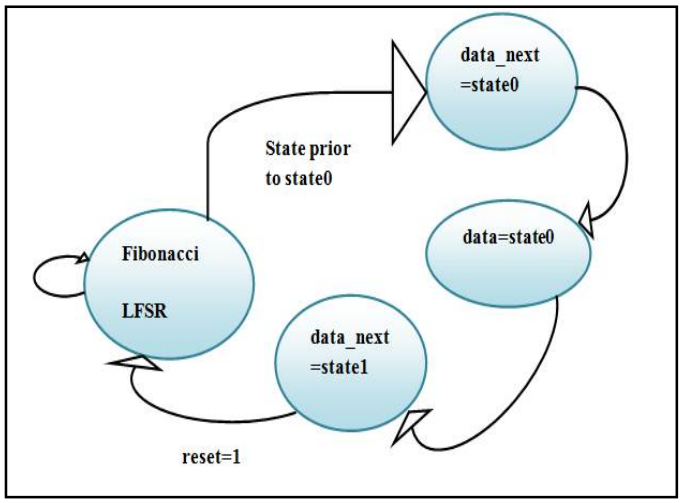

Figure 4: State diagram of State Based LFSR

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i. Declare the inputs for LFSR clock, reset and output data. Also declare an intermediate signal data_next. Both data and data_next are of 8 bit in size.
ii. Check if data is state prior to state 0. If so then assign next state as state 0. In a classical LFSR this state would be skipped.
iii. If result is false in step ii, then check if data is state 0 if so then assign data_next as state 1 else perform as per polynomial equation of Fibonacci LFSR.
iv. If positive edge of the clock and reset 0 has occurred and are synchronised, check if reset is zero then assign data to state 0 else assign data to data_next which is calculated from step ii and step iii.

The proposed algorithm is depicted in the state diagram as shown in Figure 4.

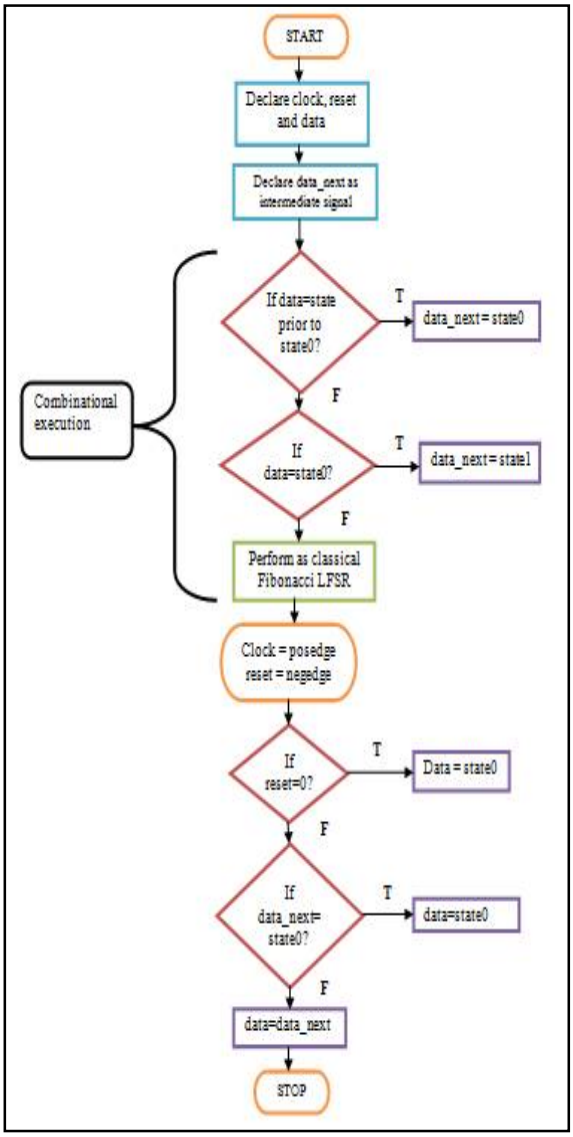

Figure 5: Flowchart of State based LFSR

Pseudo code for state based LFSR

```
always @*
begin
if(data==state prior to state0)
data_next= state0;
else if (data== state0)
data_next= state1;
else
perform  as Fibonacci LFSR

always @(posedge clk or negedge rst_n)
begin
if(!rst_n)
data <= state0;
else
begin
if(data_next== state0)
data<= state0;
else
data <= data_next;
end
end
```

Combinational part

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From Figure 4, if the reset is 0, then the output of LFSR is assigned to be state 0 that is the output is zero. According to the traditional LFSR if it enters state 0 then it will be stuck there. So next state is assigned to be state 1 that is the output is forced to 1. As long as the reset is zero, the LFSR output will be 0 and next state or output expected from LFSR will be 1. Once the reset is made high, it works as per the polynomial equation described for Fibonacci LFSR. The Fibonacci LFSR polynomial equation is designed in such a way that it skips state 0 which causes the LFSR to enter the stuck state. Therefore it is required to know the state prior to state 0 and forcefully assign it to some other state; the same is depicted in Figure 4.

IV. SIMULATION RESULTS

The proposed design is coded in Verilog, simulated using *ncsim* simulator from Cadence to check the functionality and synthesized by targeting to *slow_normal* standard cell technology library using RTL Complier from Cadence to generate the gate level net list. The RTL schematic obtained is depicted in figure 6. The simulation results obtained for the same is represented in figure 7 and 8 and the explanation of output for the stimulus is also provided.

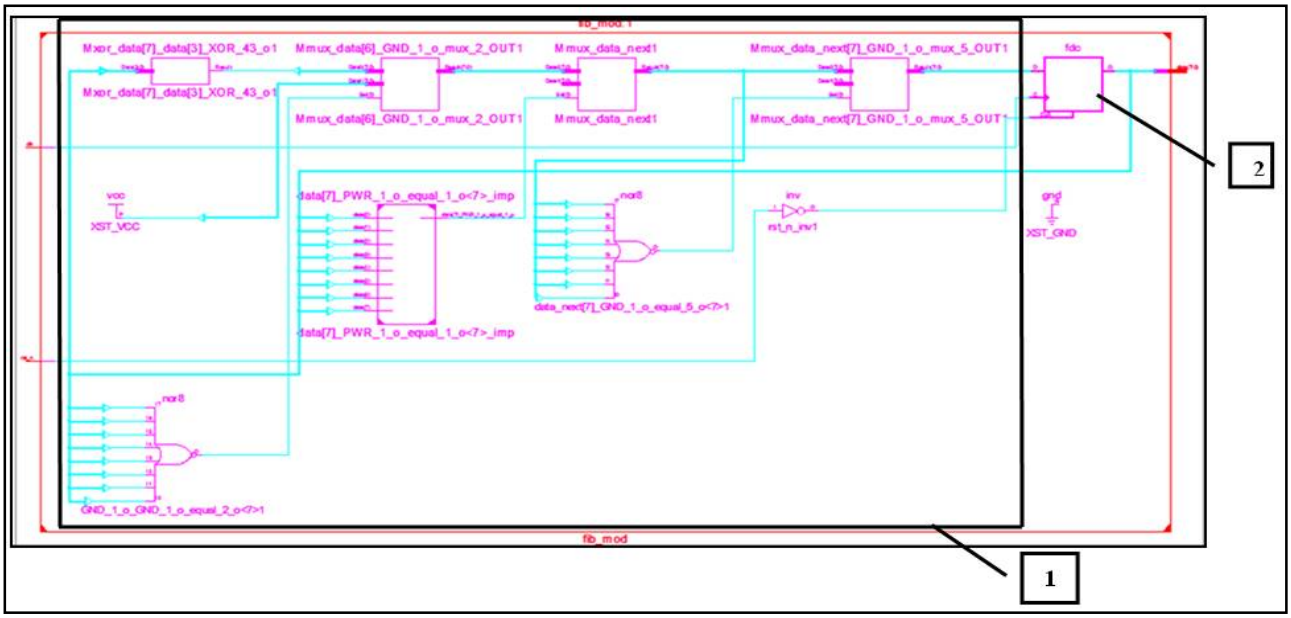

Figure 6: RTL Schematic of State based LFSR

The RTL schematic depicted in figure 6 depicts state based LFSR. Marker 2 indicates the block of D Flipflop utilised as shift register as explained in the introduction and literature survey. Marker 1 consists of the block which takes care of the polynomial equation as well as the condition to bypass the output entering stuck at state.

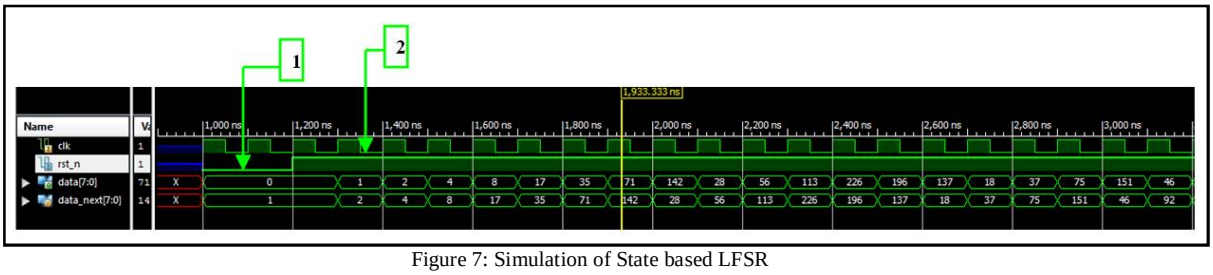

Figure 7: Simulation of State based LFSR

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Simulation result for initial stimulus is depicted in Figure 7. Marker 1 indicates when reset is 0 which means that the LFSR is not activated thus it remains in state 0 that means the output is zero. When the reset is made 1 upon one clock pulse delay (required for synchronisation) LFSR is activated and random test patterns are generated which is depicted by marker 2.

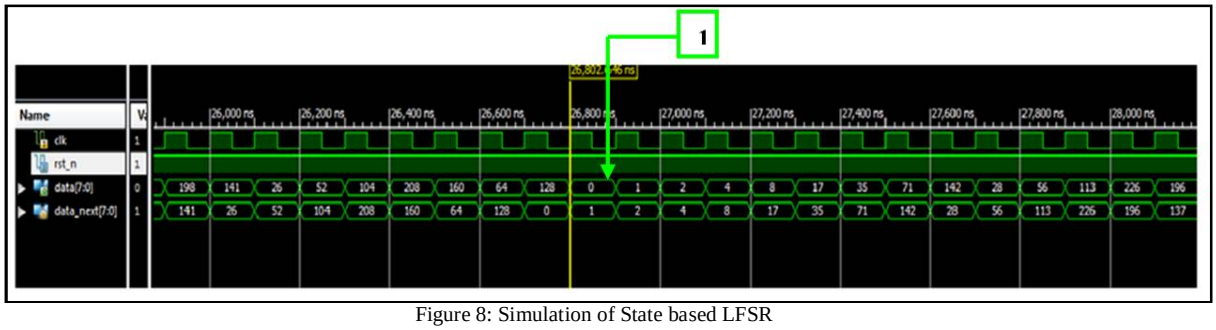

Figure 8: Simulation of State based LFSR

Simulation result for state based LFSR for repeating after 256 distinct states is shown in Figure 8. It can be observed that state 0 repeats after 26,800ns as pointed by marker 1. If in between reset is made 0, then again it goes back to state 0 and remains there until reset is made high. From Figure 7 and 8, the pattern starts at 1200ns and repeats after 26,800ns with a step size of 100ns therefore yields 256 distinct states.

Table 1: Power Comparison of Five different LFSRs

Type of LFSR	Total power (nW)	Percentage power reduction
bitswap	9411.75	---
bitswap_f	9455.89	0.47%↑
bitswap_g	9449.98	0.41%↑
(Proposed Method) fib_mod	3235.99	65.62%↓
(Modified Method) galois_mod	3342.89	64.48%↓

Table 2: Area Comparison of Five different LFSRs

Type of LFSR	Total area(cells)	Percentage area reduction
bitswap	518	---
bitswap_f	529	2.12 %↑
bitswap_g	526	1.54% ↑
(Proposed Method) fib_mod	155	70.08%↓
(Modified Method) galois_mod	157	69.69%↓

Table 1 and Table 2 show the comparison of total area, total power and percentage reduction in power and area. It can be observed that *fib_mod* provides greater reduction in the power as well as area when compared to all other types of LFSR. This is possible because of logic optimisation obtained in the proposed method. From the RTL schematic shown in Figure 6 it can be observed that the proposed method consumes less hardware. The algorithm followed to implement proposed method leads to this reduction in area and power.

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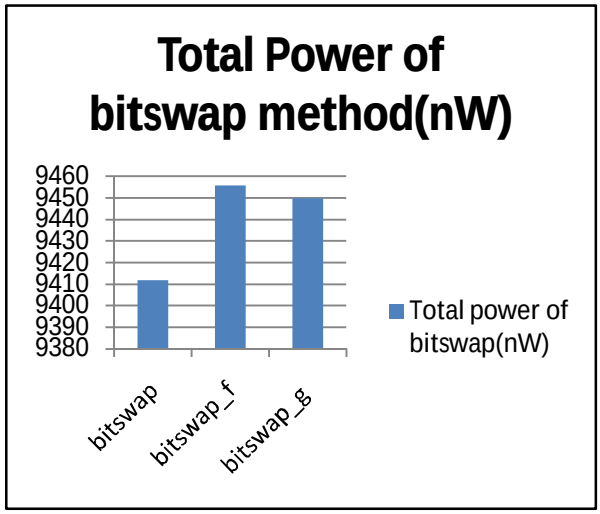
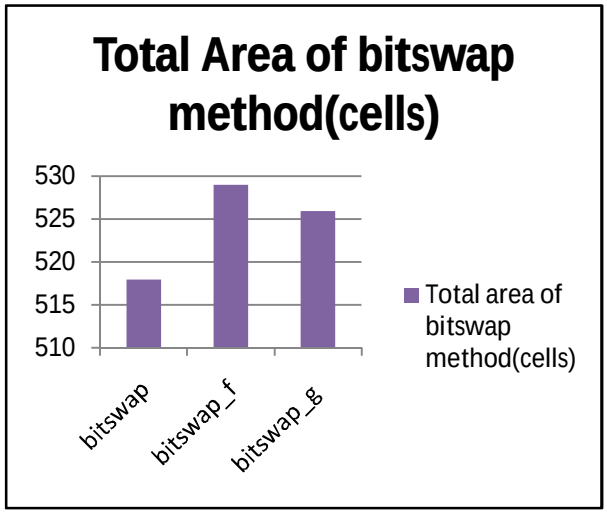
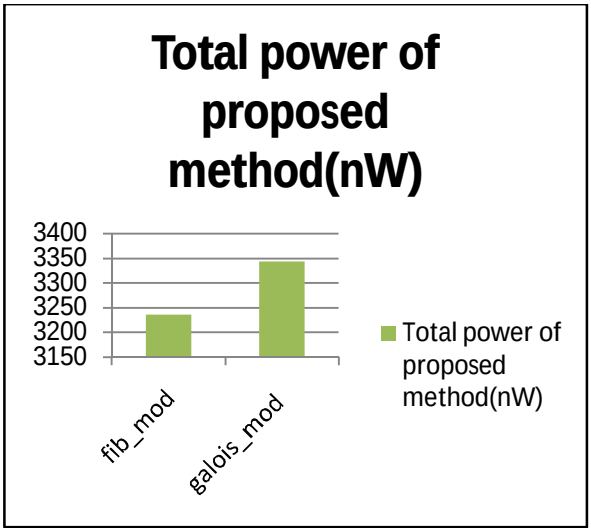


Graph 1: Comparison of Power of bitswap LFSR

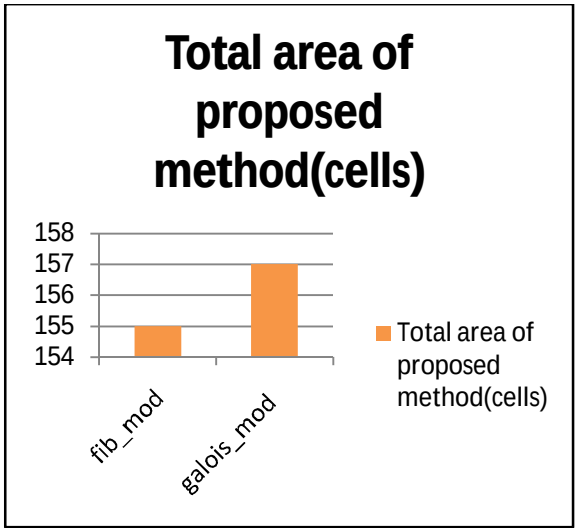


Graph 2: Comparison of Area of bitswap LFSR

Graph 1 accounts for the comparison of power consumed by bitswap method as explained earlier in the proposed method section. It can be observed that bitswap method consumes less power compared to the other two methods. Less hardware leads to less area therefore bitswap method consumes less area in terms of cells when compared to other two. This is depicted in Graph 2.



Graph 3: Power comparison by proposed method



Graph 4: Area comparison of proposed method

Graph 3 compares the total power consumed by proposed method alone and it can be observed that *fib_mod* consumes less power as compared to galois_mod. Separate comparison for two proposed methods and conventional method is done because the two LFSR designed as per proposed method consumes less power and less area than conventional. One possible explanation for this is the logic used in *fib_mod* method consumes less hardware that is with less number of logic blocks, the desired operation is achieved. Similarly from Graph 4, and *fib_mod* consumes less area.

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V. CONCLUSION AND FUTURE WORK

For synthesis slow_normal library in cadence (180nm) has been used and for simulation Xilinx 14.7 has been used. The main concentration is only on LFSR block designed for 8 bit, and comparison is made for different types of LFSR design in terms of total power (in nW) and total area. From Table 1, Table 2, Graph 1, Graph 2, Graph 3 and Graph 4 it can be observed that *fib_mo*d yields lower total power and total area respectively. *fib_mo*d is a modified Fibonacci LFSR as per the explanation in proposed method section.

REFERENCES

1. Xiaoqing Wen, "VLSI Testing and Test Power", Green Computing Conference and Workshops (IGCC), 2011 International.
2. Sakthivel, P, A. NirmalKumar and T. Mayilsamy," Low Transition Test Pattern Generator Architecture for Built in Self Test", American Journal of Applied Sciences, Vol.9, issue.9, pp. 1396-1406, 2012.
3. Sabir Hussain, K Padma Priya, "Test Pattern Generator (T PG) for Low Power Logic Built In Self-Test (BIST)", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vo l.2, Issue 4, April 2013.
4. S. Kundu and S. Chattopadhyay," Embedding a Low Power Test Set for Deterministic BIST using a Gray Counter" , Proceedings of the World Congress on Engineering, London, U.K, Vol II, July 6 - 8, 2011.
5. Pradhan, D.K and C. Liu," EBIST: A novel test generator with built in fault detection Capability", IEEE Trans. Comput. Aided Design Integrated Circ. Syst., 24: 1457-1466. DOI 10.1109/TCAD.2005.850815.
6. Chethan J, Manjunath Lakkannavar ," Design of Low Power Test Pattern Generator using Low Transition LFSR for high Fault Coverage Analysis", I.J. Information Engineering and Electronic Business, 2, pp.15-21, 2013.
7. Emina Milovanovic, Mile Stojcev, Igor Milovanovic, Tatjana Nikolic, "Concurrent Generation of Pseudo Random Numbers with LFSR of Fibonacci And Galois type", Computing and Informatics, Vol. 34,pp. 941-958, 2015.
8. Praveen Kasunde, Dr. K B ShivaKumar, Dr. M Z Kurian, "Improved Design of Low Power TPG Using LPLFSR", International Journal of Computer & Organization Trends ,Vol.3, Issue4 , May 2013.
9. Senthil Kumar. G, Paramasivam. K, "Test Power Minimization of VLSI Circuits: A Survey", 4th ICCCNT 2013,IEEE – 31661, july 4-6 2013 .
10. Kumara Swamy.H.L, Yasha Jyothi M Shirur, Veena S Chakravarthi, " Implementation of Logic BIST for the Digital Design Core", National conference on Recent Advances in Electronics & Communication Engineering, pp 1-5,May-2013.
11. Patrick Girard, Xiaoqing Wen, Nur Touba. "Low Power Testing". Morgan Kaufmann. System-on-Chip Test Architectures: Nanometer Design for Testability, pp.207-350, 2007.
12. Kaushal Buch,"Tutorial 6: Study and Implementation of Digital Noise Source",CASPER[online], Available https://casper.berkeley.edu/wiki/Tutorial_-_Noise_Source.

BIOGRAPHY

Dr. Yasha Jyothi M Shirur is a Professor in the department of Electronics and Communication, BNMIT, Bengaluru, Karnataka, India has over 17 years of academic and research experience. She is active in promoting VLSI research in academics and has filed first patent for BNMIT on "Method, System and Apparatus for Asynchronous SOC Testing and Validation" She has published more than 25 technical papers in National and International conferences and journals and guided more than 15 Post Graduate projects and 25 Under Graduate projects. She is Execom member of IEEE Nano Technology Council, Bangalore Section and is Life member ISTE.

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