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1-Bit Hybrid Full Adder by GDI and PTL Technique

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ABSTRACT- In this paper we have proposed a novel design of a 1 bit full adder hybrid circuit which consists of two techniques *i.e.* Gate Diffusion Input (GDI) technique and Pass Transistor logic (PTL) technique. Here we are using 180 nm technology and width i.e. *1µm.*and *2µm.* This method is used for the designing of fast, low power and area efficient circuit. Number of transistor used in this proposed model is 10. Average power dissipation, delay and power delay product of the circuit has been analyzed. To analyze the performance, at the end comparison of 1 bit adder by GDI-PTL (hybrid) logic has been made with 1 bit full adder by conventional CMOS, PTL logic and GDI logic. Analysis shows that the proposed hybrid 1 bit full adder has the minimum power delay product i.e. 4.68×10^{-15} J. Simulation results are performed on Cadence Virtuoso tool.

KEYWORDS: Gate Diffusion Input; Pass Transistor Logic; average power dissipation; power delay product; delay.

I. INTRODUCTION

Power dissipation and delay in the circuit are the main issues which we as a VLSI design engineers are facing today. We have various technologies on which we can work and design our circuits but at the same time there are some limitations on every design technology which cannot be denied. Operation like AND, OR, subtraction and addition are mostly and commonly used in the application such as DSP, image processing and microprocessors. As logic gates are the building blocks of all the digital circuit also in arithmetic circuits, 1 bit full adders are mostly used. So to increase the overall performance of the circuit, the performance analysis from the basic unit has to be done.

From the perspective of delay, throughput and latency are the major constraints for the addition performed in the DSP applications. In adder circuits not only delay arises but also a huge amount of power dissipates. So our main focus is to reduce power dissipation and delay in the circuit. But side by side one has to consider the size of the circuit because it plays a significant role in the days of miniaturization. Both power dissipation and the delay in the circuit are paradox. If we want fast circuit then the delay in the circuit should be minimum but if the circuit is fast then large amount of energy will dissipate in short amount of time which causes heating and burning of the circuit. This brought extra load on the designer to remove the maximum heat from the circuit which is very difficult task. So we want three things in our design 1) minimum delay 2) low power dissipation and 3) minimum circuit size.

There are different logic styles which favor one aspect at the cost of other. Static complementary metal-oxide-semiconductor (CMOS) [1], dynamic CMOS logic [2], complementary pass transistor logic (CPL) [3] and transmission gate adder [4] are mostly used logic design styles in the conventional domain. There are many design style which consist of more than one logic style known as hybrid-logic design style. By the use of hybrid-logic design style more than one aspect of design can be improve.

The advantages of conventional CMOS adder (with 28 transistors) are its property to stand strong against voltage scaling and transistor sizing but on the other side its high input capacitance and buffer requirement becomes its disadvantage [1]. Pass transistor logic (PTL) design technique come along with the advantages like 1) high speed [5], 2) low power dissipation [6] and 3) low interconnection effect [7, 8]. High speed due to small node capacitances, low power dissipation due to less number of transistor and low interconnection effect due to small area. There are also some disadvantages of PTL design techniques, there is threshold drop across the single channel pass transistor also the high input voltage level at the regenerative inverter is not V_{dd}. Gate diffusion input (GDI) technique have many advantages like 1) low power circuit design 2) reducing propagation delay 3) reducing area of digital circuit 4) maintain low complexity of the circuit

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II. PREVIOUS WORK

In last few decades there is significant development in the scenario of design. Adder which is considered to be basic blocks of application like ALU, DSP and microprocessors always been under scrutiny now or then.1bit full adder gate level circuit has been shown in Fig 1. Boolean expression of full adder is

$$sum = A \oplus B \oplus C$$

$$carry = AB + BC + CA$$

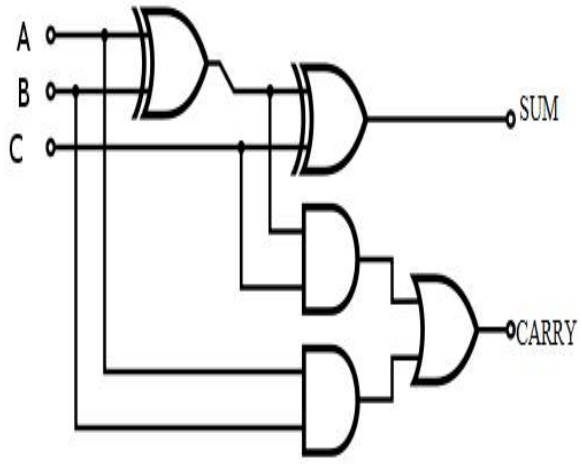

Fig 1. Gate level circuit of 1 bit full adder

From 28 transistors 1 bit full adder we are here now with 10 transistor 1 bit full adder. There are many design logics by which 1 bit full adder can also be derived. The conventional CMOS style based adder (with 28 transistors) is very robust against transistor sizing and voltage scaling. Other design is the mirror adder having same transistor count and power dissipation as in conventional CMOS but carry propagation path delay is smaller than CMOS. There is another design style by CPL which uses 32 transistors which turn out as not a intelligent choice for low power application but it shows good voltage swing. The voltage degradation is the main disadvantage in CPL which can be removed by TGA which only uses 20 transistors [9, 10].

A big step has been taken by the researcher to focus on the hybrid logic approach which can improve many aspects of design parameters. A 14-transistor full adder has been design by vesterbacka [11], by using more than one logic style. Zhang et al [12], proposed a hybrid of pass logic with static CMOS output derive full adder (HPSC) which produce full output swing. But the problem arises in the hybrid circuit is that their performance degrades in the cascade mode.

III. APPROACH OF THE DESIGNED MODEL

The basic approach of this proposed full adder is to have a fast and low power adder circuit. Here we have used two design logic i.e. GDI and PTL combining both we are going to analyze the result of the circuit. It basically consists of three modules, one is made by GDI second is by PTL and other is inverter by CMOS . Various disadvantages and advantages have been discussed above, so this design model came up with mixed results of both the techniques.

Module 1 is made by GDI technique which consists of 4 transistors as shown in Fig. 2. On comparing with conventional CMOS, GDI xor cell consist of less number of transistors. Output of module 1 has been carried out by module 2 which consists of 4 pass transistors to give sum as one output and carry as the other. Module 3 consists of inverter to fetch a inverted output which is given to the input of module 2. So total number of transistors used in this model is 10.

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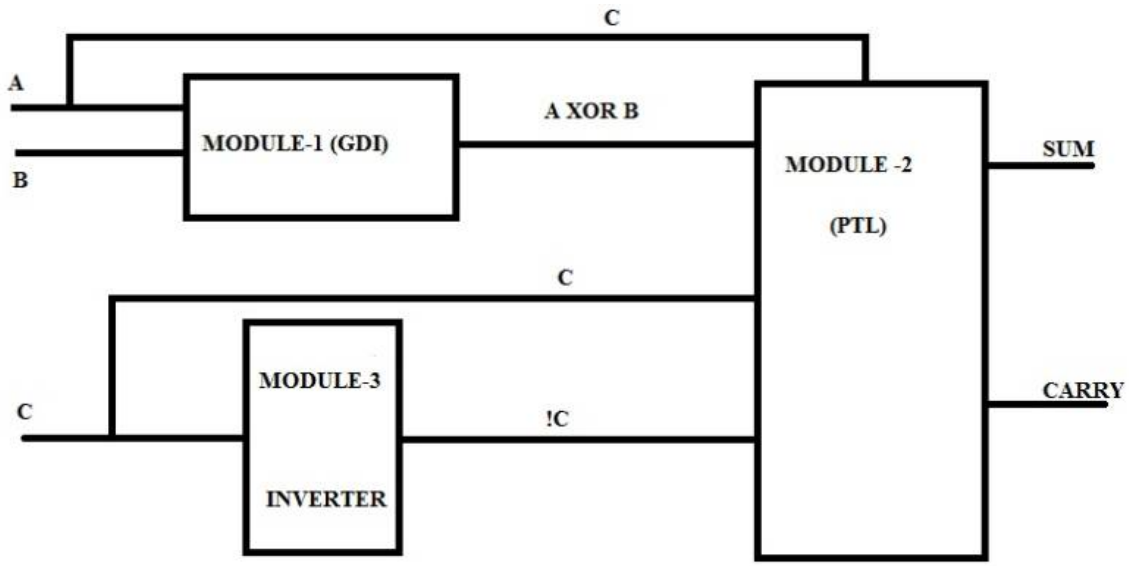

Fig. 2. Hybrid 1 bit full adder module

IV. ANALYSIS OF 1 BIT FULL ADDER BY PTL AND GDI TECHNIQUE

The common problem in both GDI and PTL techniques is the low swing output because both the techniques don't includes V_{dc}. Here we have analyzed a 1bit full adder by both the GDI and PTL techniques separately. Number of transistors used in GDI is 10 whereas in PTL number of transistors is 16. When *W= 2µm*, maximum power dissipation in GDI is 1.92 x 10^{-3} w at 1.5V whereas in PTL maximum power dissipation is 119.3 x 10^{-6} w at 3V and maximum delay produced in GDI technique is 275.60 x 10^{-12} sec. at 1.5V whereas in PTL maximum delay produced is 25.06 x 10^{-9} sec. at 1.5V. When *W=1µm*, maximum power dissipation in GDI is 992.2 x 10^{-6} w 1.5V whereas in PTL maximum power dissipation is 65.49 x 10^{-6} w at 3V and maximum delay produced by GDI is 242.2 x 10^{-12} sec. at 1.5V whereas in PTL maximum delay produced is 25.05 x 10^{-9} sec at 1.5V. In both of the designs we have used V_{dc}=3.3V, V_{Th}=1V and L=180nm. 1 bit full adder by GDI and PTL has been shown in Fig. 3,4 whereas there waveform has been shown in Fig. 5,6.

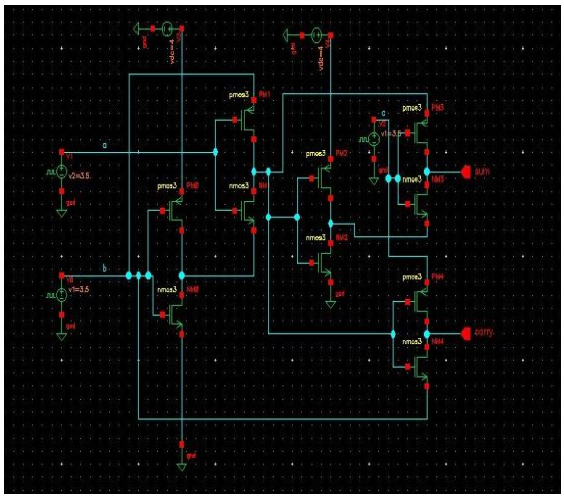

Fig. 3. 1 bit full adder circuit by GDI

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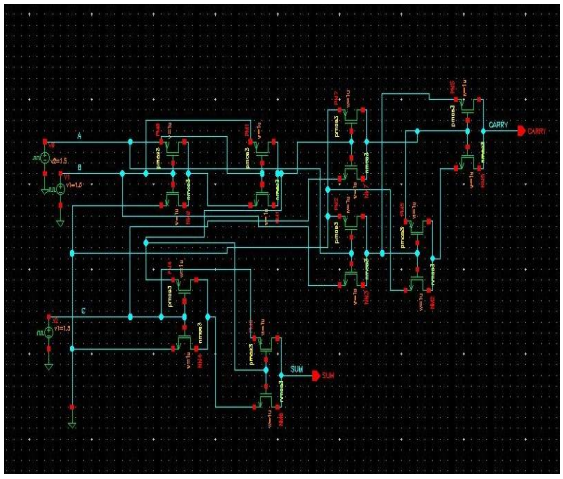

Fig. 4. 1 bit full adder circuit by PTL

Fig. 5. Graph of 1 bit full adder by GDI

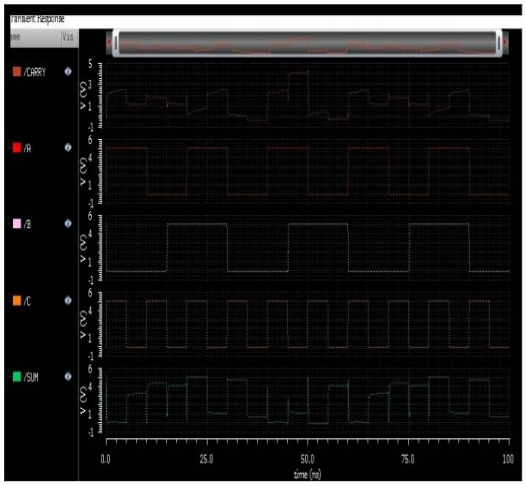

Fig. 6. Graph of 1 bit full adder by PTL

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V. COMPARISON OF LOGIC STYLES

In this work various models of full adder have been design and implemented. Working technology is 180nm with *W= 1µm* and *W= 2µm*. These circuits are simulated on the platform called cadence virtuoso at 3.3V, 33.3 MHz and 27°C. We have compared 1 bit full adder made by 20 transistors, 16 transistors (PTL), 10 transistors (GDI) and 10 transistors (GDI+PTL) on the basis of power dissipation, delay, power delay product (PDP) and transistor count. Comparison of above four design styles has been shown in Table 1 and 2. After analyzing the table we have concluded that power dissipation in (W) from maximum to minimum are in the order ***20T>GDI>hybrid>16T(PTL***) whereas delay are in the order ***hybrid>GDI>16T (PTL)>20T*** and power delay product ***20T>GDI>16T(PTL)>hybrid.***

VI. OPERATIONAL ANALYSIS OF HYBRID FULL ADDER

The proposed hybrid full adder combines both GDI and PTL techniques. It only consist 10 transistors as shown in Fig. 7 and graph of 1 bit hybrid full adder is shown in Fig. 8. While analyzing the performance of the hybrid adder we have come across with the data that its performance lie between the GDI and PTL full adder in terms of power dissipation and delay. But power delay product of the hybrid adder at 3V is minimum than both GDI and PTL. The behavior of this hybrid adder changes as we increase input voltage supply. This is because both the GDI and PTL does not produce full swing output due to unavailability of voltage source (V_{dc}). As we increase our input supply voltage (V_p) from 1.5V to 3V, more voltage can be transfer from input to output which can easily drive the other transistors. When *W= 1µm* and V_p =1.5V, power dissipation of hybrid adder is 887.9 x 10^{-6} w, delay is 1.77 x 10^{-9}sec and power delay product is 1.571 x 10^{-12} J and at V_p= 3V, power dissipation is 23.97 x 10^{-6}w, delay is 195.4 x 10^{-12}sec and power delay product is 4.68 x 10^{-15} J. When *W= 2µm* and V_p =1.5V, power dissipation of hybrid adder is 1.74 x 10^{-3} w, delay is 2.09 x 10^{-9}sec and power delay product is 3.63 x 10^{-12} J and at V_p= 3V, power dissipation is 64.24 x 10^{-6}w, delay is 183.5 x 10^{-12}sec and power delay product is 1.178 x 10^{-14} J. So as the input voltage increases from 1.5V to 3V, there is huge improvement in terms of all three aspects mainly in power delay product.

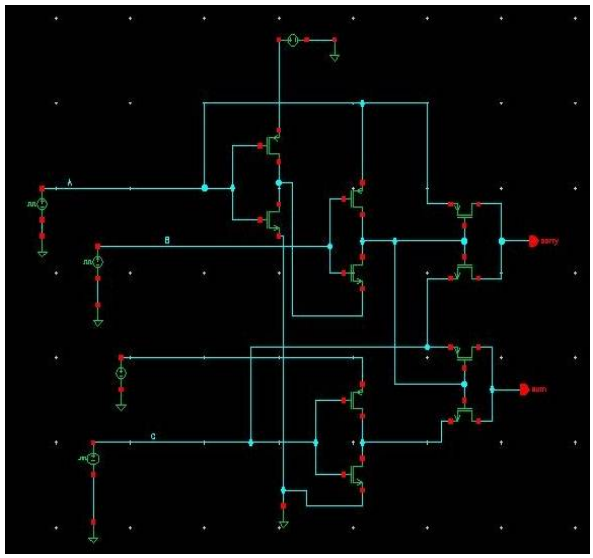

Fig. 7. Proposed 1bit hybrid full adder circuit

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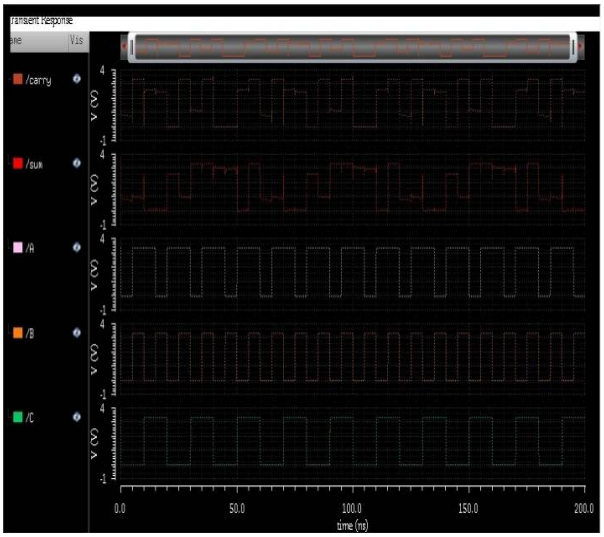

Fig. 8. Graph of 1bit hybrid full adder circuit

Table 1 Showing result of comparative analysis at W=1µm

V_p	Power dissipation (µW)				Delay (ps)				Power delay product (pJ)			
	20T	16T(ptl)	gdi	hybrid	20T	16T(ptl)	Gdi	hybrid	20T	16T(ptl)	gdi	hybrid
1.5V	2090	2.57	992.9	887.9	377.2	25050	242.2	1770	78.8	.0643	.240	1.571
2.0V	1350	10.23	777.1	510.3	157.1	5010	135.6	503.7	21.2	.0512	.0976	25.7
2.5V	674.4	30.8	460.7	155.1	124.9	406.8	125.6	294.6	.0842	.0125	.0578	.0456
3.0V	402.0	65.49	308.8	23.97	109.4	184	108.9	195.4	.0439	.0120	.0335	.00468

Table 2 Showing result of comparative analysis W=2µm

V_p	Power dissipation (µW)				Delay (ps)				Power delay product (pJ)			
	20T	16T(ptl)	gdi	hybrid	20T	16T(ptl)	Gdi	hybrid	20T	16T(ptl)	gdi	hybrid
1.5V	3980	4.716	1920	1740	401.1	25050	275.6	1770	1.59	11.81	52.9	3.63
2.0V	2690	18.64	1503	997.4	157.5	4490	135.6	503.7	42.3	.083	20.53	.0049
2.5V	1280	57.28	891	291.3	124.8	509.8	125.6	294.6	15.97	.0292	1.119	.0802
3.0V	791	119.3	601.9	64.24	109.6	187.2	109.1	195.4	8.66	.0223	.0656	.0117

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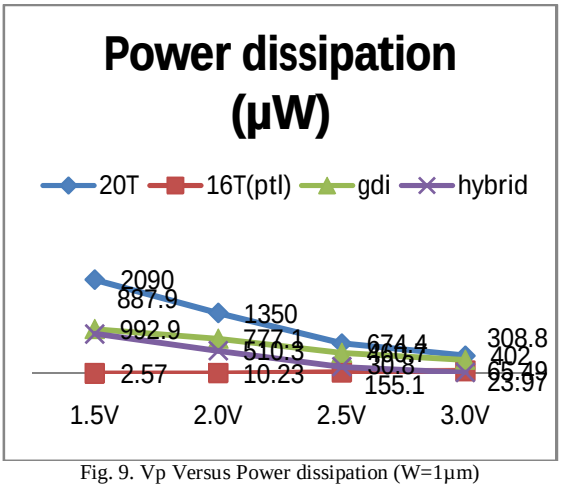

Fig. 9. Vp Versus Power dissipation (W=1µm)

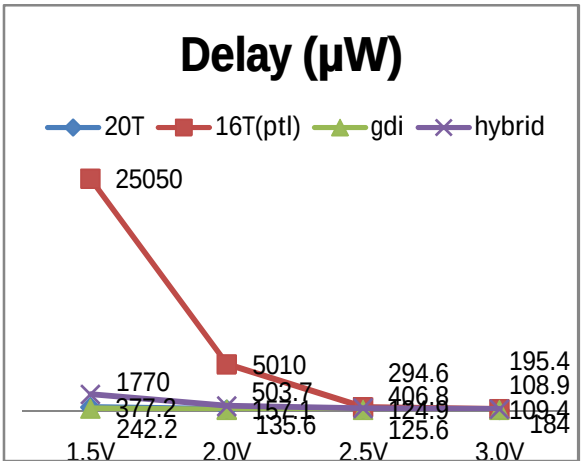

Fig.10. Vp Versus Delay (W=1µm)

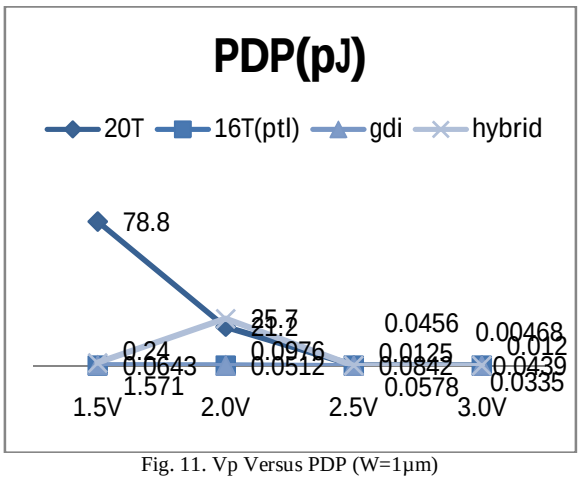

Fig. 11. Vp Versus PDP (W=1µm)

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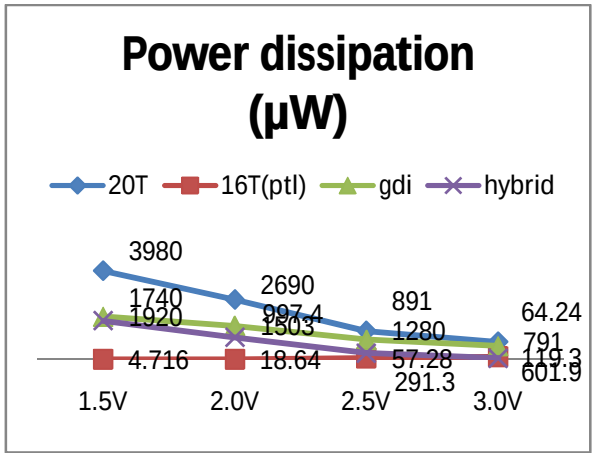

Fig. 12. Vp Versus Power dissipation (W=2µm)

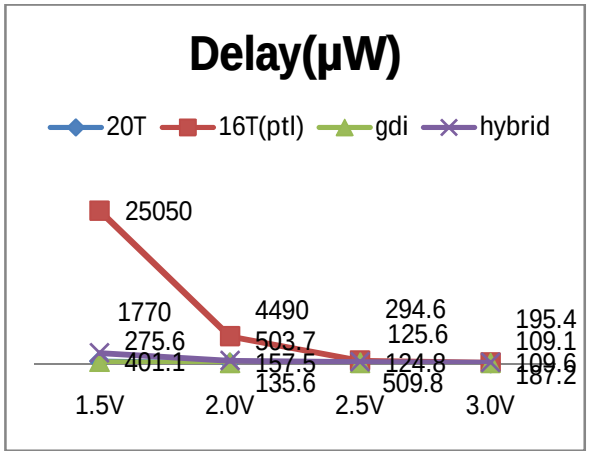

Fig. 13. Vp Versus Delay (W=2µm)

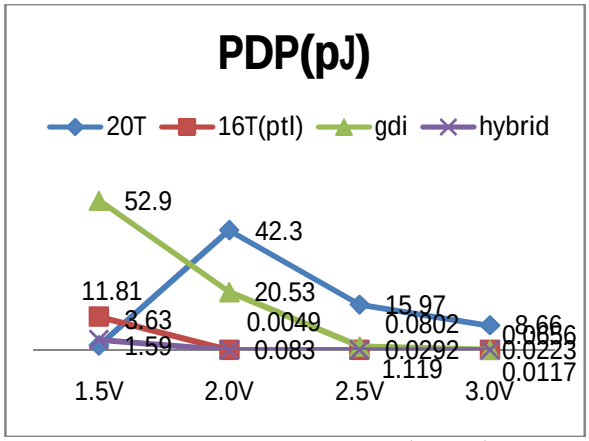

Fig. 14. Vp Versus PDP (W=2µm)

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VII. CONCLUSION

Various design model of full adder with different techniques have been shown in this paper with the conclusion that a hybrid circuit can be implement by using two or more different design styles. Here we analyzed mainly two techniques GDI and PTL, combining both of these techniques a new hybrid circuit has been proposed. The proposed adder combines the merit of both the techniques. It is quick due to module consist of GDI and dissipate less power due to module consist of pass transistors. It comes with the huge advantage in terms of power delay product.

VIII. FUTURE SCOPE

Due to less number of transistors and improved power delay product (PDP) this hybrid adder can be used in realizing a subtractor, multiplier, compressor, multiplexer and sequential circuits.

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BIOGRAPHY

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