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Design and Stimulation of Reliable Low Power CMOS Logic Gates

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ABSTRACT: the rapid increase in leakage power dissipation was caused by high device density and low threshold voltages. For some years, researchers have been interested in reducing leakage power in Cmos VLSI. There is a significant trade-off between technology scaling and static power consumption in Cmos IC design. Power Leakage Plays a Significant Role in Today's Technology Our research focuses on a low-power technology known as Gate Diffusion Input (GDI), which can be utilized for digital design at nanoscale foundries. Prior methodologies are considered and applied to AND gate, OR gate, Invertor, NAND gate, NOR gate, OR gate, Full adder, Half adder, Carry look ahead adder, Ripple carry adder for area and power comparison. On 22nm, 32nm all procedures are parametrically examined. Our suggested research compares GDI with other approaches in terms of power consumption, design delay and complexity, and number of transistors needed. The benefits of GDI are also presented in our suggested work.

KEYWORDS- CMOS, GDI, Gate, Power consumption, low power.

I. INTRODUCTION

The growing demand for low-power portable and implantable electronics on VLSI chips has resulted in recent advances in ultra-low-power designs. With improved power efficiency and throughput, VLSI design techniques are necessary. To keep the temperature of implantable electronics at a tolerable level, dissipated heat must be properly eliminated. It is vital to consider all power estimation and optimization considerations while constructing any ultra-low power circuit. As a result, specialized ultra-low power designing techniques are necessary to reduce dissipation to an acceptable level. Total power dissipation in any VLSI circuit is the sum of static and dynamic power dissipation.In nanoscale VLSI design, leakage current is one of the most important elements for static power dissipation, which is affected by leakage below the threshold, leakage at Reversed biased PN junctions, and leakage owing to carrier tunnelling. The activity factor, load capacitance, switching frequency, and supply voltage all affect dynamic power dissipation. When operated at a reduced supply voltage, small transistors with a narrow channel width produce an increase in static power dissipation. At various abstraction levels, low-power design methods can be maximised. Partitioning and power gating can be done at the system level for optimization, while complexity, concurrency, and regularity can be verified at the method level. Optimization can be done at three levels: strategy, logic, and technology Logic style changes and transistor resizing can be done at the logic level.This research concentrates on technology and logic level optimization, and presents the GDI technique as a new enhanced low power technique (Gate Diffusion Input) when compared to complementary CMOS technology (CCT), LECTOR technique, Multi threshold cmos technique (MTCMOS), and conventional approach, the suggested GDI technique has been found to be more power efficient. Our suggested research compares GDI with other approaches in terms of power consumption, design delay and complexity, and number of transistors needed. The benefits of GDI are also presented in our proposed work.

II. PROPOSED SYSTEM

A. **Basic GDI** *Cell*

The GDI approach relies on the employment of a basic cell like the one shown in Figure 1. The fundamental cell appears to be similar to a normal CMOS inverter at first glance, however there are three key differences: The GDI cell has three inputs: G, H, and I. (common gate input of nMOS and pMOS). P (input to the pMOS source/drain) and N(input to the nMOS source/drain). It should be noted that while not all functionalities are possible in conventional technology p-well CMOS, they can be implemented successfully in twin-well CMOS or SOI technologies. In following Subsections, we'll talk about this subject.
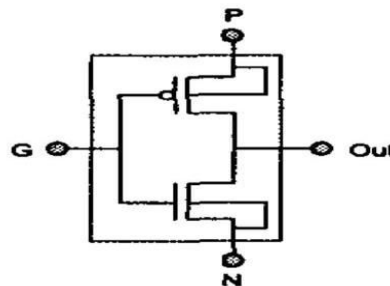

Fig 1: General GDI Cell

In CMOS and conventional implementations, the majority of these functions are complex (6-12 transistors), while in the GDI design process, they are quite basic (just 2 transistors per function).As can be observed, the GDI cell structure differs from prior techniques and has some key properties that allow for increased design complexity, transistor count, static power dissipation, and logic level swing. Understanding the features of GDI cells necessitates a more in-depth operational investigation of the basic cell in various circumstances and configurations.

N	P	G	Out	Function
'0'	B	A	A`B	F1
B	'1'	A	A`+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	A`B+AC	MUX
'0'	'1'	A	A`	NOT

Table 1: various logic functions of GDI cell for different Input configuration

B.OPERATION ANALYSIS OF GDI CIRCUITS

One of the frequent drawbacks with existing design methodologies, as discussed in section I, is the low swing of output signals due to the threshold drop across single-channel pass transistors. To circumvent this difficulty, previous solutions employ additional buffering hardware.

We propose the following analysis, based on the example of F1 functions, to understand the effect of low swing problem in GDI cell. Table 2 lists all of F1's logic states and associated functionality modes.

Table 2 shows that the only state in which the output value has a modest swing is A=0, B=0. Because of the weak high-to-low transition characteristics of pMOS pass transistors, the voltage level of F1 is V_{TP} (rather than the predicted 0V). The transition from A=0, B=V_{DD} TO A=0, B=0 is obviously the only instance (among all conceivable transistors) where the effect happens.

A	B	Functionality	F1
0	0	pMOS Trans Gate	V_{TP}
0	V_{DD}	CMOS Inverter	V_{DD}
V_{DD}	0	nMOS Trans Gate	0
V_{DD}	VDD	CMOS Inverter	0

Table 2: Input logic states vs. functionality and output swing of F1 function

The fact that the GDI acts as a standard CMOS inverter in around half of the cases (for B=1), which is extensively utilised as a digital buffer for logic level restoration, deserves special attention. When VDD='1' without a swing decrease from the preceding stage, a GDI cell acts as an inverter buffer and recovers the voltage swing in certain of these circumstances. Despite the fact that this function allows for self-swing repair in some circumstances.

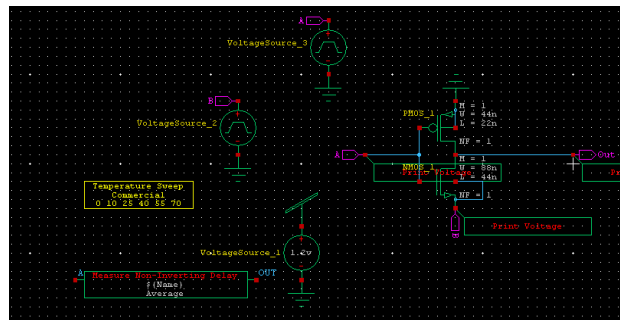### III. COMPARISONS WITH OTHER LOGIC STYLES

A.   AND Gate

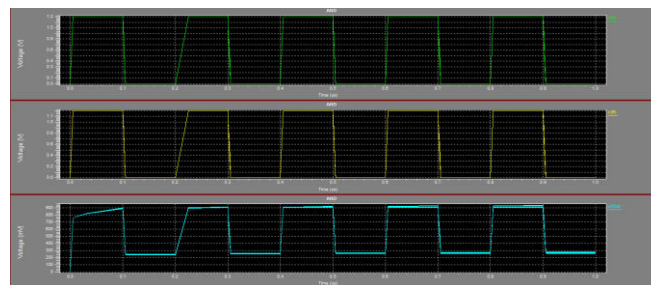**Fig 2: SCHEMATIC PRESENTATION OFAND GATE USING GDI TECHNIQUE**

Fig 3: OUTPUT WAVEFORM OF AND GATEUSING GDI TECHNIQUE

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	10	3.e-008	6.6e-010
CMOS	6	1.e-007	2.8e-010
CONVENTIONAL	12	7.e-009	4.9e-012
MTCMOS	6	1.e-007	2.8-010
GDI	**2**	**1.e-012**	**7.9e-010**

**Table 3: POWER DISSIPATION AT 0 DEGREE
TEMPERATURES ON 32nm.**

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	10	1.e-008	7.5e-010
CMOS	6	2.e-008	1.1e-010
CONVENTIONAL	12	6.e-011	1.1e-011
MTCMOS	6	2.e-006	2.5e-010
GDI	**2**	**1.e-012**	**6.7e-010**

Table 4: POWER DISSIPATION AT 0 DEGREE TEMPERATURES ON 22nm
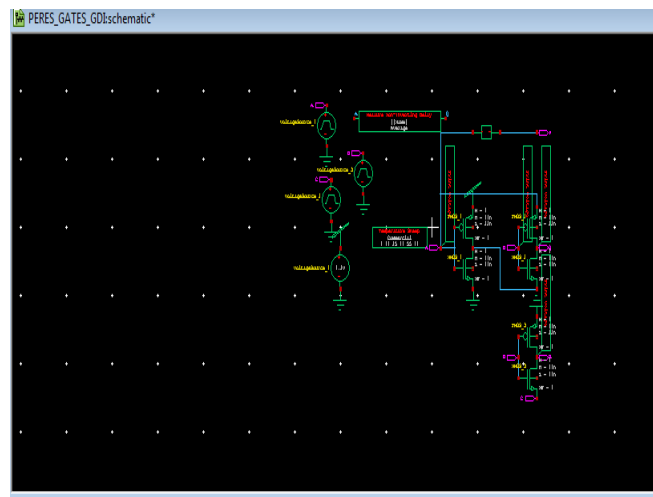
B.HALF ADDER

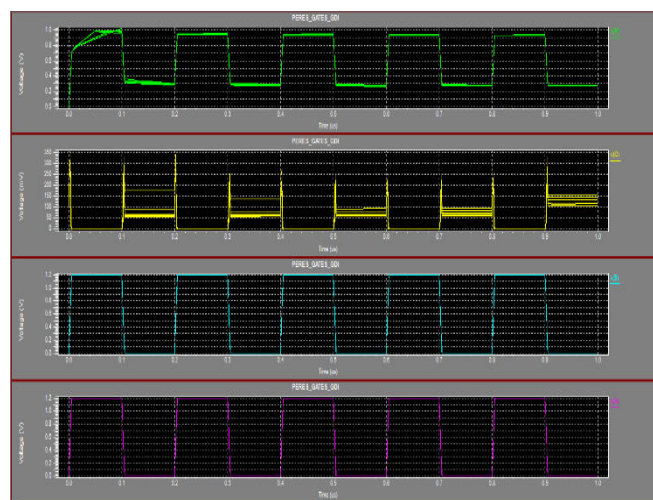**Fig 4: SCHEMATIC PRESENTATION OF HALF ADDER USING GDI TECHNIQUE**

Fig 5: OUTPUT WAVEFORM OF HALF ADDER USING GDI TECHNIQUE

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	28	2.1e-007	-5.026e-008
CMOS	22	3.3e-005	7.854e-010
CONVENTIONAL	22	2.9e-005	-4.999e-008
MTCMOS	48	7.6e-005	5.676e-010
GDI	**6**	**7.6e-007**	**2.254e-007**

Table 5: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 32nm

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	28	3.3e-008	1.506e-007
CMOS	22	2.0e-007	-1.327e-010
CONVENTIONAL	22	1.3e-00	5.032e-008
MTCMOS	48	1.8e-005	2.102e-010
GDI	**6**	**7.9e-008**	**4.565e-010**

Table 6: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 22nm

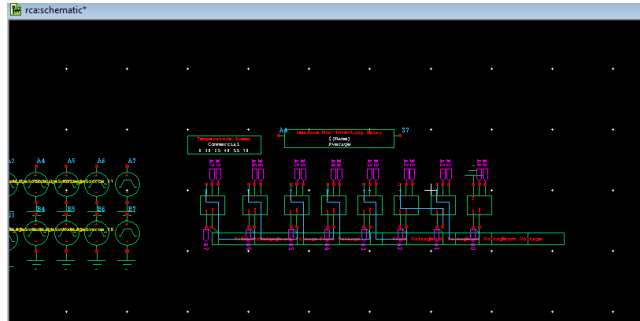**C.16 BIT RIPPLE CARRY ADDER**

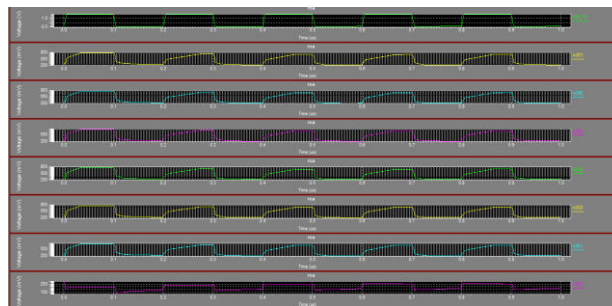**Fig 6: SCHEMATIC PRESENTATION OF RIPPLE CARRY ADDER USING GDI TECHNIQUE**

Fig 7: OUTPUT WAVEFORM OF RIPPLE CARRY ADDER USING GDI TECHNIQUE

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	64	3.1e-008	2.239e-009
CMOS	19	8.7e-008	2.204e-009
CONVENTIONAL	36	2.5e-004	4.765e-010
MTCMOS	70	4.2e-004	6.984e-008
GDI	**17**	**6.4e-013**	**0000e-000**

Table7: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 32nm

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	64	8.9e-006	1.151e-009
CMOS	19	3.8e-008	2.454e-009
CONVENTIONAL	36	7.2e-006	8.687e-007
MTCMOS	70	1.1e-004	0000e-000
GDI	**17**	**6.4e-013**	**0000e-000**

Table 8: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 22nm

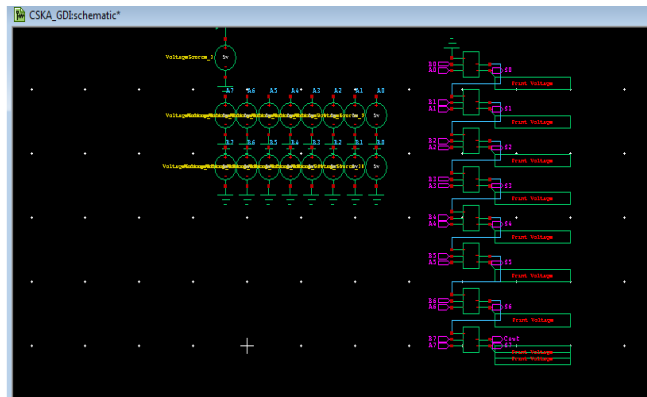**D.16 BIT CARRY LOOK AHEAD ADDER**

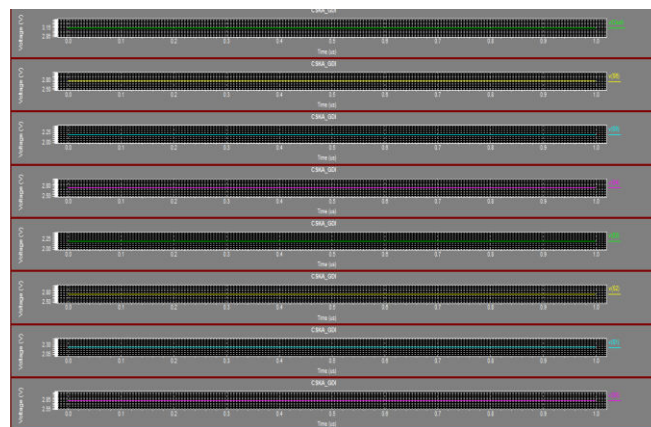**Fig 8: SCHEMATIC PRESENTATION OFCARRY LOOK ADDER USING GDI TECHNIQUE**

Fig 9: OUTPUT WAVEFORM OF CARRY LOOK AHEAD ADDER USING GDI TECHNIQUE

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	46	7.5e-004	0000e-000
CMOS	54	1.3e-002	0000e-000
CONVENTIONAL	36	2.7e-004	3.923e-008
MTCMOS	108	3.1e-004	5.867e-010
GDI	**18**	**9.5e-010**	**0000e-000**

Table 9: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 32nm

TECHNIQUE	NO.OF TRANSISTOR	POWER (W)	DELAY
LECTOR	46	7.4e-005	-4.974e-008
CMOS	54	5.7e-004	6.786e-010
CONVENTIONAL	36	3.0e-006	3.923e-008
MTCMOS	108	4.4e-006	2.675e-010
GDI	**18**	**6.7e-012**	**5.344e-010**

Table 10: POWER DISSIPATION AT 0 DEGREE TEMPERATURE ON 22nm

IV. CONCLUSION

The use of the innovative Gate-Diffusion Input (GDI) technology for low-power design was demonstrated. Using the GDI approach, a simple and efficient design algorithm based on the Shannon expansion can be used. As a result of the simulation, we can conclude that the GDI technology dissipates less power than the CMOS technique. We can also see that the GDI technique has less transistors than the other ways.VLSI circuit designers may find that GDI design adds to their toolkit.

As a result, in today's digital era, the GDI methodology is far more efficient than other methods.

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